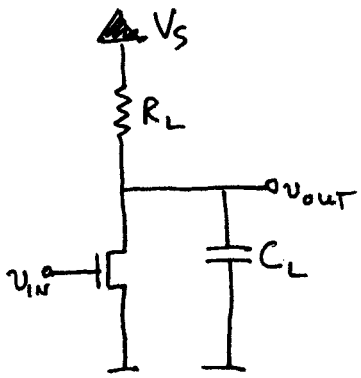
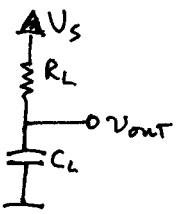
1. (A&L exercise 12.1)

6.002 PS12 Solutions Fall 2001



This is the same circuit as in section 12.3 of A&L. For a very detailed analysis, make sure you read through that section.

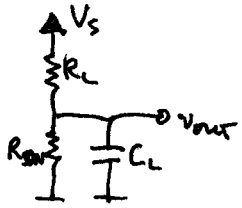
(a) Steady-state power refers to the power dissipated after any transients have died out, due to charging or discharging of the load capacitor. When a 0 is applied as input, our circuit looks like this:



When we have steady-state, our capacitor is fully charged, so it is an open circuit. Thus no current is flowing, and

$$P_{steady\text{-}state,0} = 0$$

(b) When a 1 is applied, we get:



Again at steady state our capacitor is an open, so

$$P_{steady\text{-}state,1} = \frac{V_S^2}{R_L + R_{ON}}$$

(c) The Static Power consumed in this circuit is the time averaged Steady state power. So for a sequence of 010101...

We get:

$$\overline{P} = \frac{E_1 + E_2}{T} = \frac{\left(\frac{V_S^2}{R_L+R_{ON}} \cdot \frac{T}{2} + 0 \cdot \frac{T}{2}\right)}{T}$$

$$P_{static} = \frac{V_S^2}{2(R_L+R_{ON})}$$

The dynamic power is consumed by the charging and discharging capacitor. We know that for a 0 input, the capacitor charges to $v_C = V_S$ and for a 1 input, the capacitor discharges to $v_C = V_S \cdot \frac{R_{ON}}{R_L+R_{ON}}$.

So for each transition, $P = \frac{1}{2} C_L v_C^2 = \frac{1}{2} C_L \left(V_S - V_S \cdot \frac{R_{ON}}{R_L+R_{ON}}\right)^2 = \frac{V_S^2 C_L}{2}\left(1 - \frac{R_{ON}}{R_L+R_{ON}}\right)^2$

Thus for average, it is this power averaged over time: $P_{Dynamic} = \frac{2 \cdot P}{T} = \frac{V_S^2 R_L^2 C_L}{(R_L+R_{ON})^2 T}$

(d) So if we know that $P_{dynamic} = \frac{V_S^2 R_L^2 C_L}{(R_L+R_{ON})^2 T}$ then,

(i) if T is doubled, $P_{dynamic}$ is halved

(ii) if V_S is halved, $P_{dynamic}$ is quartered

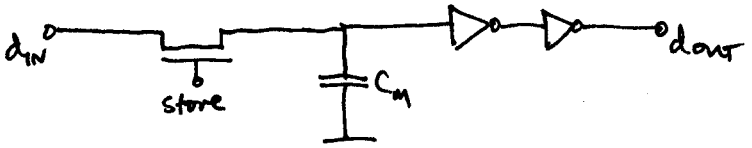
(iii) if C_L is halved, $P_{dynamic}$ is halved

(e) We can see that the main effect of R_L on the total power consumed in this circuit is in the denominator of our function.

$$P_{total} = \frac{V_S^2}{R_L+R_{ON}}\left(\frac{1}{2} + \frac{R_L^2 C_L}{(R_L+R_{ON})T}\right)$$

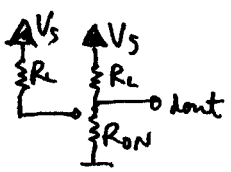
Thus to minimize powers, we want to maximize R_L, but pay attention to our constraints at the same time. We have to watch out make sure the static discipline is always followed to ensure good logic, and also not to make R_L so large that it negates the effect of the rest of the circuit.

2. (A&L 12.4)

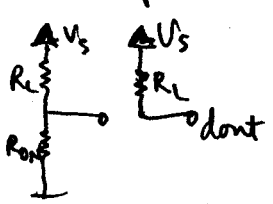


Because we are using NMOS inverters, no current flows from my capacitor to my inverters. Since there is no source of current flow except in my inverters, that is the only place current can flow and power dissipate.

For a 0 input,



For a 1 input,



Either way, instaneous power dissipated is just

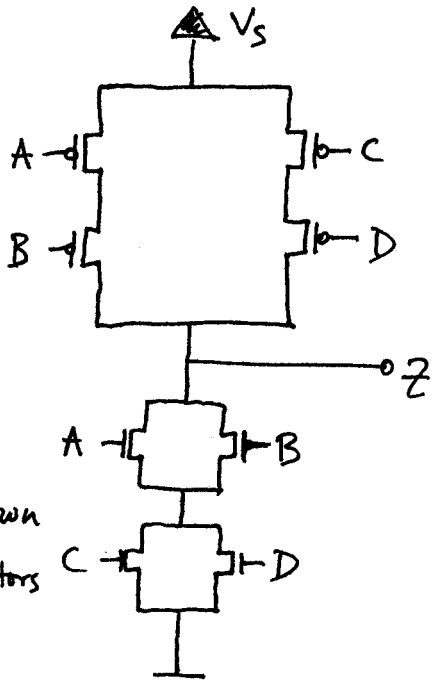
$$P = \frac{V_S^2}{R_L+R_{ON}}$$

3. (A&L 12.5 #2,3)

2) $Z = \overline{(A+B)\cdot(C+D)}$ $*_1$

$= \overline{(A+B)} + \overline{(C+D)}$

$= (\overline{A}\cdot\overline{B}) + (\overline{C}\cdot\overline{D})$ $*_2$



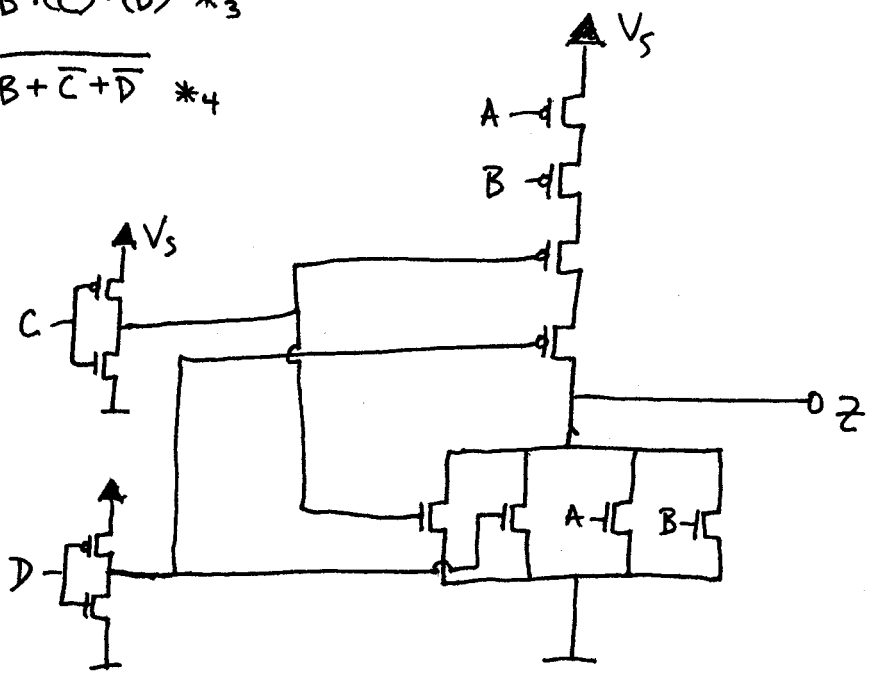
We use $*_2$ as our pullup circuit made with PMOS transistors

and $\overline{*_1}$ as our pulldown circuit using NMOS transistors

3) $Z = \overline{A}\cdot\overline{B}\cdot C\cdot D$

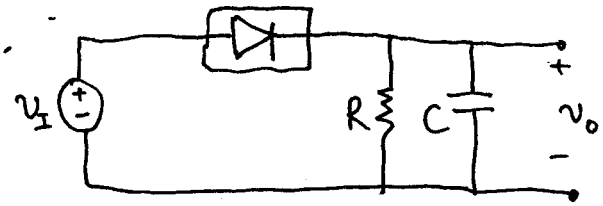
$= \overline{A}\cdot\overline{B}\cdot\overline{(\overline{C})}\cdot\overline{(\overline{D})}$ $*_3$

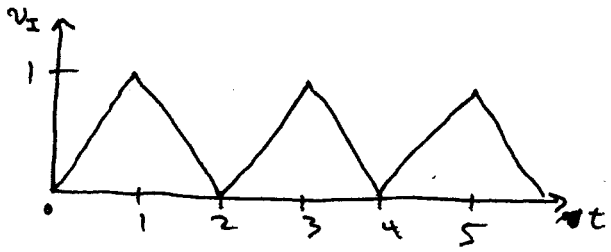
$= \overline{A+B+\overline{C}+\overline{D}}$ $*_4$



This time we use $*_3$ as our pullup and $\overline{*_4}$ as our pulldown, noting that we must invert our C & D inputs before getting to the main logic.

4.





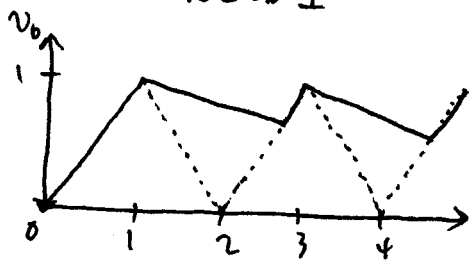
For all three of these cases, this is just a peak detector. Thus, from $t=0$, v_o will follow v_I upto the peak at $t=1$, and when v_I begins to drop, the diode will shut off. At this point, the charged capacitor will just discharge through the resistor. This happens until the rising v_I again equals v_o on its way up, and again, v_o follows v_I to the peak.

So, when diode is on, $v_o = v_I$

and when diode is off, $v_o = 1 \cdot e^{-(t-t_p)/RC}$

where t_p is the time of a peak

(a) When $RC \gg 1$

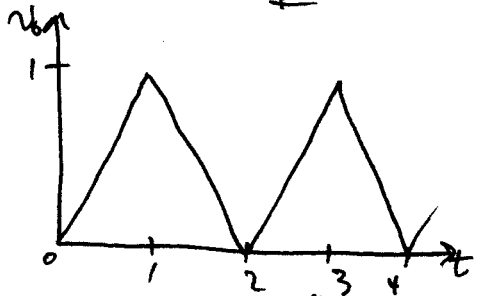


dotted line = v_I

solid line = v_o

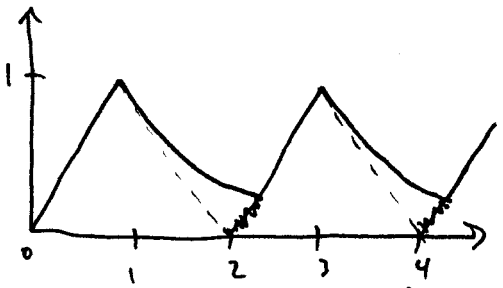
We see that it has a long time constant, so the exponential just looks linear, and it has a shallow slope down.

(b) When RC ~~<<~~ 1



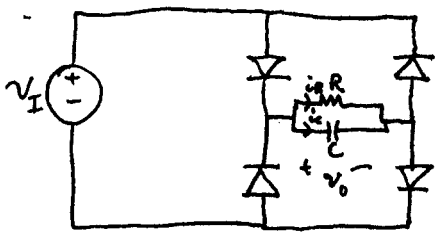
When τ is ~~big~~ small, it just becomes a follower for all time

(C) When $RC = 1$



When $\tau = 1$, $v_o = e^{-t}$, so we know that we will notice the intersection, and that it will occur a little after 1 sec. later.

5.

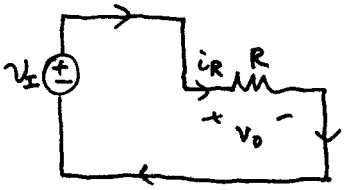


$v_I = 12 \sin(120\pi t)$

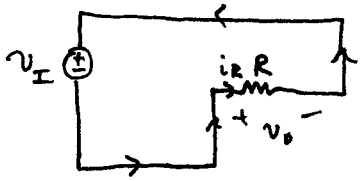
$RC = 1/6$

Let us conceptually think about what is going on in this circuit by just thinking of a resistor being at the bridge. In that case, we would find that we have two possible circuits; 1 for $+v_I$ and one for negative v_I.

Case I: $v_I > 0$

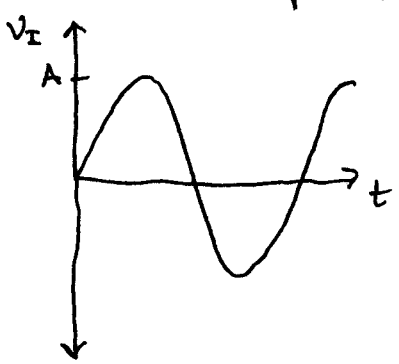


Case II: $v_I < 0$

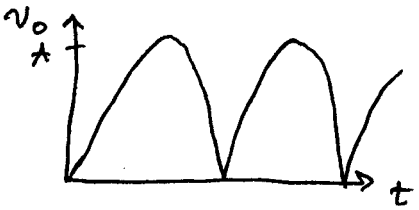


This we get just by realizing when each diode will be either an open circuit or a short circuit, considering its v_D or i_D relation.

Interestingly, for each case, the current through the bridge resistor is in the same direction, and thus we find that for sinusoidal input:



we get this output

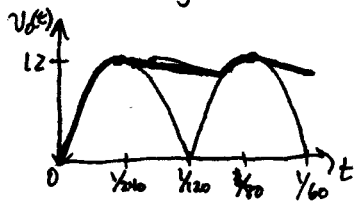


So conceptually, if there were just a resistor, this would just rectify the input so we get $v_o = |v_I|$

Now lets go back to when we learned about the half-wave rectifier and the peak detector. For the peak detector, all we did was add a capacitor in series with the resistor in the half-wave rectifier, and we got that interesting effect of slow decay after following the peak.

This circuit is analogous.

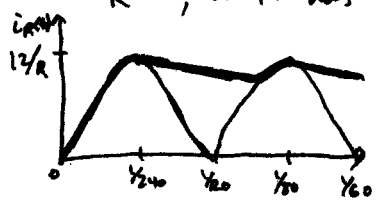
(a) $v_o(t)$ is just like a better peak detector than our original one.

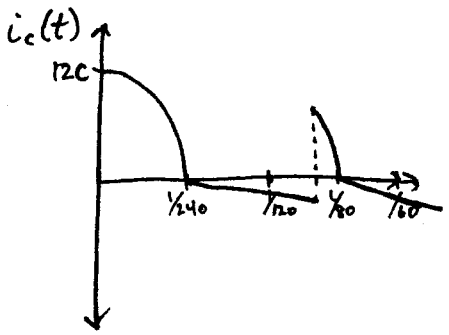


light line = $|v_\Sigma(t)|$, $\frac{|v_\Sigma(t)|}{R}$

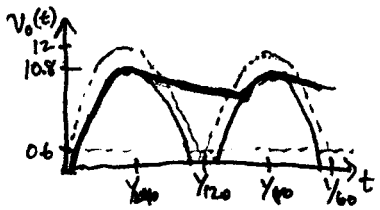
DARK LINE = $v_o(t)$, $i_R(t)$

$i_R(t) = \frac{v_o(t)}{R}$, so it has the same shape



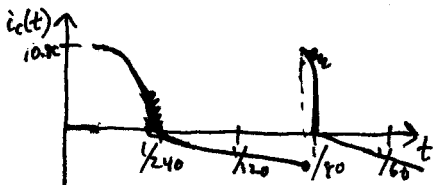


(b) With the 0.6V model added in, we now just decrease our max $v_o(t)$

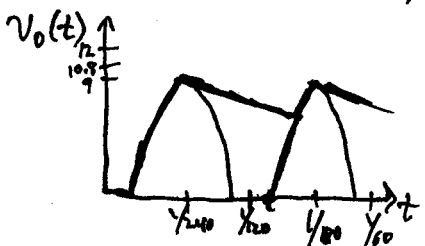


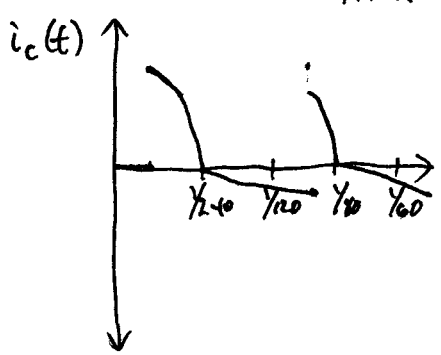
$12 - 2 \times 0.6V = 10.8V$

Again, $i_R(t) = \frac{v_o(t)}{R}$, so it just follows



(c) With R_{ON}'s at 0.1R, now when v_c is charged, $\frac{10.8V}{1.2R} = v_{o_{MAX}}$.



$12 - 2 \times 0.6 = \frac{10.8}{1.2R} = \frac{9V}{R}$

$i_R(t) = \frac{v_o(t)}{R}$