6.002 PROBLEM SET #5 SOLUTIONS

1. THE MAIN CONCEPT BEHIND DETERMINING THE VALUES IN PARTS (a) THROUGH (d) IS THAT WE HAVE TO MAKE SURE THAT NOISE IS NOT AMPLIFIED. THE WAY WE DO THIS IS BY MAKING SURE THAT ANY PORTION OF THE GRAPH WHICH HAS GAIN > 1 IS BETWEEN V_{OH} and V_{OL} OR V_{IH} and V_{IL}. THUS WE FIND THE POINTS ON THE GRAPH WHICH ARE PARALLEL TO OUR LINE OF $V_{IN} = V_{OUT}$. THESE POINTS WILL GIVE US OUR MAXIMUM LOW THRESHOLDS, AND OUR MINIMUM HIGH THRESHOLDS.

(a) MAX $V_{OL} = 0.18\ V$
(b) MIN $V_{OH} = 0.88\ V$
(c) MAX $V_{IL} = 0.38\ V$
(d) MIN $V_{IH} = 0.58\ V$

TO FIND OUR RANGE OF NOISE MARGINS FOR LOW INPUTS, WE HAVE TO FIND OUR MINIMUM VALUES FOR V_{IL} and V_{OL}. THIS WOULD BE THE POINT AT WHICH THE CURVE HAS SLOPE OF ZERO.

SO, MIN $V_{IL} = 0.2\ V$
MIN $V_{OL} = 0.1\ V$

NOW THE DEFINITION OF NOISE MARGIN IS $V_{IL} - V_{OL} = NM_L$

SO, MAX $NM_L = (\text{MAX } V_{IL}) - (\text{MAX } V_{OL}) = 0.38\ V - 0.18\ V = 0.2\ V$
MIN $NM_L = (\text{MIN } V_{IL}) - (\text{MIN } V_{OL}) = 0.2\ V - 0.1\ V = 0.1\ V$

THEREFORE, $\boxed{0.1V \leq NM_L \leq 0.2V}$

2. (A&L 5.1, p.368. PARTS (c) and (f) ONLY)

(c)

A	B	C	$\overline{B}$	$A\overline{B}$	BC	$\overline{A\overline{B}}$	$\overline{BC}$	$(\overline{A\overline{B}})(\overline{BC})$	$\overline{(\overline{A\overline{B}})(\overline{BC})} = Z$
0	0	0	1	0	0	1	1	1	0
0	0	1	1	0	0	1	1	1	0
0	1	0	0	0	0	1	1	1	0
0	1	1	0	0	1	1	0	0	1
1	0	0	1	1	0	0	1	0	1
1	0	1	1	1	0	0	1	0	1
1	1	0	0	0	0	1	1	1	0
1	1	1	0	0	1	1	0	0	1

NOW WE CAN DERIVE OR BOOLEAN EXPRESSION IN TWO WAYS. ONE IS USING DE MORGAN'S LAWS. THE OTHER IS BY DOING MSP.

$Z = \overline{(\overline{A\overline{B}})(\overline{BC})}$

$\boxed{Z = A\overline{B} + BC}$

OR

$Z = \overline{A}BC + A\overline{B}\overline{C} + A\overline{B}C + ABC$

$= A\overline{B}C + A\overline{B}\overline{C} + ABC + \overline{A}BC$

$= A\overline{B}(C+\overline{C}) + (A+\overline{A})BC$

$\boxed{Z = A\overline{B} + BC}$

(f)

A	B	C	$\overline{B}$	$A+\overline{B}$	$B+C$	$\overline{A+\overline{B}}$	$\overline{B+C}$	$(\overline{A+\overline{B}})(\overline{B+C})$	$\overline{(\overline{A+\overline{B}})(\overline{B+C})} = Z$
0	0	0	1	1	0	0	1	0	1
0	0	1	1	1	1	0	0	0	1
0	1	0	0	0	1	1	0	0	1
0	1	1	0	0	1	1	0	0	1
1	0	0	1	1	0	0	1	0	1
1	0	1	1	1	1	0	0	0	1
1	1	0	0	1	1	0	0	0	1
1	1	1	0	1	1	0	0	0	1

FROM MSP, $\boxed{Z = 1}$

USING DE MORGAN'S: $Z = \overline{\overline{(A+\overline{B})}\,\overline{(B+C)}}$

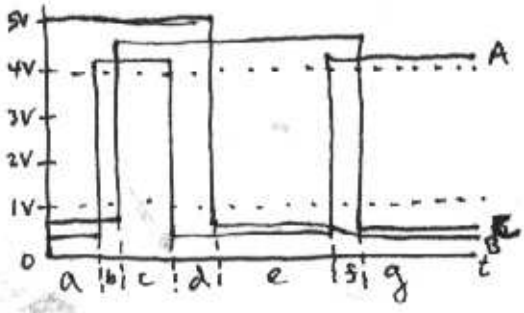
$= (A+\overline{B}) + (B+C)$

$= (A+C) + (B+\overline{B})$

$= (A+C) + 1$

$\boxed{Z = 1}$

3. (A&L 5.2, p.370)

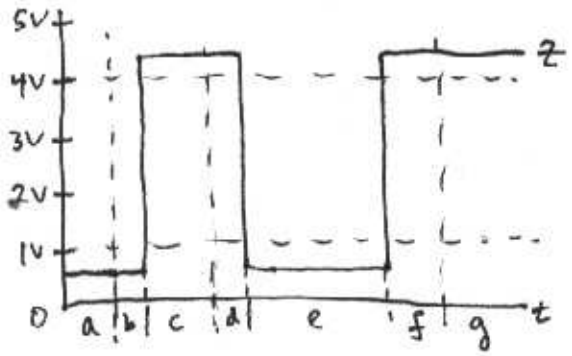


Since we know that $V_L = 1V$ and $V_H = 4V$ we first realize that all the transitions are valid transitions from logical "0" to logical "1" or vice versa.

LET US DONATE THE TIME SEGMENTS BETWEEN EACH TRANSITION WITH THE LETTERS a→g, as THERE ARE 6 DISTINCT TRANSITIONS. THEN WE CAN WRITE OUT A TABLE OF THE VALUES OF A, B, & C IN EACH SEGMENT AND USE OUR TRUTH TABLE FROM 2(c) TO HELP US FIND OUR OUTPUT WAVEFORM

	A	B	C	Z
a	0	1	0	0
b	1	1	0	0
c	1	1	1	1
d	0	1	1	1
e	0	0	1	0
f	1	0	1	1
g	1	0	0	1

THEREFORE, OUR OUTPUT WAVEFORM LOOKS LIKE THIS:



4. (A&L 5.8, p. 372)

LET US WRITE OUT A TRUTH TABLE FOR A 4-INPUT MAJORITY CIRCUIT.

A0	A1	A2	A3	Z
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	0
0	1	1	0	0
0	1	1	1	1
1	0	0	0	0
1	0	0	1	0
1	0	1	0	0
1	0	1	1	1
1	1	0	0	0
1	1	0	1	1
1	1	1	0	1
1	1	1	1	1

THUS, $Z = (\bar{A0})(A1)(A2)(A3) + (A0)(\bar{A1})(A2)(A3) + (A0)(A1)(\bar{A2})(A3) + (A0)(A1)(A2)(\bar{A3}) + (A0)(A1)(A$

$Z = [(\bar{A0})(A1)(A2)(A3) + (A0)(A1)(A2)(A3)] + [(A0)(\bar{A1})(A2)(A3) + (A0)(A1)(A2)(A3)] + [(A0)(A1)(\bar{A2})(A3) + (A0)(A1)(A2)(A3)] + [(A0)(A1)(A2)(\bar{A3}) + (A0)(A1)(A2)(A$

since we know that $A+B = A+B+A$

NOW, since $(A+\bar{A}) = 1$,

$$Z = (A0)(A1)(A2) + (A0)(A1)(A3) + (A0)(A2)(A3) + (A1)(A2)(A3)$$

TO IMPLEMENT A 3-INPUT MAJORITY CIRCUIT, WE NEED A CIRCUIT THAT WILL OUTPUT Z=1 IF AT LEAST 2 OF THE 3 INPUTS ARE HIGH. BUT IF WE LOOK AT THE BOTTOM HALF OF THE TRUTH TABLE, WE SEE EXACTLY THIS FOR A1, A2, & A3. THUS IF WE **SET A0 = 1**, THEN WE CAN IMPLEMENT A 3-INPUT MAJORITY CIRCUIT, WITH A1, A2, & A3 AS OUR INPUTS.

TO IMPLEMENT A 2-INPUT MAJORITY CIRCUIT, WE ONLY OUTPUT Z=1 FOR BOTH INPUTS ARE HIGH. AGAIN, USING OUR TRUTH TABLE, IF WE **SET A0 = 0** & **SET A1 = 1** AND USE A2 & A3 AS INPUTS, WE IMPLEMENT OUR 2-INPUT MAJORITY CIRCUIT.

5. (A&L 5.14, p. 375)

a) (a) $Z = \overline{1 \cdot \overline{A \cdot \overline{B}}}$

$Z = 0 + (A + \overline{B}) \rightarrow \boxed{Z = A + \overline{B}}$

(b) $Z = \overline{0 \cdot \overline{A \cdot \overline{B}}}$

$Z = 1 + (A + \overline{B}) \rightarrow \boxed{Z = 1}$

(c) $Z = \overline{1 \cdot \overline{A \cdot 1}}$

$Z = 0 + (0 + A) \rightarrow \boxed{Z = A}$

(d) $Z = \overline{0 + \overline{0 + A}}$

$Z = 1 \cdot (1 \cdot A) \rightarrow \boxed{Z = A}$

b) If $X = 1$, then we have part (a) from above, so

FOR $X = 1$, $Z = A + \overline{B}$

If $X = 0$, the we have part (b) from above, so

FOR $X = 0$, $Z = 1$

TO FIGURE OUT WHETHER $X = 0$ or $X = 1$, WE HAVE TO TRY AND FORCE $Z = 0$ IN THE CASE THAT $X = 1$. IF WE THEN FIND THAT $Z = 1$, THEN WE KNOW THAT $X = 0$, OTHERWISE, $X = 1$.

THUS, WE SET

$A = 0$
$B = 1$
$C = 0$ or 1

AND OBSERVE Z. → FOR $Z = 1$, $X = 0$
FOR $Z = 0$, $X = 1$

6. (A&L exercise 6.2(d), p. 426)

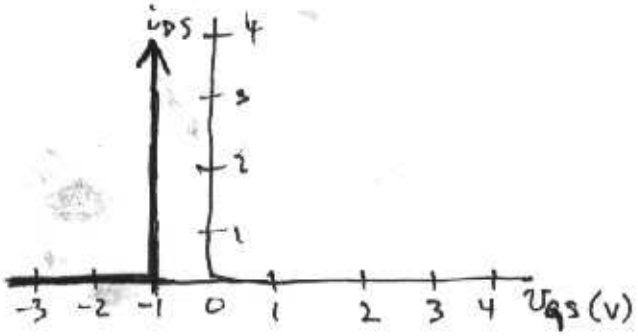
USING OUR KNOWLEDGE OF NMOS, WE JUST FIND THAT

$$\boxed{OUT = \overline{(AB + C)(EN)}}$$

7. (A&L 6.2, p. 429)

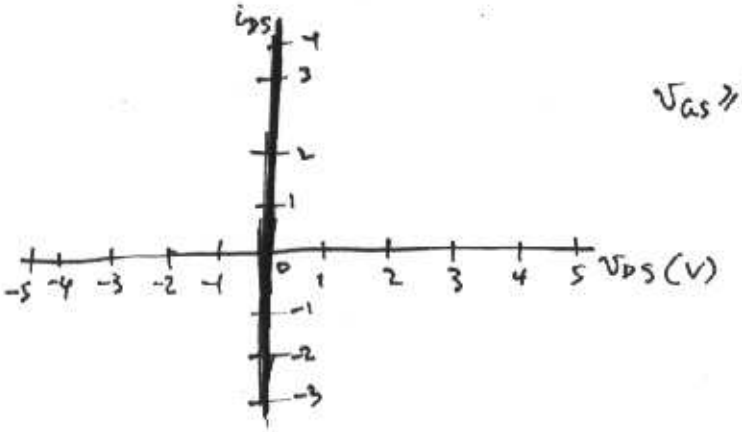
(a) We know that for $v_{GS} < -1\,V$, $i_{DS} = 0$ (open circuit)

and for $v_{GS} \geq -1\,V$, $i_{DS} = \infty$ (short circuit)

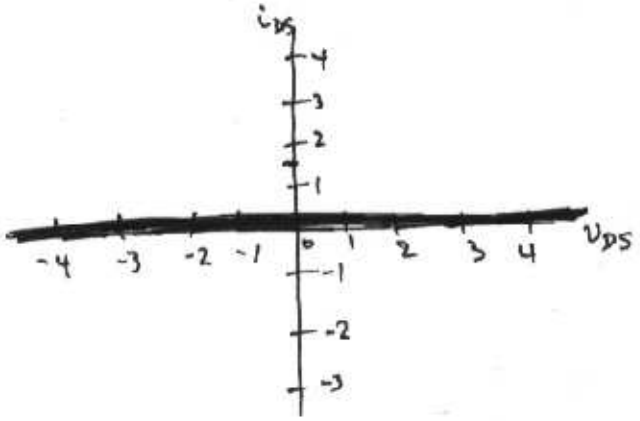


(b) For $v_{GS} \geq V_T$, the MOSFET is a short.

This means $v_{DS} = 0$ for all values i_{DS}



$v_{GS} \geq V_T$

For $v_{GS} < V_T$, the MOSFET is an open.

This means $i_{DS} = 0$ for all values v_{DS}