Massachusetts Institute of Technology
Department of Electrical Engineering and Computer Science

6.002 – Electronic Circuits

Lab #2: MOSFET Inverting Amplifiers & First-Order Circuits
Fall 2002

Introduction

This lab examines the behavior of an inverting MOSFET amplifier. It begins by examining the static input-output relation of the amplifier, and concludes by examining the dynamic behavior of the same amplifier when used as a digital logic inverter. You should complete the pre-lab exercises in your lab notebook before coming to lab. Then, carry out the in-lab exercises on your assigned lab day between October 28 and November 1. After completing the in-lab exercises, have a TA or LA check your work and sign your lab notebook. Finally, complete the post-lab exercises in your lab notebook. You may turn in your lab notebook for grading at that time, or keep it until the end of Lab #4.

Pre-Lab Exercises

(2-1) Consider the inverting MOSFET amplifier shown in Figure 1. Using the SCS MOSFET model, determine $v_{\rm OUT}$ as a function of $v_{\rm IN}$ for $0 \leq v_{\rm IN} \leq v_{\rm OUT} + v_{\rm T}$. Also, sketch and clearly label $v_{\rm OUT}$ as a function of $v_{\rm IN}$ over the same range.

(2-2) Determine the small-signal gain of the MOSFET amplifier shown in Figure 1 assuming that its MOSFET is biased into saturated operation.

(2-3) Consider the network shown in Figure 2. First, assume that $v_{\rm OUT} = 0$ at $t = 0$. Then, determine $v_{\rm OUT}(t)$ for $t \geq 0$ given that $v_{\rm IN}$ steps from 0 V to $V_{\rm I}$ at $t = 0$. Second, assume that $v_{\rm OUT} = \frac{R_2}{R_1+R_2}V_{\rm I}$ at $t = 0$. Then, determine $v_{\rm OUT}(t)$ for $t \geq 0$ given that $v_{\rm IN}$ steps from $V_{\rm I}$ to 0 V at $t = 0$.

(2-4) For both transients determined in Pre-Lab Exercise 2-3, determine the time at which $v_{\rm OUT}$ reaches a given $V_{\rm T}$ where $0 < V_{\rm T} < \frac{R_2}{R_1+R_2}V_{\rm I}$.

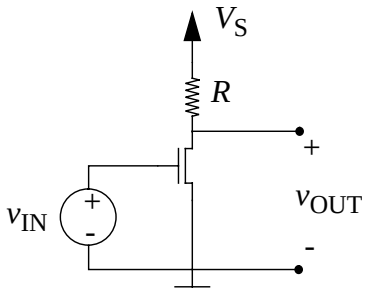

Figure 1: inverting MOSFET amplifier for Pre-Lab Exercises 2-1 and 2-2.

In-Lab Exercises

As part of the in-lab exercises, you will measure the threshold voltage and gate-to-source capacitance of a MOSFET. These parameters will be used to interpret the results of other in-lab exercises. Therefore, use the same MOSFET in every in-lab exercise described below.

(2-1) This exercise measures the static input-output relation of the MOSFET amplifier shown in Figure 1. To begin, construct the amplifier as shown in Figure 3, and connect the signal generator and oscilloscope as shown. Next, set the signal generator to produce a 1-kHz sine wave with a peak-to-peak amplitude of 3 V and an offset of 1.5 V. Thus, the signal generator will produce a biased sine wave between 0 V and 3 V. Set the oscilloscope to operate in its X-Y mode with an X-axis (Channel #1) sensitivity of 500 mV per division and a Y-axis (Channel #2) sensitivity of 1 V per division. You should now see the input-output relation displayed on the oscilloscope. Finally, compare the displayed relation to that sketched in Pre-Lab Exercise 2-1.

Record the following data. First, record the value of $v_{\rm IN}$ above which $v_{\rm OUT}$ just begins to fall. This is the threshold voltage $v_{\rm T}$ of the MOSFET; see the sketch from Pre-Lab Exercise 2-1. Second, record the values of $v_{\rm IN}$ which correspond to $v_{\rm OUT}$ values of 5 V, 4 V, 3 V, 2 V and 1 V. Alternatively, you may find it easier and much more accurate to use the signal generator as a programmable $v_{\rm IN}$ source and measure $v_{\rm OUT}$ with a multimeter.

(2-2) This exercise measures the small-signal gain of the amplifier shown in Figure 1 when its output bias voltage is 2 V. To begin, construct Circuit #1 shown in Figure 4. Adjust the potentiometer until $v_{\rm OUT} = 2$ V as measured by the multimeter. Next, connect the signal generator and the oscilloscope as shown in Circuit #2. Set the signal generator to

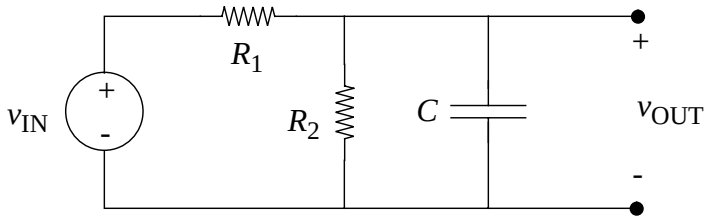

Figure 2: network for Pre-Lab Exercises 2-3 and 2-4.

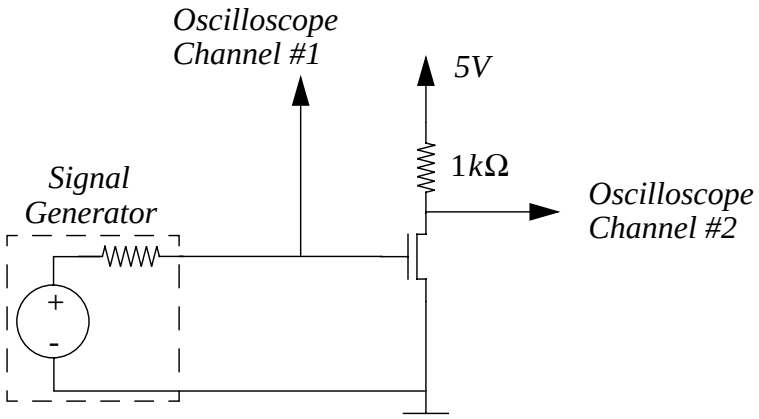

Figure 3: measuring the static input-output relation of the MOSFET amplifier shown in Figure 1.

produce an unbiased 1-kHz sine wave with a peak-to-peak amplitude of 100 mV. Measure the amplitude of both v_{in} and v_{out}, which are the sinusoidal components of v_{IN} and v_{OUT}, respectively; use AC coupling in Channel #1 of the oscilloscope to accurately measure v_{in}. The ratio of the amplitudes is the small-signal gain. Finally, adjust the input bias with the potentiometer, and observe the variation in v_{OUT}.

(2-3) This exercise measures the gate-to-source capacitance C_{GS} of the MOSFET. First, construct the circuit shown in Figure 5. Set the signal generator to produce a 20-kHz square wave with an amplitude of 5 V peak-to-peak and an offset of 2.5 V. The oscilloscope should display a first-order step response. Measure the time constant of that step response. Second, remove the MOSFET from the circuit, and measure the time constant again.

(2-4) This exercise measures the delay of the MOSFET amplifier shown in Figure 1 when it is used as a digital logic inverter. Construct the circuit shown in Figure 6; the 100-kΩ resistor in this circuit models the Thevenin resistance of whatever drives the inverter. Next, connect the oscilloscope and signal generator as shown. Set the signal generator to produce a 20-kHz square wave with an amplitude of 5 V peak-to-peak and an offset of 2.5 V. Finally, use the oscilloscope to measure the delay from the time at which the signal generator switches high to the time at which the inverter output begins to switch low. Also, measure the delay from the time at which the signal generator switches low to the time at which the inverter output begins to switch high. Since the output of the inverter begins to switch when the MOSFET gate voltage passes by v_{T}, the two delays may not be the same; see Pre-Lab Exercise 2-4.

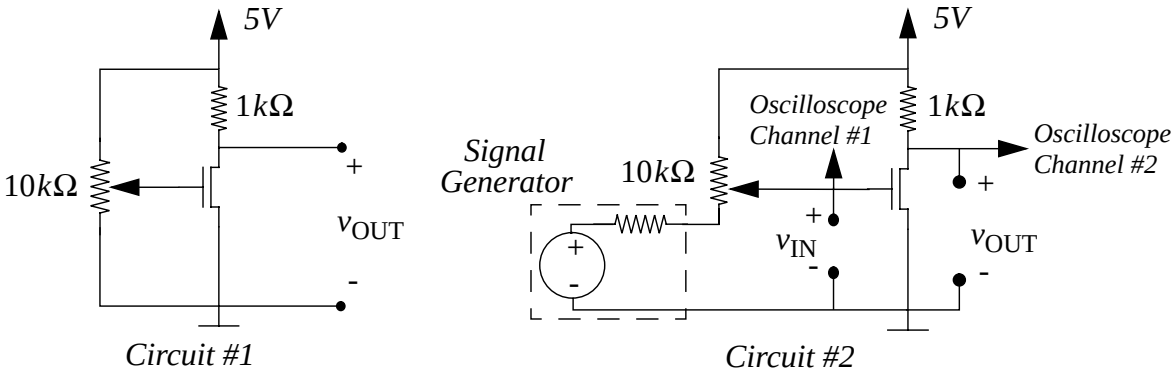

Figure 4: measuring the small-signal gain of the MOSFET amplifier.

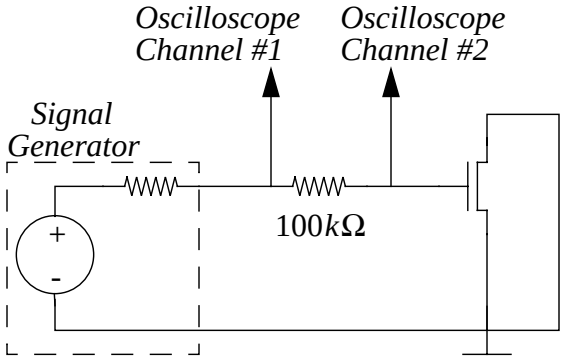

Figure 5: measuring the gate-to-source capacitance of the MOSFET amplifier.

Post-Lab Exercises

(2-1) This exercise examines how well the MOSFET amplifier model developed during Pre-Lab Exercise 2-1 explains the input-output relation measured during In-Lab Exercise 2-1. The model contains four parameters which are required to numerically evaluate the input-output relation: V_S, R, v_T and K. From Figure 3, $V_S = 5$ V and $R = 1$ kΩ. Further, v_T was measured during In-Lab Exercise 2-1. Thus, only K is unknown. Use the value of v_{IN} recorded for $v_{OUT} = 1$ V to determine K. Then, use the numerical parameters and the model to graph v_{OUT} as a function of v_{IN} for $1\text{ V} \leq v_{OUT} \leq 5\text{ V}$. On this graph, also plot the data measured during In-Lab Exercise 2-1. How well does the model explain the data?

(2-2) From the data recorded during In-Lab Exercise 2-2, compute the small-signal gain of the amplifier for $v_{OUT} = 2$ V. From the data recorded during In-Lab Exercise 2-1, again compute the small-signal gain by estimating the slope of the input-output relation at $v_{OUT} = 2$ V. Finally, compute the small-signal gain from the analysis of Pre-Lab Exercise 2-2 using the parameters determined during Post-Lab Exercise 2-1. Do the three gains match well?

(2-3) Figure 2 models the circuit shown in Figure 5: R_1 models the generator source resistance and the 100-kΩ resistor; R_2 models the oscilloscope input resistance; and C models C_{GS} in parallel with the oscilloscope input capacitance and a parasitic wiring capacitance. Assume that the oscilloscope input resistance and capacitance are 100 MΩ and 10 pF, respectively. Combine the analysis of Pre-Lab Exercise 2-3 and the time constants measured during In-Lab Exercise 2-3 to determine C_{GS} and the wiring capacitance.

(2-4) With $V_I = 5$ V and $V_T = v_T$, the analysis of Pre-Lab Exercise 2-4 models the delays measured during In-Lab Exercise 2-4. Using the parameters computed during Post-Lab Exercise 2-3, predict the delays and compare the predictions to the measurements. Note that the oscilloscope with its input resistance and capacitance were not connected to the MOSFET gate when the delays were measured; see Figure 6.

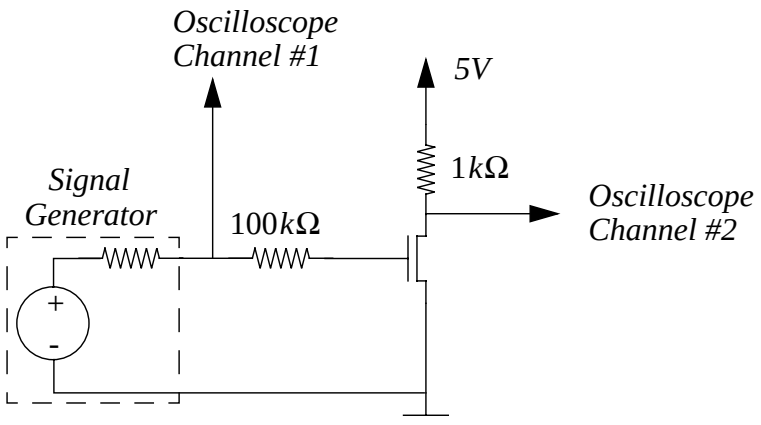

Figure 6: measuring the delay of the MOSFET amplifier shown in Figure 1 when it is used as a digital logic gate.