MASSACHUSETTS INSTITUTE OF TECHNOLOGY
Department of Electrical Engineering and Computer Science

6.002 – Electronic Circuits
Fall 2002

Problem Set 4

Issued: September 25, 2002 **Due: October 2, 2002**

Reading Assignment:

- A&L Section 2.6 for Thursday, September 26.
- A&L Chapter 7 for Tuesday, October 1.

Problem 4.1:

(A) Implement the logical function $A\bar{B} + \bar{A}B$ using

(i) only NOT and NAND gates.
(ii) only NOT and NOR gates.

(B) Determine a circuit implementation for the gate configurations found in part (A) using MOSFETs and pull-up resistors. You do not need to determine element values.

Problem 4.2: Design a circuit to implement the Boolean expressions given below using MOSFETs and pull-up resistors. You do not need to determine element values.

(A) $A + \bar{B} + \bar{C}$

(B) $AB\bar{C}$

(C) $AB + C$

In each case the circuit can be implemented by at most four MOSFETs and two resistors. Try to use the minimum number of components.

Problem 4.3: The NOR gate shown in Figure 1 is a member of a family of logic gates that operates with the following voltage thresholds:

$$V_{OL} = 0.5V, \quad V_{IL} = 1.5V, \quad V_{IH} = 4V, \quad V_{OH} = 4.5V$$

Since the voltage V_G is more than one threshold voltage above V_S, the pull-up MOSFET, like the MOSFETs used to implement the NOR gate, operates in the S-R regime with $R_{on} = R_n \frac{L}{W}$ where $R_n = 1k\Omega$ and L and W are the lateral dimensions of the MOSFET channel. Assume that the area of each MOSFET is given by $L \times W$, that the dimensions of each MOSFET can be independently specified, and that the minimum dimension of any MOSFET channel is $0.5\mu m$.

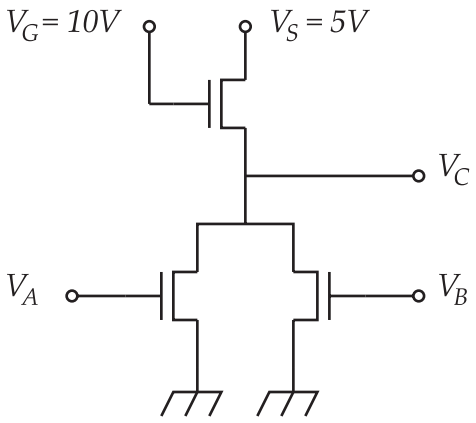

Figure 1: Circuit for Problem 4.3

(A) A random batch of MOSFETs has variability in their threshold voltage values. What is the widest range of V_T values that would be acceptable in implementing the above gate?

(B) Determine the minimum total MOSFET area required to implement the NOR gate.

(C) Assume that the NOR gate operates for equal time in each of its four input states. What is the total average power dissipated by the MOSFETs?

Problem 4.4: Figure 2 shows a simplified model of a single-stage amplifier that incorporates a bipolar junction transistor (BJT). Typically the parameter $\beta \approx 100$. Although we will not study BJT's in 6.002, this problem illustrates that the tools we are developing are sufficient to analyze and design circuits containing them, given appropriate models.

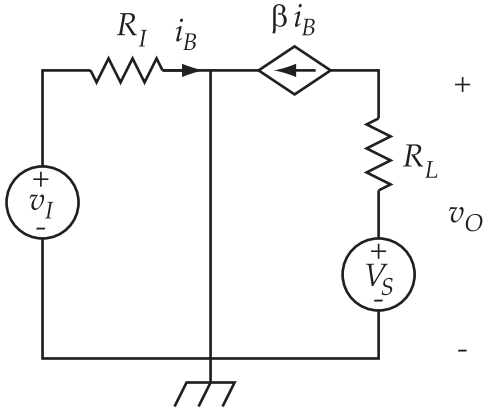

Figure 2: Circuit for Problem 4.4

(A) Determine the relationship between v_O and v_I.

(B) Graph this relationship and indicate a range of validity if the model holds only for $i_B > 0$ and $v_O > 0$. In this range, what is the small-signal gain dv_O/dv_I?

Problem 4.5:

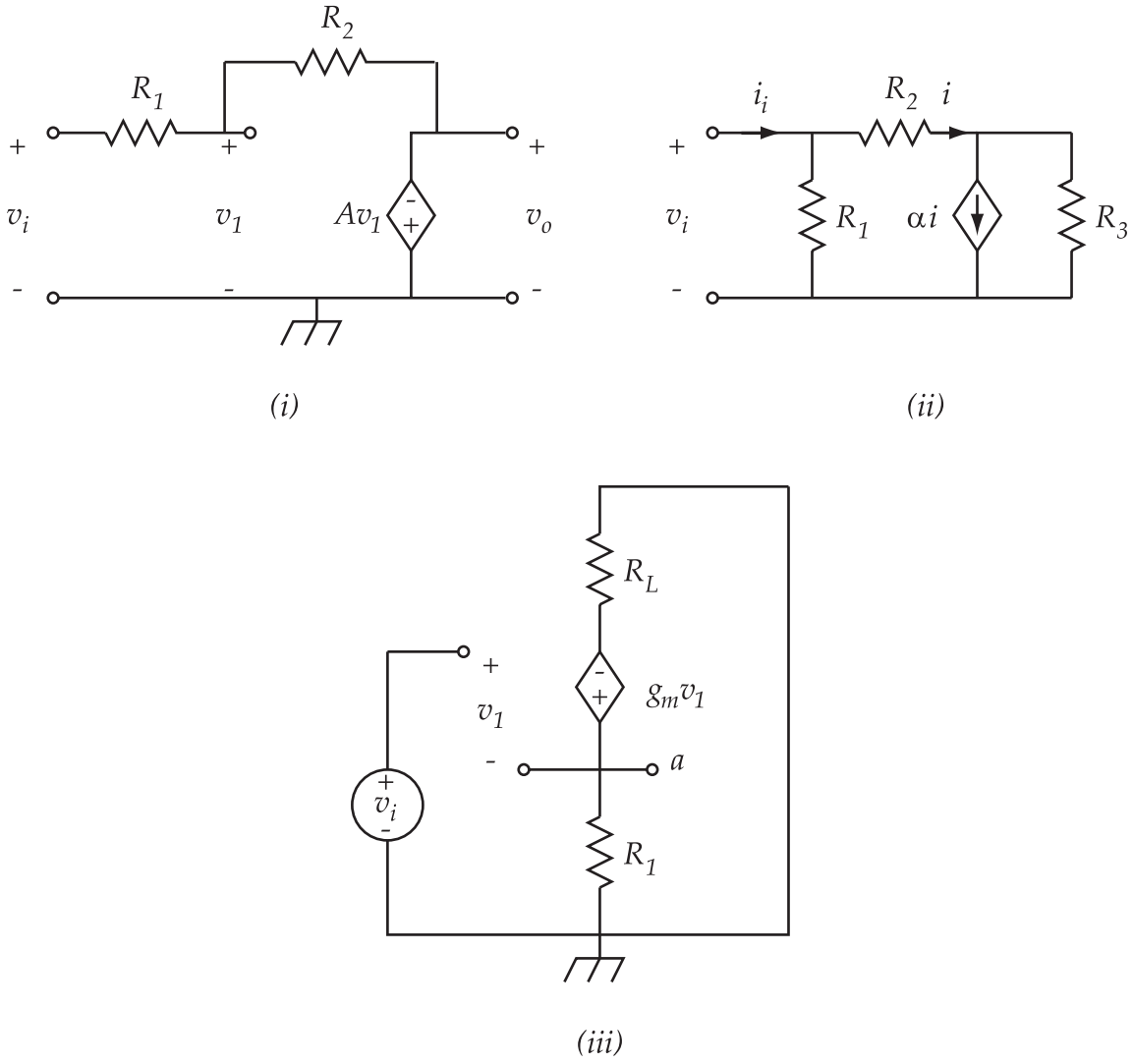

Figure 3: Circuits for Problem 4.5

(A) Compute the gain $A = v_o/v_i$ in Figure 3(i).

(B) Compute the Thévenin resistance $R_{Th} = v_i/i_i$ in Figure 3(ii).

(C) Determine the Thévenin equivalent circuit at the terminal pair formed by a and the ground node in Figure 3(iii).