Massachusetts Institute of Technology
Department of Electrical Engineering and Computer Science

6.002 – Electronic Circuits
Fall 2002

Homework #4 Solutions

Problem 4.1 Answer:

(A) The answers to these problems make use of DeMorgan's theorem. Information on this can be found in the course notes on pages ???-???. DeMorgan's theorem states that the following expressions are equivalent:

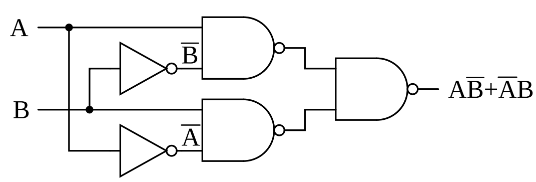
$$A + B = \overline{\overline{A}\;\overline{B}}$$
$$AB = \overline{\overline{A} + \overline{B}}$$

Verify this for yourself by writing out the truth tables for the above expressions.

(i) Using DeMorgan's theorem to turn the OR operation into a NAND, this expression becomes

$$\overline{(\overline{A\overline{B}})(\overline{\overline{A}B})}$$

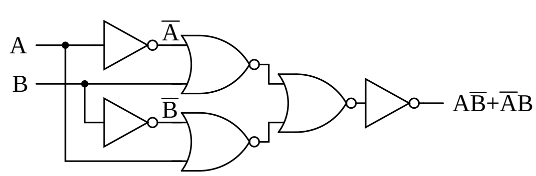
This is implemented in only NOT and NAND gates as



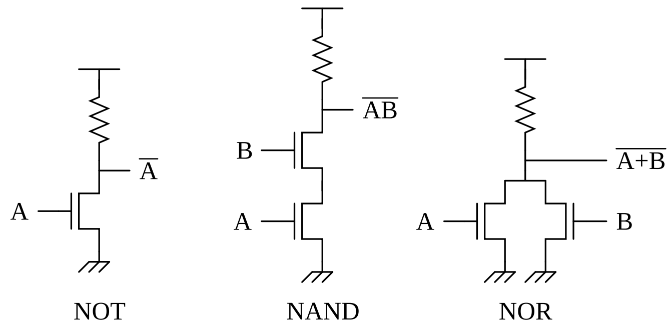
(ii) Using DeMorgan's theorem to turn the AND operations into NORs, this expression becomes

$$\overline{\overline{A} + B} + \overline{A + \overline{B}}$$

This is implemented in only NOT and NOR gates as

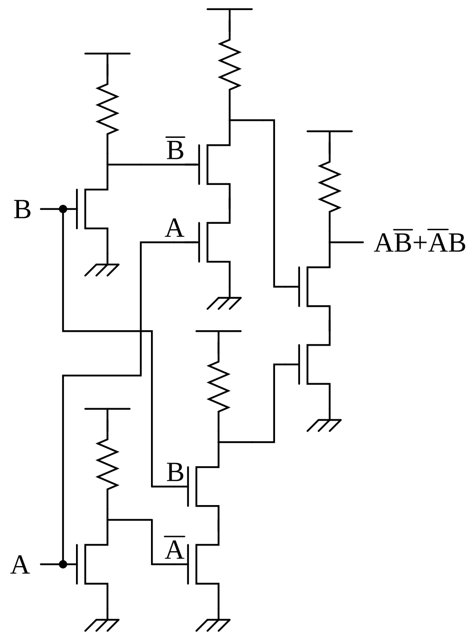


(B) We know that NOT, NAND, and NOR gates implemented with n-channel MOSFETs and pull-up resistors look like the following.

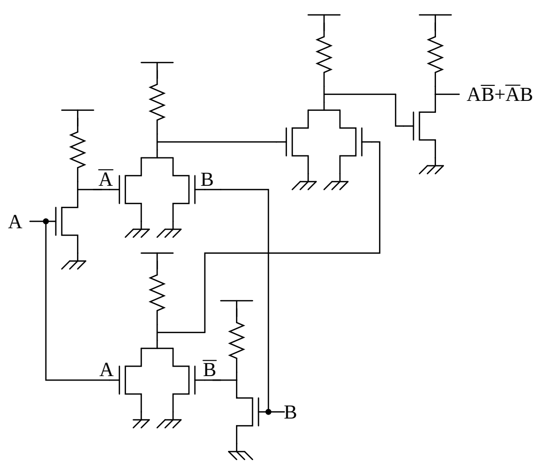


We can use these building blocks and connect them according to the diagrams in Part (A) to find the following implementations.

(i) The circuit implemented with NAND and NOT gates is



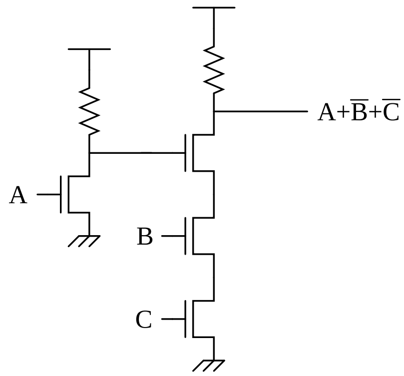
(ii) The circuit implemented with NOR and NOT gates is



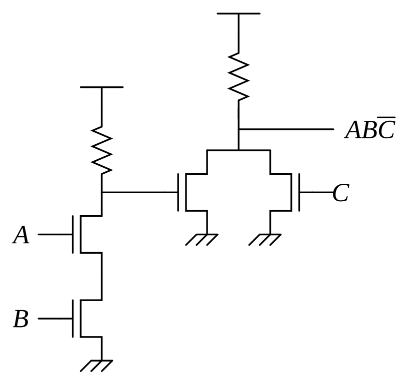
Problem 4.2 Answer:

Again, we can use DeMorgan's Theorem to simplify these expressions so they can be implemented with fewer transistors and pull-up resistors.

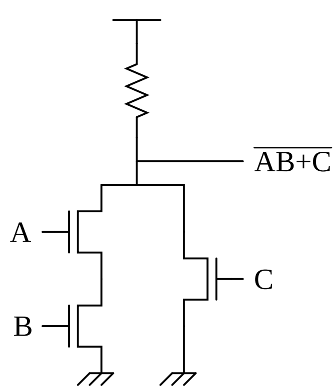
(A) $A + \overline{B} + \overline{C}$ can be transformed into $\overline{\overline{A}BC}$ by changing the ORs to NANDs. This can be implemented with one inverter and one three-input NAND gate, as shown below.



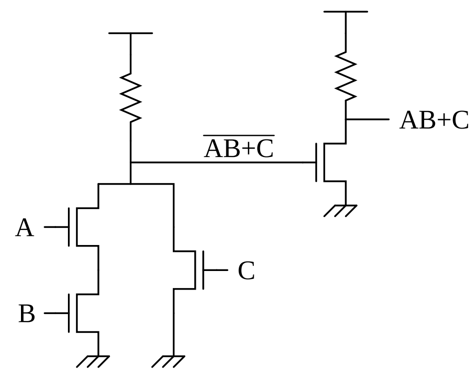
(B) Transform the AND in $(AB)(\overline{C})$ into a NOR to get $\overline{\overline{AB} + C}$. This can be implemented using one two-input NAND gate, and one 2-input NOR gate.



(C) This expression is a little more challenging to synthesize with no more than four MOSFETs and two resistors. Notice that the output should be high when either AB or C is high. We can synthesize a circuit which has the opposite behavior, that is the output is low when AB or C is high. That circuit is



Add an inverter to it's output, and we get the desired logic function. This circuit is



Problem 4.3 Answer:

(A) Neither of the input MOSFETs can turn on (and bring the output low) unless $V_{A,B} > V_{IL}$. This means that $V_T < V_{IL}$. We also know that the MOSFETs must turn on for $V_{A,B} > V_{IH}$, which implies that $V_T < V_{IH}$. The acceptable range of values for V_T is then

$$1.5\text{V} < V_T < 4\text{V}$$

(B) The R_{on} resistances of the three MOSFETs determine the output voltage V_C. The two restrictions on V_C are

(i) $V_C > V_{OH}$ when the output should be high

(ii) $V_C < V_{OL}$ when the output should be low

Restriction (i) is satisfied for any R_{on} of the three MOSFETs when V_A and V_B are low. V_C will be equal to V_S independent of the R_{on} of the pull-up MOSFET because no current flows through it. Restriction (ii) on V_C will determine the R_{on} of the devices. The highest value of V_C when the output should be low is produced when only one of the two input MOSFETs is on. We can write V_C in terms of the R_{on} values for the MOSFETs (with only one input high) as:

$$V_C = V_S \frac{1\text{k}\Omega \frac{L_i}{W_i}}{1\text{k}\Omega \frac{L_i}{W_i} + 1\text{k}\Omega \frac{L_p}{W_p}} = V_S \frac{R_I}{R_I + R_P} < V_{OL}$$

where L_I, W_I and R_I are the length, width and resistance of one of the input MOSFETs, respectively and L_P, W_P and R_P are the length, width and resistance of the pullup MOSFET.

Both input MOSFETs must be the same size. If B were larger than A, for example, there exists a smaller MOSFET (namely A) that would still satisfy the static discipline, so B could be made smaller. Both MOSFETs will be the "optimum" value.

Using the V_{OL} restriction above, we can rearrange $V_S \frac{R_I}{R_I + R_P} < V_{OL}$ and substitute in values for V_S and V_{OL} to find

$$9R_I < R_P$$

If we choose R_P greater than $9R_I$, though, there is a resistor of smaller value (and therefore smaller area) that would also satisfy the restriction. Minimizing the area of the transistors requires that $R_P = 9R_I$.

Look again at the V_{OL} restriction. Ideally, we want R_P to be large, and R_I to be small. This implies that $W_P = L_I = .5\mu m$. If this were not the case, we could achieve the same resistances for R_P or R_O with proportionally smaller L's and W's, which means the total area would be smaller.

Armed with this knowledge, we can minimize the area $A = L_P W_P + 2L_I W_I$.

Substitute in $W_P = L_I = .5\mu m$ into the area equation and the $R_P = 9R_I$ equation to get the following (note that all dimensions are in μm, units have been omitted):

$$\begin{aligned} A &= .5L_P + W_I \\ \frac{L_P}{.5} &= 9\frac{.5}{W_I} \end{aligned}$$

Solve the second equation for L_P and substitute it into the area equation to get

$$A = \frac{1.125}{W_I} + W_I$$

Take the derivative of this and set it equal to zero to find the W_I that minimizes the area of the gate.

$$\begin{aligned} 0 &= \frac{d}{dW_I}\left(\frac{1.125}{W_I} + W_I\right) \\ 1 &= \frac{1.125}{W_I^2} \\ \frac{3}{2\sqrt{2}} &= W_I \approx 1.0607\mu m \end{aligned}$$

We can use this to find

$$L_P = \frac{9}{4W_I} = \frac{3}{\sqrt{2}} \approx 2.1213\mu m$$

The minimal total gate area is then

$$.5\frac{3}{\sqrt{2}} + 2 * .5\frac{3}{2\sqrt{2}} = \frac{3}{\sqrt{2}} = 2.1213(\mu m)^2$$

(C) Recall that the power dissipated by resistive devices is given by $\frac{V^2}{R}$. The resistance between V_S and the ground node for each of the four input states is summarized in the table below. Note that the R_P is $3\sqrt{2}$k$\Omega \approx 4.2426$kΩ and the resistance of each of the pull-down resistors R_I is $\frac{\sqrt{2}}{3}$k$\Omega \approx .4714$kΩ from Part (B).

A	B	R
0	0	∞
0	1	$(3\sqrt{2} + \frac{\sqrt{2}}{3})k\Omega$
1	0	$(3\sqrt{2} + \frac{\sqrt{2}}{3})k\Omega$
1	1	$(3\sqrt{2} + \frac{\sqrt{2}}{6})k\Omega$

The total average power dissipated by the gate is the average of the power dissipated in each state (because the gate is operated in each state for equal time). This is

$$\frac{1}{4}\left(\frac{25}{\infty\Omega}\text{W}+\frac{25}{(3\sqrt{2}+\frac{\sqrt{2}}{3})\text{k}\Omega}\text{W}+\frac{25}{(3\sqrt{2}+\frac{\sqrt{2}}{3})\text{k}\Omega}\text{W}+\frac{25}{(3\sqrt{2}+\frac{\sqrt{2}}{6})\text{k}\Omega}\text{W}\right)\approx 4.0473\text{mW}$$

Problem 4.4 Answer:

(A) The node between R_I and the dependent current source is at the same potential as the ground node (they are connected!). This allows us to write out an equation for i_B directly as

$$i_B=\frac{v_I}{R_I}$$

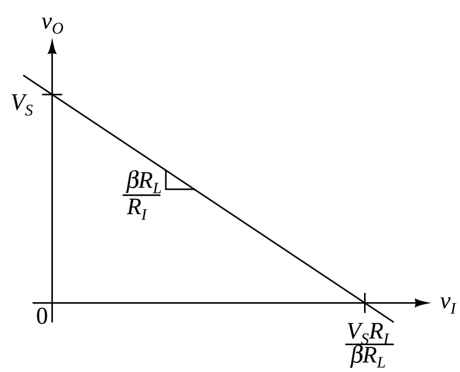
With this information, we can express v_O as the sum of the voltage V_S and the voltage drop across the resistor R_L. This gives

$$v_O=V_S-R_L\beta i_B$$

Substituting in the equation for i_B above yields an expression for v_O in terms of v_I.

$$v_O=V_S-R_L\beta\frac{v_I}{R_I}$$

(B) The equation found for v_O in Part (A) has intercepts at $v_O=V_S$ and $v_I=V_S\frac{R_I}{\beta R_L}$. For $i_B>0$, $v_I>0$. The other restriction on valid operating ranges (given in the problem statement) is that $v_O>0$. These two restrictions limit the range of validity of this model to the first quadrant, graphed below.



The small signal gain $\frac{dv_o}{dv_i}$ is found by differentiating the expression for v_O above.

$$\frac{dv_o}{dv_i}=-\frac{R_L\beta}{R_I}$$

Problem 4.5 Answer:

(A) To compute the gain of the circuit A_v, we need to find an expression for v_o in terms of v_i, and then divide both sides by v_i to find $A_v = \frac{v_o}{v_i}$.

The current flowing into the resistor R_1 (from the v_i side) is equal to the current flowing out of R_2 into the dependent voltage source. This allows us to write

$$\frac{v_i - v_1}{R_1} = \frac{v_1 - v_o}{R_2}$$

We also know that v_o is just

$$v_o = -Av_1$$

Substitute the second equation into the first for v_1 and solve for $\frac{v_o}{v_i}$.

$$\begin{aligned} \frac{v_i - v_1}{R_1} &= \frac{v_1 - v_o}{R_2} = v_1 \frac{1+A}{R_2} \\ \frac{v_i}{R_1} &= v_1 \left(\frac{1+A}{R_2} + \frac{1}{R_1} \right) \\ \frac{v_i}{R_1} &= -\frac{v_o}{A} \left(\frac{1+A}{R_2} + \frac{1}{R_1} \right) \\ \frac{v_o}{v_i} &= -\frac{AR_2}{R_1(1+A) + R_2} \end{aligned}$$

(B) Let e_1 denote the potential of the node in the top right-hand side of the circuit (where R_2 meets R_3). If i flows into this node, and αi flows out through the dependent current source, we know that $(1-\alpha)i$ must flow out of the node through R_3. The node voltage e_1 is given by

$$e_1 = R_3(1-\alpha)i$$

The current i can be expressed as

$$\begin{aligned} i &= \frac{v_i - e_1}{R_2} = \frac{v_i - R_3(1-\alpha)i}{R_2} \\ i &= \frac{v_i}{R_2 + R_3(1-\alpha)} \end{aligned}$$

Combine this with KCL at the input node:

$$i_i = \frac{v_i}{R_1} + i$$

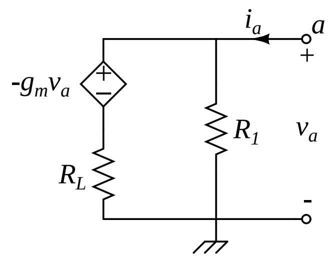
to find that

$$i_i = v_i \left(\frac{1}{R_1} + \frac{1}{R_2 + R_3(1-\alpha)} \right)$$

Solve this equation for $\frac{v_i}{i_i}$ to find R_{Th}. This yields

$$R_{Th} = \frac{1}{\frac{1}{R_1} + \frac{1}{R_2 + R_3(1-\alpha)}} = \frac{R_1(R_2 + R_3(1-\alpha))}{R_1 + R_2 + R_3(1-\alpha)}$$

(C) First find R_{Th}. All independent sources are set to zero, which means that v_1 is going to be equal to $-v_a$ where v_a is the voltage at the terminal a. For clarity, redraw the circuit as shown below, and define i_a as the test current into the terminal a.



The Thévenin resistance is $R_{Th} = \frac{v_a}{i_a}$. Write KCL at the node a to obtain

$$\frac{v_a}{R_1} + \frac{v_a + g_m v_a}{R_L} = i_a$$

Solve for $\frac{v_a}{i_a}$ to find

$$R_{Th} = \frac{1}{\frac{1}{R_1} + \frac{1+g_m}{R_L}} = \frac{R_1 R_L}{R_1(1+g_m) + R_L}$$

Next we need to find the Thévenin voltage at terminal a. The resistors R_1 and R_L form a voltage divider with the dependent voltage source. We can write

$$v_a = g_m v_1 \frac{R_1}{R_1 + R_L}$$

Writing KVL around the simple loop on the left side of the circuit gives

$$v_1 = v_i - v_a$$

Substitute this equation into the first for v_1 to find

$$v_a = \frac{g_m R_1}{R_1 + R_L}(v_i - v_a)$$

Solve this to find an expression for v_a to get

$$V_{Th} = v_a = v_i \frac{g_m R_1}{g_m R_L + R_1 + R_L}$$