MASSACHUSETTS INSTITUTE OF TECHNOLOGY
Department of Electrical Engineering and Computer Science

6.002 – Electronic Circuits
Fall 2002

Problem Set 6

Issued: October 9, 2002 **Due: October 16, 2002**

Reading Assignment:

- A&L Chapters 9 and 10 for Thursday, October 10.

Problem 6.1: In this problem, we will examine the behavior of the two stage MOSFET amplifier shown in Figures 1(a). A simplified model of the MOSFET characteristics will be used, namely one in which the characteristics in the triode region $v_{DS} < v_{GS} - V_T$ are all compressed to the single i_{DS}-v_{DS} relation $i_{DS} = \frac{K}{2} v_{DS}^2$. The MOSFET characteristics with this approximation are illustrated in Figure 1(b). In the saturation region, the characteristics are given by the usual square-law relation $i_{DS} = \frac{K}{2}(v_{GS} - V_T)^2$ where $K = 2mA/V^2$ and $V_T = 2V$. *Note: In working this problem use the numerical values of the circuit parameters.*

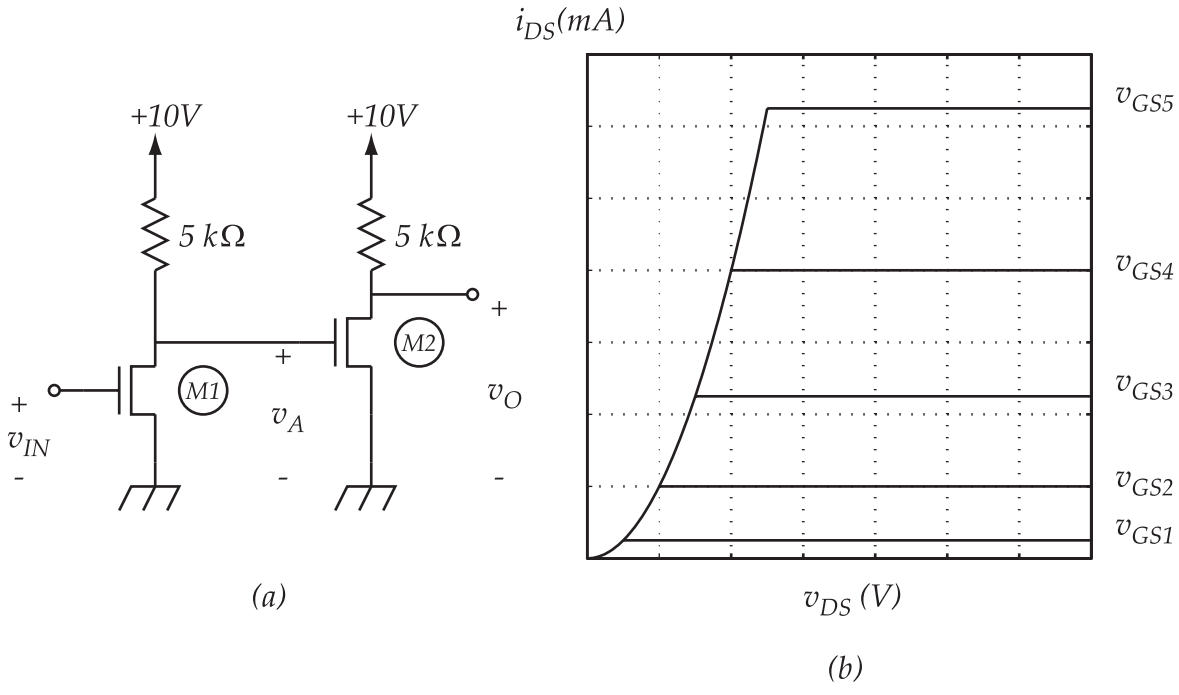

Figure 1: Circuit and characteristic for Problem 6.1

(A) Determine v_A as a function of v_{IN} and provide a labeled sketch of this relationship. Indicate on your sketch the values of v_A and v_{IN} where $M1$ transitions from cutoff to saturation and from saturation to the triode region. *The result of Problem 5.1 for the amplifier shown in Figure 3a should be helpful in answering this part.*

(B) Repeat part (A) for the relationship of v_O vs. v_A. Again, sketch v_O vs. v_A indicating the values of v_O and v_A at the two transition points.

(C) For what range of v_A will *both* $M1$ and $M2$ operate in the saturation region? What range of v_{IN} does this correspond to?

(D) Determine an expression for v_O vs. v_{IN} valid for the input voltage range found in (C).

In parts (E) and (F), let $v_{IN} = 3.2V + v_i$ where v_i is a small-signal.

(E) Use the expression found in (D) to calculate the gain of this amplifier v_o/v_i.

(F) Draw the small-signal equivalent circuit for the amplifier at the operating point determined by $V_{IN} = 3.2V$. Solve this circuit to find the gain v_o/v_i and compare with the result obtained in part (E).

Problem 6.2: Figure 2 depicts the amplifier that was the subject of Problem 5.2. Recall that $M1$ and $M2$ were identical with $K = 1mA/V^2$ and $V_T = 2V$, and that R was chosen so that $I_C = 2mA$ when $v_I = 0$. In this case the bias condition for $M1$ and $M2$ is $I_A = I_B = 1mA$. In this

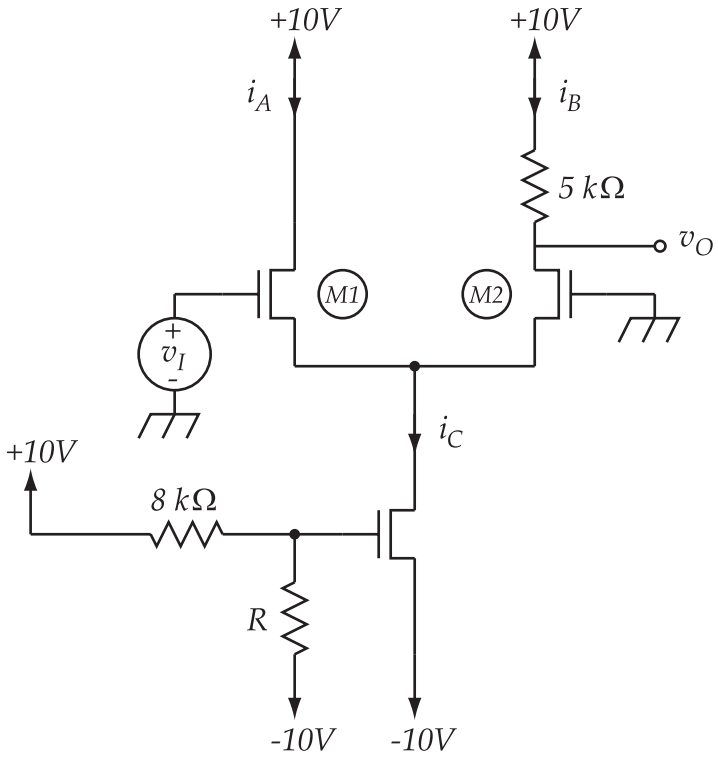

Figure 2: Circuit for Problem 6.2

problem, $v_I = v_i$, a small-signal input, and we are interested in determining the gain v_o/v_i where

v_o is the small-signal component of the output voltage v_O. Although you have already solved this problem in PS5, we will take a different tack by using the small-signal equivalent circuit to get the same result.

(A) Draw the small-signal circuit appropriate for this amplifier. Specify all element values.

(B) Solve the circuit drawn in part (A) to determine v_o/v_i.

(C) Now suppose $v_I = v_i = 0$ but a small-signal input v_i' is inserted between the gate of $M2$ and ground. Determine v_o/v_i'.

(D) Finally suppose inputs v_i and v_i' are applied simultaneously to the gates of $M1$ and $M2$, respectively. What would v_o be? Explain why this configuration is referred to as a "difference amplifier".

Problem 6.3: Find the equivalent capacitance of the all-capacitor network, and the equivalent inductance of the all-inductor network shown in Figure 3.

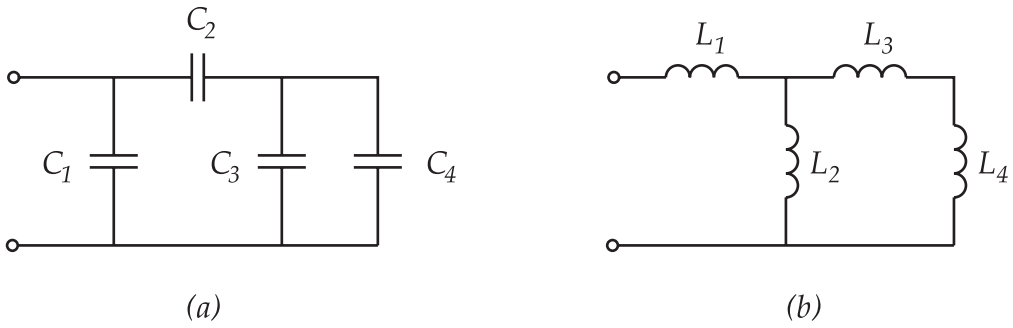

Figure 3: Networks for Problem 6.3

Problem 6.4: The sources in the networks shown in Figure 4 have step-function time dependence, i.e.,

$$i_S(t) = \begin{cases} I_S & t > 0 \\ 0 & t < 0 \end{cases} \qquad v_1(t) = \begin{cases} V_1 & t > 0 \\ 0 & t < 0 \end{cases} \qquad v_2(t) = \begin{cases} V_2 & t > 0 \\ 0 & t < 0 \end{cases}$$

The networks have zero state for $t < 0$.

(A) Determine $v(0+)$ and $v(\infty)$, and $i(0+)$ and $i(\infty)$.

(B) Determine the time constants for these networks.

(C) Using the results of (A) and (B) construct $v(t)$ and $i(t)$ for $t > 0$.

As part (C) is intended to show, it is not necessary to derive and solve the differential equations for $v(t)$ and $i(t)$ in order to determine their behavior for $t > 0$ in this special case of step excitations.

(D) By using the method followed in parts (A)-(C), determine the current i in Figure 4(b) in the

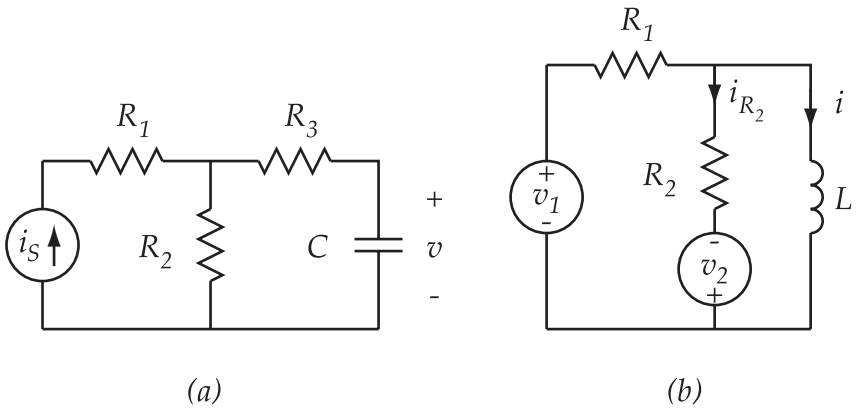

Figure 4: Networks for Problem 6.4

case where

$$v_1(t) = \begin{cases} V_1 & t > 0 \\ 0 & t < 0 \end{cases}$$

and $v_2(t) = V_2$ (constant) for $-\infty < t < \infty$. Assume $i(-\infty) = 0$.

(E) For the sources in part (D), determine the current i_{R_2} for $t > 0$. Notice that the current i_{R_2} can be algebraically related to the sources v_1 and v_2 and the current $i(t)$.

Problem 6.5: Figure 5 shows a buffer circuit and an equivalent circuit for calculating v_1. The capacitor C_{eq} represents the effective gate-to-source capacitance of the second MOSFET. As discussed in lecture and as we'll see quantitatively in this problem, this capacitance is critical to the speed at which the buffer can operate. Assume that v_{IN} is a square wave of period T and amplitude V_S as indicated in Figure 6.

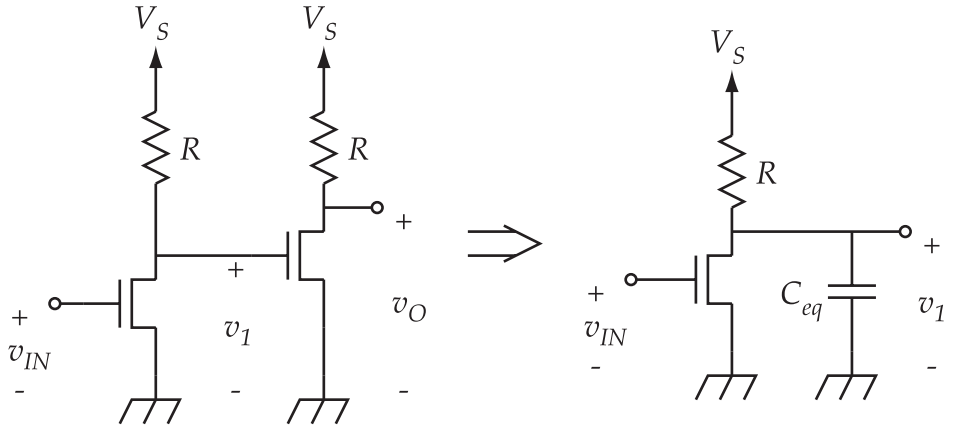

Figure 5: A simple buffer and an equivalent circuit for calculating $v_1(t)$

(A) Assume $RC_{eq} << T/2$ so that the capacitor is fully charged at $t = 0-$. Determine and sketch $v_1(t)$ for $0 < t < T/2$ using the SR model for the MOSFET with $R_{ON} << R$ and $V_S > V_T$.

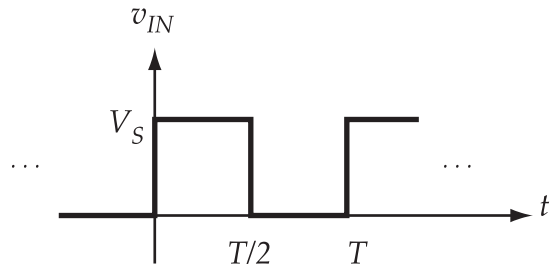

Figure 6: Time function for v_{IN}

(B) What is the time delay between the Lo-Hi transition of the input and the time when v_1 falls below an output low threshold V_{OL}?

(C) Determine and sketch $v_1(t)$ for $T/2 < t < T$, again assuming that $RC_{eq} << T/2$. What is the time delay between the time of a Lo-Hi transition at the input and the time when v_1 rises above an output high threshold V_{OH}?

(D) For fixed C_{eq} and V_S, the switching speed of this buffer can be reduced by reducing the resistance R of the pull-up resistor. What price is paid for increasing the speed by reducing R?