MASSACHUSETTS INSTITUTE OF TECHNOLOGY
Department of Electrical Engineering and Computer Science

6.002 – Electronic Circuits
Fall 2002

Problem Set 8

Issued: October 23, 2002 **Due: October 30, 2002**

Reading Assignment:

- A&L Section 13.1 for Tuesday, October 29.

Problem 8.1: Find the corresponding $v(t)$ in the network shown in Figure 1 for each of the input waveforms $v_S(t)$ illustrated in Figure 2. Assume the network has zero state for $t < 0$.

You may wish to take advantage of the following properties of LCCODE's, where x is the excitation, y the response, and there is no initial state.

$$\text{If} \quad x \rightarrow y \quad \text{then:}$$
$$\int_{-\infty}^{t} x dt' \rightarrow \int_{-\infty}^{t} y dt'$$
$$x(t-T) \rightarrow y(t-T)$$
$$ax \rightarrow ay$$

$$\text{If} \quad x_1 \rightarrow y_1 \quad \text{and} \quad x_2 \rightarrow y_2 \quad \text{then:}$$
$$x_1 + x_2 \rightarrow y_1 + y_2$$

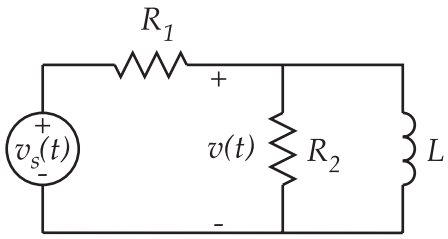

Figure 1: Circuit for Problem 8.1

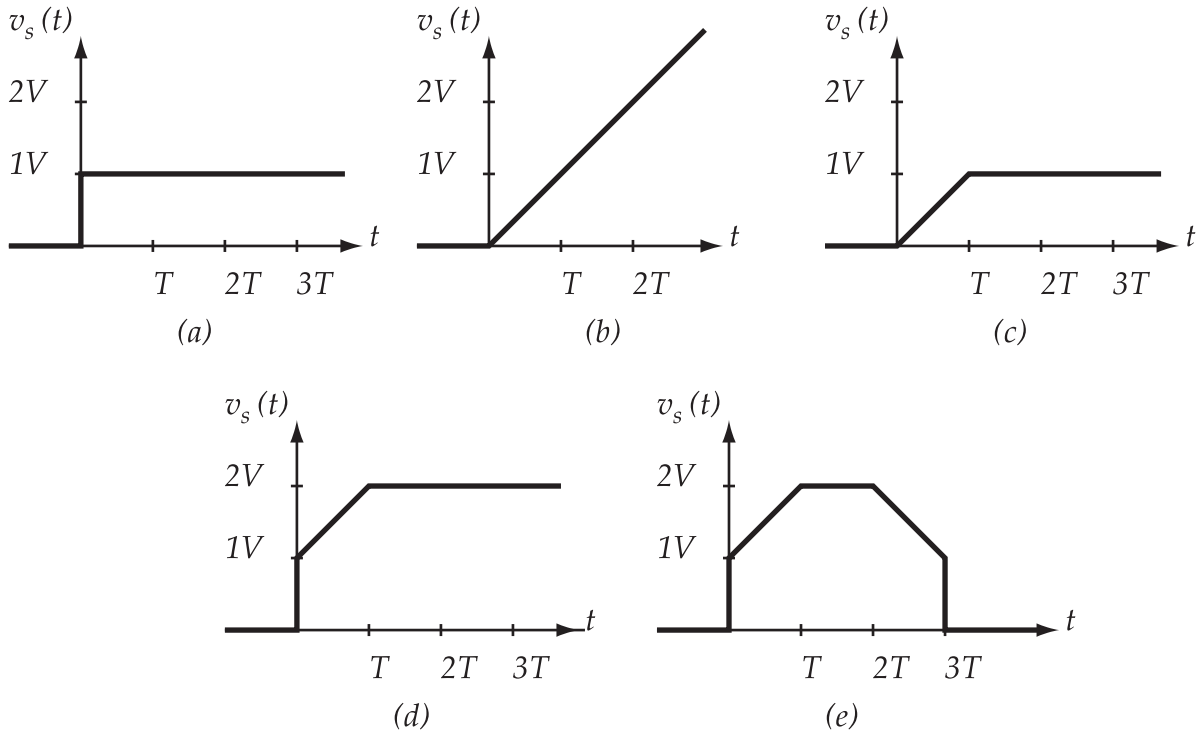

Figure 2: Inputs for Problem 8.1

Problem 8.2: Consider the buffer circuit from Problem 6.5, whose circuit is reproduced in Figure 3.

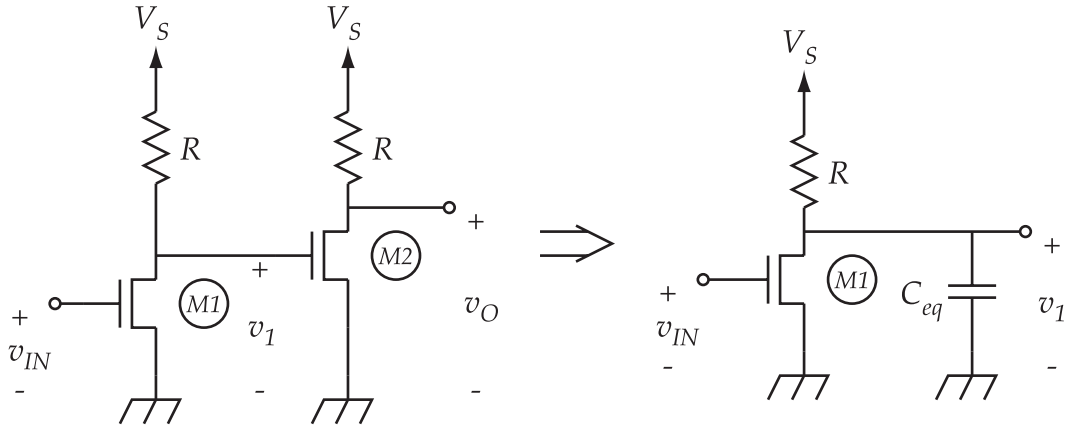

Figure 3: Circuit for Problem 8.2

In Problem 6.5, you solved for the voltage v_1 across the gate-to-source terminals of $M2$ with a square-wave input and where C_{eq} represents the equivalent gate-to-source capacitor of $M2$. The solution for v_1 over the first period is:

$$v_1(t) = \begin{cases} \frac{R_{ON}}{R_{ON}+R}V_S + \frac{R}{R_{ON}+R}V_S e^{-t/\tau_1} & 0 < t < T/2 \\ V_S - \frac{R}{R_{ON}+R}V_S e^{-(t-T/2)/\tau_2} & T/2 < t < T \end{cases}$$

where $\tau_1 = (R||R_{ON})C_{eq}$, $\tau_2 = RC_{eq}$ and we've assumed that $\tau_1 << T$ and $\tau_2 << T$. The input square wave and v_1 are sketched in Figure 4.

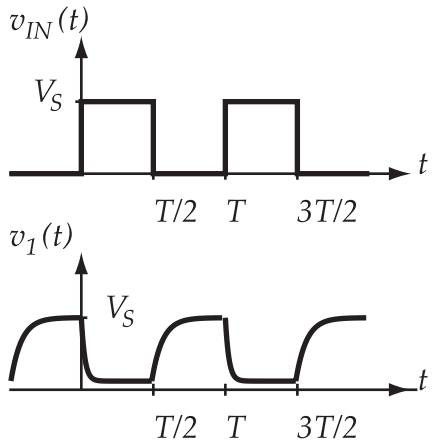

Figure 4: Input for Problem 8.2

(A) Use the above expressions to calculate the total energy dissipated in $M1$ and the pull-up resistor R during the first half period.

(B) Repeat (A) during the second half period.

(C) Using the results of (A) and (B), calculate the time averaged power dissipated in $M1$ and the pull-up resistor. Identify the terms corresponding to static and dynamic power.

(D) Let $R = 100k\Omega$, $R_{ON} = 10k\Omega$, $V_S = 5V$, $C_{eq} = 10^{-2}pF$ and $T = 10^{-8}s$. Evaluate the result found in (C). Which term dominates, the static or dynamic power?

Problem 8.3: Do exercise 4 on page 778 in A&L.

Problem 8.4: Consider again the Boolean expressions from Problem 4.2 that you implemented using NMOS logic and pull-up resistors:

(A) $A + \bar{B} + \bar{C}$

(B) $AB\bar{C}$

(C) $AB + C$

Draw circuit diagrams that implement each of these logical functions using CMOS logic.

Problem 8.5: Consider the logic circuit illustrated in Figure 5. Model each of the MOSFETs with the SR model and assume that $M4$ has a gate-to-source capacitance C_{GS}. Assume that all MOSFETs have the same $R_{ON} << R$. Assume further that the inputs cycle through each of the eight possible states ABC in the order 000, 001, 010, 011, 100, 101, 110, 111 dwelling in each state for time $T >> RC_{GS}$. Determine the average power dissipated in this circuit over the time required for a complete input cycle.

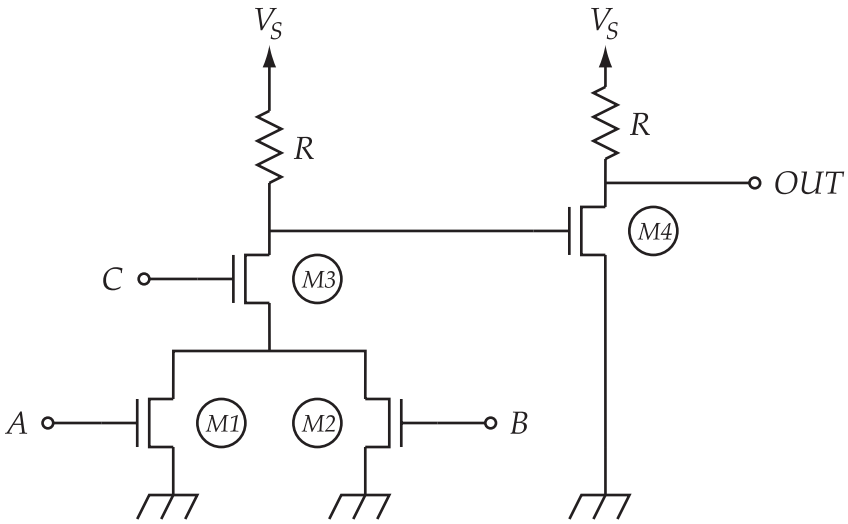

Figure 5: Circuit for Problem 8.5