MASSACHUSETTS INSTITUTE OF TECHNOLOGY
Department of Electrical Engineering and Computer Science

6.002 – Electronic Circuits
Fall 2002

Problem Set 9

Issued: October 30, 2002 **Due: November 6, 2002**

Reading Assignment:

- A&L Sections 13.2-4 for Wednesday, October 30.
- A&L Sections 13.5-12 for Thursday, October 31.
- A&L Chapter 14 and Appendices A and B for Tuesday, November 5.

Problem 9.1: Consider the inverter circuit shown in Figure 1(a), where C_{eq} accounts for the capacitance of the gates the inverter drives and L_{eq} represents lead inductance.

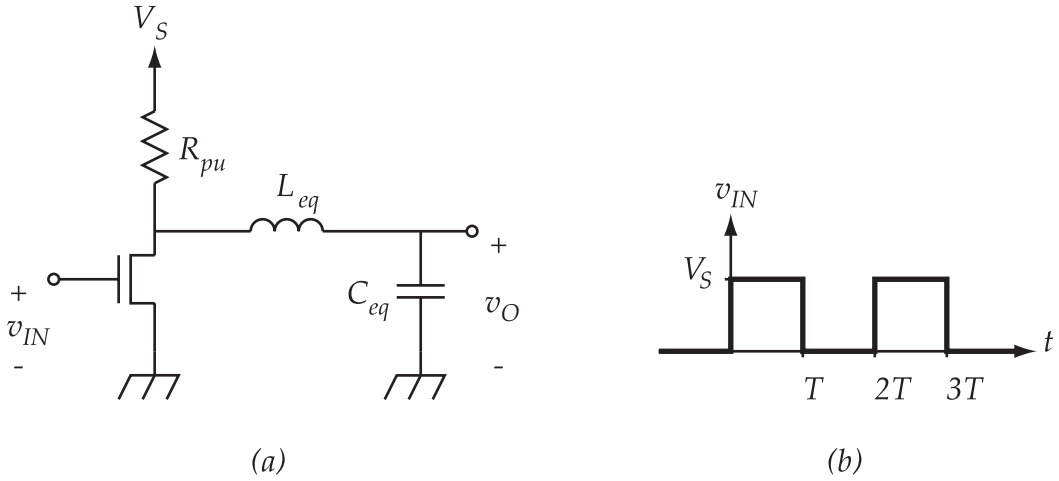

Figure 1: Circuit for Problem 9.1

(A) Calculate and sketch $v_o(t)$ when the circuit is driven by the square wave input in Figure 1(b). Assume that $L/R << T$ and $\sqrt{L/C} > R/2$, where R is the effective resistance in the L-C circuit, i.e., either R_{pu} or $R_{pu}||R_{ON}$. Make reasonable approximations.

(B) Suppose $V_{OH} = 0.8V_S$. What constraint does this impose on the circuit parameters? For example, how much lead inductance could be tolerated if $R_{pu} = 1k\Omega$, $C = 10^{-2}pF$, and $R_{ON} << R_{pu}$?

Save your results from Problem 9.1 for use in the Pre-Lab of Lab #3.

Problem 9.2:

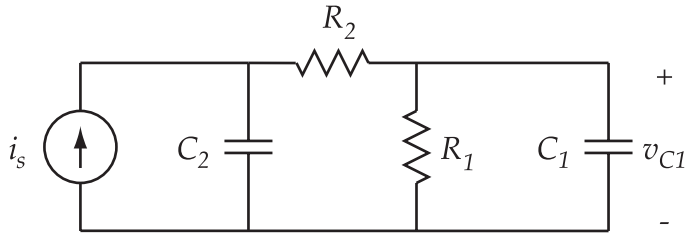

Figure 2: Circuit for Problem 9.2

(A) For the circuit in Figure 2, determine a differential equation relating the capacitor voltage $v_{C1}(t)$ to the source current $i_S(t)$.

(B) Find $v_{C1}(t)$ for $i_S = I_S u(t)$ and the following circuit parameters $R_1 = 1\Omega$, $C_1 = 2/3F$, $R_2 = 3\Omega$, $C_2 = 1/6F$. Organize your solution according to the following steps:

(i) Determine the natural frequencies, i.e., the roots of the characteristic equation;
(ii) Write down the most general form of the solution of the homogeneous equation;
(iii) Determine a particular solution valid for $t > 0$;
(iv) Find the initial conditions, $v_{C1}(0^+)$ and $\frac{dv_{C1}}{dt}|_{0^+}$ arguing directly from the circuit;
(v) Use the results of steps (i)-(iv) to complete the solution for $v_{C1}(t)$ valid for $t > 0$.

Problem 9.3:

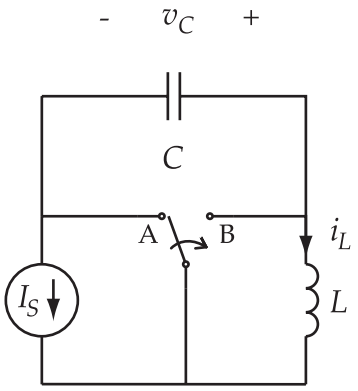

Figure 3: Circuit for Problem 9.3

The circuit shown in Figure 3 is "current pump", so-named because, by repetitively moving the switch between terminals A and B, the current is the inductor can be increased to arbitrarily high values (at least within the framework of our model). In this problem, we'll investigate its operation for the first two switching cycles.

(A) For $t < 0$, the switch is in position A and no energy is stored in the circuit. At $t = 0$, the switch is moved to position B for a time T. Determine and sketch $v_C(t)$ and $i_L(t)$ for $0 < t < T$.

(B) At time T the switch is moved back to position A and held there until time T_1, where T_1 is the time at which the capacitor voltage has decreased to zero. Determine and sketch $v_C(t)$ and $i_L(t)$ for $T < t < T_1$.

(C) At time T_1 the switch returns to position B and is held there for a duration T (the same duration as in part (A)). Determine $v_C(t)$ and $i_L(t)$ for $T_1 < t < T_1 + T$.

(D) Finally, at time $T_1 + T$ the switch moves back to position B and remains there until time T_2, where T_2 is again the time at which the capacitor voltage has decreased to zero. Determine and sketch $v_C(t)$ and $i_L(t)$ for $T_1 + T < t < T_2$, and find the time T_2.

(E) Summarize the results of parts (A)-(D) by providing a clearly labeled sketch of $v_C(t)$ and $i_L(t)$ for $0 < t < T_2$.

Problem 9.4: This problem is a continuation of Problem 9.3. It uses energy conservation to analyze the operation of the current pump.

(A) Determine the energy stored in the capacitor at time T.

(B) The energy stored in the capacitor at time T is transferred to the inductor at time T_1. Use this fact to calculate $i_L(T_1)$ and compare with your answer to part (B) of Problem 9.3.

(C) Determine the energy stored in the capacitor at time $T_1 + T$.

(D) Use energy conservation to find $i_L(T_2)$. The result should be the same as found in part (D) of Problem 9.3.

(E) Now suppose that the switch moves repetitively through the A→B→A cycle, where the duration in position A is always T and the duration in position B is that required for the capacitor voltage to go to zero. Assuming that v_C and I_L are initially zero, determine i_L at the end of the nth switching cycle in terms of n, C, L, T and I.