

MASSACHUSETTS INSTITUTE OF TECHNOLOGY  
Department of Electrical Engineering and Computer Science

6.002 – Electronic Circuits  
Fall 2002

Quiz 2 Solutions

Name: \_\_\_\_\_ Recitation Section: \_\_\_\_\_

Recitation Instructor: \_\_\_\_\_ Teaching Assistant: \_\_\_\_\_

Enter all your work and your answers directly in the spaces provided on the printed pages. Make sure that your name is on all sheets. Use the backs of the printed pages as scratch paper, but we will only grade the work that you neatly transfer to the spaces on the printed pages. Answers must be derived or explained, not just simply written down. The quiz is closed book, but **calculators are allowed**.

This quiz contains 8 pages including the cover sheet. Make sure that your quiz contains all 8 pages and that you hand in all 8 pages.

| Problem | Points | Grade | Grader |
|---------|--------|-------|--------|
| 1       | 50     |       |        |
| 2       | 50     |       |        |
| Total   | 100    |       |        |

**Problem 1:** (50 points) Figure 1(a) shows a simple one-stage MOSFET amplifier. The input-output relationship is graphed in Figure 1(b), where the solid curve indicates operation in the saturated region and the dashed curves indicate operation in the cutoff and triode regions.

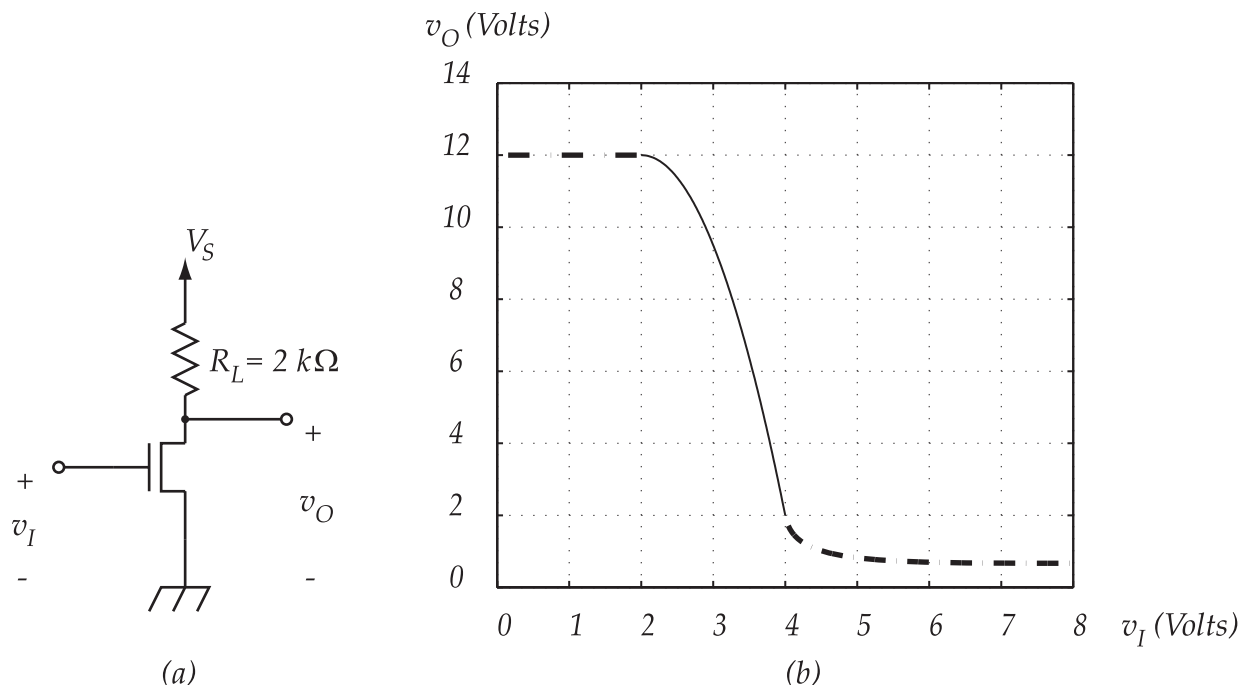


Figure 1: Circuit and characteristic for Problem 1

(A) Determine the MOSFET threshold voltage  $V_T$  and the power supply voltage  $V_S$ .

$$V_T = \underline{2V}$$

$$V_S = \underline{12V}$$

(B) Determine the MOSFET parameter  $K$ .

$$v_O = V_S - R_L K / 2 (v_I - V_T)^2 = 12V - 10^3 \Omega \cdot K (v_I - 2V)^2$$

Using point  $v_I = 4V$ ,  $v_O = 2V$

$$2V = 12V - 10^3 \Omega \cdot K (4V - 2V)^2 \Rightarrow K = 2.5 \text{mA/V}^2$$

$$K = \underline{2.5 \text{mA/V}^2}$$

(C) Determine the minimum and maximum small-signal gain  $|\frac{v_o}{v_i}|$  in the saturated region. A graphical solution is acceptable.

$$\left| \frac{v_o}{v_i} \right| = R_L K (v_I - V_T) = 5V^{-1} (v_I - 2V)$$

$$\text{If } v_I \in [2, 4] \text{ then } \left| \frac{v_o}{v_i} \right| \in [0, 10]$$

$$\min \left| \frac{v_o}{v_i} \right| = \underline{0}$$

$$\max \left| \frac{v_o}{v_i} \right| = \underline{10}$$

The circuit shown in Figure 2 is used to bias the amplifier and inject an input signal to be amplified. The values of  $R_1$  and  $R_2$  are to be determined.

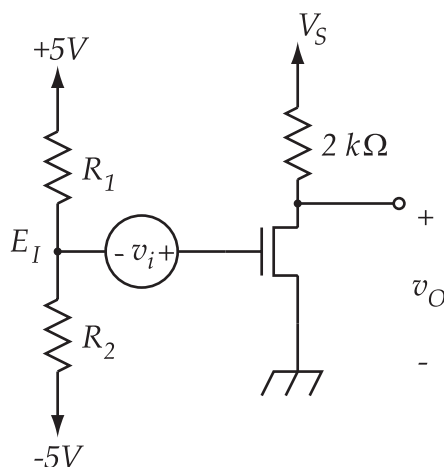


Figure 2: Circuit for Problem 1(D), where  $v_O = V_O + v_o$

- (D) Determine the bias voltage  $E_I$  (with respect to ground) such that equal positive and negative excursions of  $v_o$  can be as large as possible without leaving the saturation region.

For maximum excursions, center  $V_O$  in the middle of the saturation region, i.e.,  $V_O = 7V$ .

With  $v_i = 0V$  (since it is small-signal and we're computing bias conditions), choose  $E_I$  such that  $V_O = 7V$ .

$$7V = 12V - 5/2V^{-1}(E_I - 2V)^2 \Rightarrow E_I = (2 + \sqrt{2})V \approx 3.4V$$

$$E_I = \underline{3.4V}$$

- (E) The resistors in Figure 2 satisfy the constraint  $R_1 + R_2 = 10k\Omega$ . Determine values for  $R_1$  and  $R_2$  so that the bias voltage  $E_I$  will be that found in part (D).

$$E_I = \frac{R_2}{R_1 + R_2}5V - \frac{R_1}{R_1 + R_2}5V = \frac{5V}{10k\Omega}(R_2 - R_1)$$

$$R_2 - R_1 = (4 + 2\sqrt{2})k\Omega$$

$$R_1 + R_2 = 10k\Omega$$

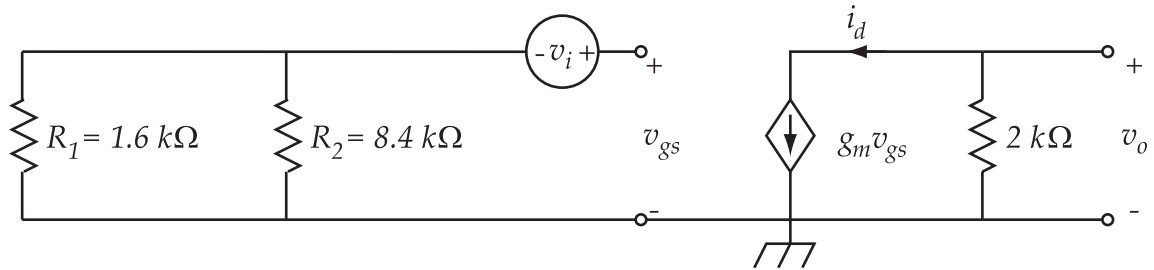
$$\Rightarrow R_1 = (3 - \sqrt{2})k\Omega \approx 1.6k\Omega$$

$$\Rightarrow R_2 = (7 + \sqrt{2})k\Omega \approx 8.4k\Omega$$

$$R_1 = \underline{1.6k\Omega}$$

$$R_2 = \underline{8.4k\Omega}$$

- (F) Draw the small-signal circuit valid for the operating point defined in part (D). Label the numerical values of all circuit parameters and determine the small-signal gain at this operating point from your circuit.



$$g_m = \frac{i_d}{v_{gs}} = \left. \frac{\partial i_D}{\partial v_{GS}} \right|_{v_{GS}=E_I} = K(E_I - V_T)$$

$$= 2.5 \text{ mA/V}^2 [(2 + \sqrt{2})\text{V} - 2\text{V}] = \frac{5\sqrt{2}}{2} \text{ mS} \approx 3.5 \text{ mS}$$

Gain:

$$\frac{v_o}{v_i} = -2 \text{ k}\Omega \cdot \frac{5\sqrt{2}}{2} \text{ mS} = -5\sqrt{2} \approx -7$$

$$\left| \frac{v_o}{v_i} \right| = 5\sqrt{2} \approx 7$$

**Problem 2:** (50 points) The circuit of Figure 3 is a model for a proposed logic inverter which is to join a logic family whose members must satisfy the following digital discipline:

$$\begin{aligned} V_{IH} &= 3.3V & V_{OH} &= 4.0V \\ V_{IL} &= 1.55V & V_{OL} &= 1.0V \end{aligned}$$

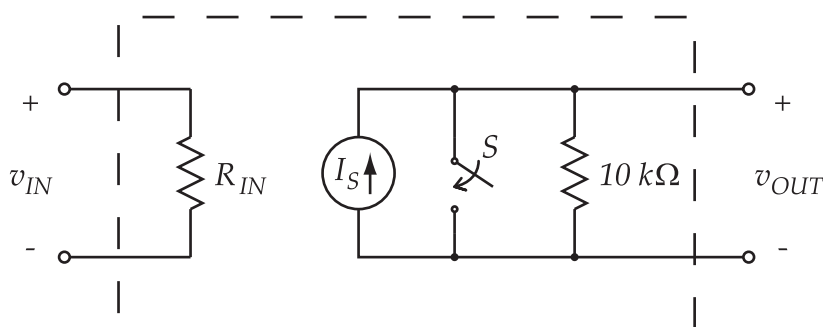


Figure 3: Circuit for Problem 2

Switch S is controlled by the voltage  $v_{IN}$  such that it is open when  $v_{IN} \leq 1.8V$  and closed otherwise. Also,  $I_S = 0.5mA$  in the current source.

(A) Fill in the following table with the output voltages which will result if the circuit is supplied by input voltages which satisfy the digital discipline:

| Input | $v_{OUT}(V)$ |
|-------|--------------|
| High  | 0V           |
| Low   | 5V           |

If  $v_{IN} < v_{IL} = 1.55V$  then switch S is open and  $v_{OUT} = 0.5mA \times 10k\Omega = 5V$ .

If  $v_{IN} > v_{IH} = 3.3V$  then switch S is closed, the output terminal is shorted and  $v_{OUT} = 0V$ .

- (B) Each gate in this logic family will have the same input resistance  $R_{IN}$ . One of the requirements of this gate is that it be able to drive up to three other gates from this family, connected in parallel. Find the minimum allowable value of  $R_{IN}$ ,  $R_{min}$ , such that this gate will satisfy the digital discipline under all acceptable operating configurations.

The constraint is  $(R_{min}/3 || 10k\Omega) \times I_S = V_{OH}$ .  
 $\Rightarrow R_{min} = 120k\Omega$

$$R_{min} = \underline{120k\Omega}$$

- (C) What is the noise margin for this logic family (i.e., what is the maximum noise amplitude in  $V$  that can appear anywhere in a circuit in which this logic family is used such that all the gates in this circuit are guaranteed to operate properly)?

$$\begin{aligned} \text{Noise margin} &= \min\{V_{IL} - V_{OL}, V_{OH} - V_{IH}\} \\ &= \min\{1.55V - 1.0V, 4.0V - 3.3V\} \\ &= \min\{0.55V, 0.7V\} \\ &= 0.55V \end{aligned}$$

$$\text{Noise margin} = \underline{0.55V}$$

- (D) Circle the logic expressions which describe the logic functions implemented by the circuits shown in Figures 4 and 5 from the respective lists below each figure. The circuits employ the logic inverter of Figure 3 (indicated by a rectangular box). You may assume that each MOSFET has threshold voltage,  $V_T$ , of 2.0V.

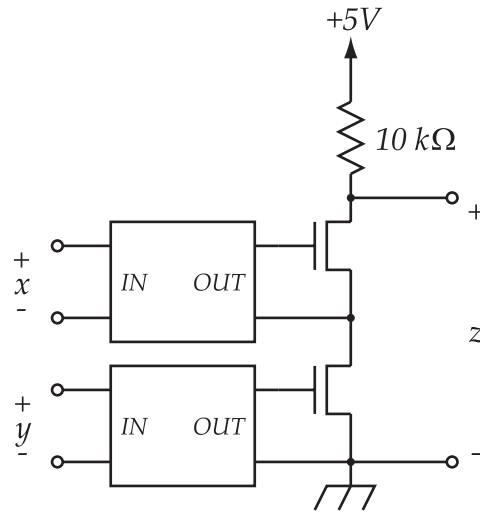


Figure 4: Logic circuit for Problem 2(D)

$$\begin{array}{cccc}
 z = \overline{xy} & z = \overline{x}\overline{y} & \boxed{z = x + y} & z = \overline{x + y} \\
 z = y & z = \overline{x} + xy & z = \overline{xy} & z = x \\
 & & \overline{\overline{xy}} = x + y & 
 \end{array}$$

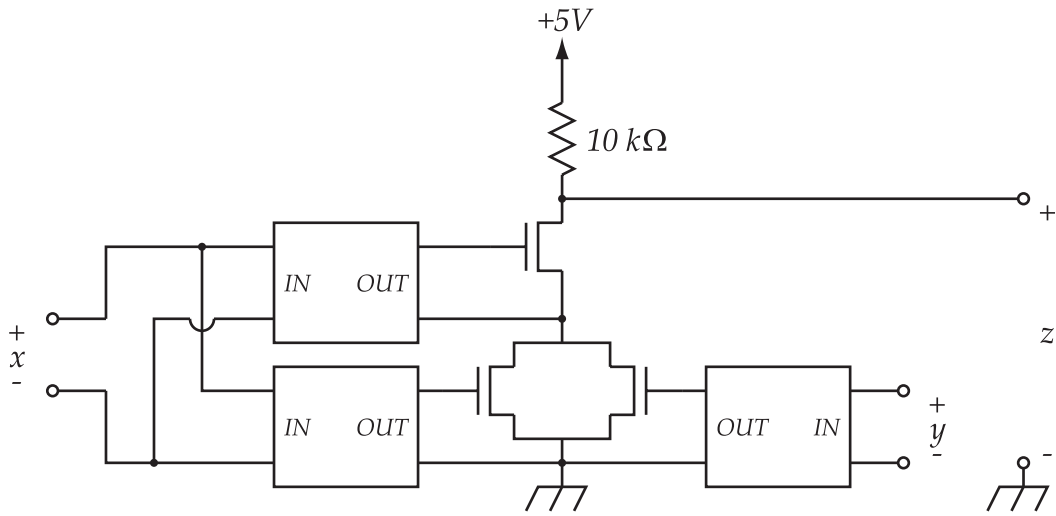


Figure 5: Logic circuit for Problem 2(D)

$$z = \overline{xy} \quad z = \overline{x\bar{y}} \quad z = x + y \quad z = \overline{x + y}$$

$$z = y \quad z = \bar{x} + xy \quad z = \bar{x}y \quad \boxed{z = x}$$

$$\overline{\bar{x}(\bar{x} + \bar{y})} = x$$