Exercise 3.1: Any Boolean function can be completely described by its truth table. For a 3-input function, \( F(A, B, C) \), the truth table contains the following:

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For each of these rows, the value of \( F \) can be 0 or 1. Thus, the total number of such truth tables, and the total number of 3-input Boolean functions, is \( 2^3 = 256 \).

Similarly, for Boolean functions with \( n \) variables, the truth table would have \( 2^n \) rows, with each row corresponding to an output of 0 or 1, so the total number of such functions is \( 2^{2n} \).

Exercise 3.2: a) From sum of products, we find that

\[
F = \overline{A} \overline{B} \overline{C} + A \overline{B} C + A \overline{B} C + A B C,
\]

\[
G = \overline{A} B C + A \overline{B} C + A B \overline{C} + A B C.
\]

b) Simplifying \( F \), we get

\[
F = (\overline{A} + A) \overline{B} \overline{C} + A C (\overline{B} + B)
\]

\[
= \overline{B} \overline{C} + A C,
\]

which can be implemented as follows:
d) $F$ can be simplified by using DeMorgan’s Laws as

$$F = \overline{B \overline{C}} + A\overline{C} = \overline{BC} \overline{A C}.$$ 

Then, by noting that, $\overline{A} = \overline{A A}$, $F$ can be implemented as

It is not a coincidence that $F$ can be implemented using only 2-input NAND gates. In fact, any computable logic function can be built using only 2-input NAND (or NOR) gates.

**Exercise 3.3:**

a) $OUT = \overline{A} = A$

b) $OUT = \overline{A + \overline{B}} = AB$

c) $OUT = \overline{A(B + \overline{C})} = \overline{A + \overline{B + C}} = \overline{A} + \overline{BC}$

d) $OUT = (AB + C)\overline{EN} = \overline{AB + C + EN}$

**Problem 3.1:** From the gate-level circuit, the function is

$$Z = \overline{AB \overline{BC}} = A\overline{B} + BC,$$

which corresponds to the following truth table:
Then, noting that the input signals satisfy the static discipline, we can determine $Z$ for each combination of the inputs and plot the output as shown below. Note that the actual output voltage levels can be any of those that satisfy the static discipline.

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<tr>
<th>$A$</th>
<th>$B$</th>
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**Problem 3.2:** In order for one logic family to drive another, we must confirm that the driving family’s output levels, $V_{OL}$ and $V_{OH}$, are below and above, respectively, the input levels, $V_{IL}$ and $V_{IH}$, of the driven family. Put another way, if family $A$ is driving family $B$, the two following...
equations must be satisfied:

\[ \begin{align*}
V_{OL,A} &< V_{IL,B}, \\
V_{OH,A} &> V_{IH,B}.
\end{align*} \]

For a YTL inverter driving an NTL inverter, both of these constraints are satisfied, and the circuit will operate correctly.

\[ \begin{align*}
V_{OL,YTL} &= 0.3 < 1.5 = V_{IL,NTL} \\
V_{OH,YTL} &= 4.5 > 3.5 = V_{IH,NTL}
\end{align*} \]

For an NTL inverter driving a YTL inverter, however, only one of the constraints is satisfied, and, therefore, the circuit may not function correctly.

\[ \begin{align*}
V_{OL,NTL} &= 1.0 \not< 0.8 = V_{IL,YTL} \\
V_{OH,NTL} &= 4.0 > 3.0 = V_{IH,YTL}
\end{align*} \]

**Problem 3.3:** a) The inverter must produce an output greater than \( V_{OH} \) with an input \( < V_{IL} \), with its transfer function having a slope \( \leq 1 \) in this region. Similarly, it must produce an output less than \( V_{OL} \) for inputs \( > V_{IH} \), also with a slope \( \leq 1 \) in this region. An example plot is shown below.

b) The following figure shows the schematic of the inverter and the equivalent circuits using the SR model of the MOSFET when the inputs are below and above the threshold voltage, respectively.
Then, to satisfy the static discipline, we must ensure that $V_{out} < V_{OL}$ whenever $V_{in} > V_{IH}$ and $V_{out} > V_{OH}$ when $V_{in} < V_{IL}$.

Case 1: $V_{in} < V_{IL} = 1.6$. As these input voltages are all less than the threshold of the MOSFET, the MOSFET is off, as shown in the middle schematic above. Thus, $V_{out} = V_{S} = 5V > 4.4V$, and the static discipline is satisfied independent of the dimensions of the resistor and MOSFET.

Case 2: $V_{in} > V_{IH} = 3.2$. Since $3.2 > 1.8 = V_{T}$, the transistor is on, and the circuit behaves as depicted on the right of the above figure. We can solve for

$$V_{out} = \frac{R_{on}}{R_{on} + R_{PU}} V_{S} < V_{OL} = 0.5 \implies R_{on} \leq \frac{R_{PU}}{9}.$$

At this point, we can arbitrarily choose $R_{on}$ and $R_{PU}$ to be any values that satisfy the above equation and then choose proper combinations of $L_{T}/W_{T}$ and $L_{R}/W_{R}$ to meet these resistances:

$$R_{PU} = 9k\Omega \quad \quad \quad R_{on} = 1k\Omega$$

$$= R_{C}(L_{R}/W_{R}) \quad \quad = R_{n}(L_{T}/W_{T})$$

$$= 500 \cdot (L_{R}/W_{R}) \quad \quad = 1k \cdot (L_{T}/W_{T})$$

$$L_{R} = 9\mu m \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad L_{T} = 0.5\mu m$$

$$W_{R} = 0.5\mu m \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad W_{T} = 0.5\mu m$$

The total area of the inverter is

$$A = L_{R}W_{R} + L_{T}W_{T} = 4.75\mu m^{2}.$$

Power is only dissipated when the input is high, and the power dissipated is

$$P = \frac{V_{S}^{2}}{R_{on} + R_{PU}} = \frac{25}{10k} = 2.5mW.$$

Finally, the input-output transfer function is shown below