

Massachusetts Institute of Technology
Department of Electrical Engineering and Computer Science

6.002 – Electronic Circuits

Homework #4 Solution
Handout F98-31

Exercise 4-1: For the two Boolean expressions given below, express C as a function of A and B in the form of a truth table. Also, implement each expression using NOT, NAND and/or NOR gates.

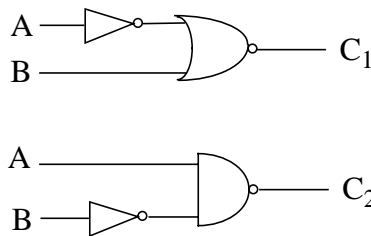
$$C_1 = \overline{\overline{A} + B} \quad C_2 = \overline{A \cdot \overline{B}}$$

Answer:

Applying DeMorgan's Law, we find that $C_1 = \overline{\overline{A} + B} = A \cdot \overline{B} = \overline{C_2}$.

| A | B | $C_1 = \overline{\overline{A} + B}$ | $C_2 = \overline{A \cdot \overline{B}}$ |
|-----|-----|-------------------------------------|---|
| 0 | 0 | 0 | 1 |
| 0 | 1 | 0 | 1 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 1 |

C_1 and C_2 can be directly implemented with NOT, NAND, and NOR gates:



Exercise 4-2: The truth table for an EXCLUSIVE OR gate is given below; the output of an EXCLUSIVE OR gate is TRUE if and only if either input is TRUE alone. Give a logic-gate implementation of the EXCLUSIVE-OR gate in terms of NOT, NAND and NOR gates.

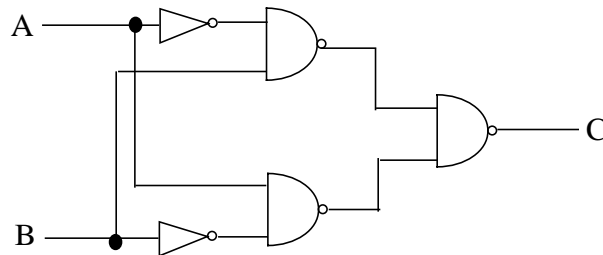
| INPUT 1 | INPUT 2 | OUTPUT |
|---------|---------|--------|
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

Answer:

Let A =INPUT 1, B =INPUT 2, C =OUTPUT, and \oplus =XOR, then from the truth table we find $A \oplus B = \bar{A} \cdot B + A \cdot \bar{B}$.

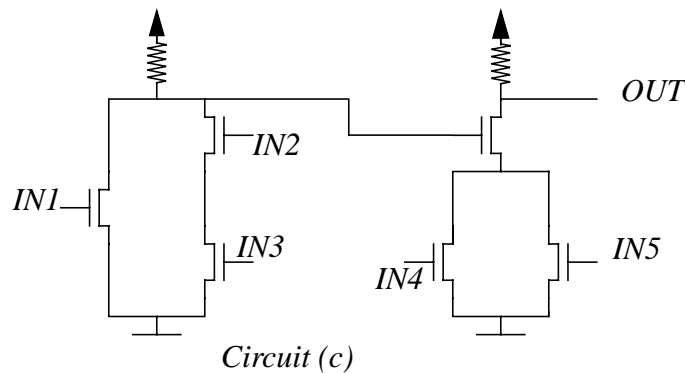
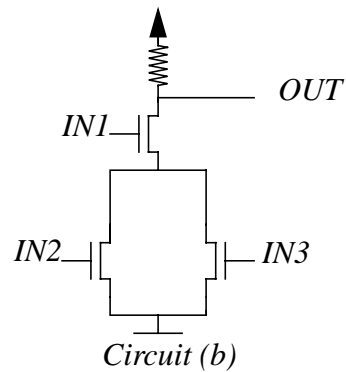
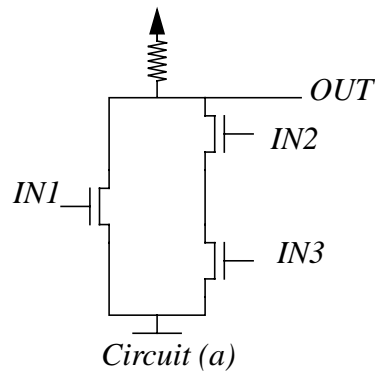
To implement the above logic expression in NOT, NAND, and NOR gates, we need to apply DeMorgan's Law:

$$A \oplus B = \overline{(\bar{A} \cdot B) \cdot (A \cdot \bar{B})}$$



Problem 4-1: This problem continues to explore the implementation of Boolean logic functions with MOSFET switches.

- (a) Determine the Boolean expression implemented by each of the following circuits. Assume that each input is TRUE if it is large enough to turn its corresponding MOSFET on, and FALSE if it is not.



Answer:

circuit(a) The output is low if either $IN1$ is high **or** both $IN2$ **and** $IN3$ are high. The logic function for this is

$$OUT = \overline{IN1 + (IN2 \cdot IN3)}$$

circuit(b) The output is low if $IN1$ is high **and** either $IN2$ **or** $IN3$ is high. This results in the logic function

$$OUT = \overline{IN1 \cdot (IN2 + IN3)}$$

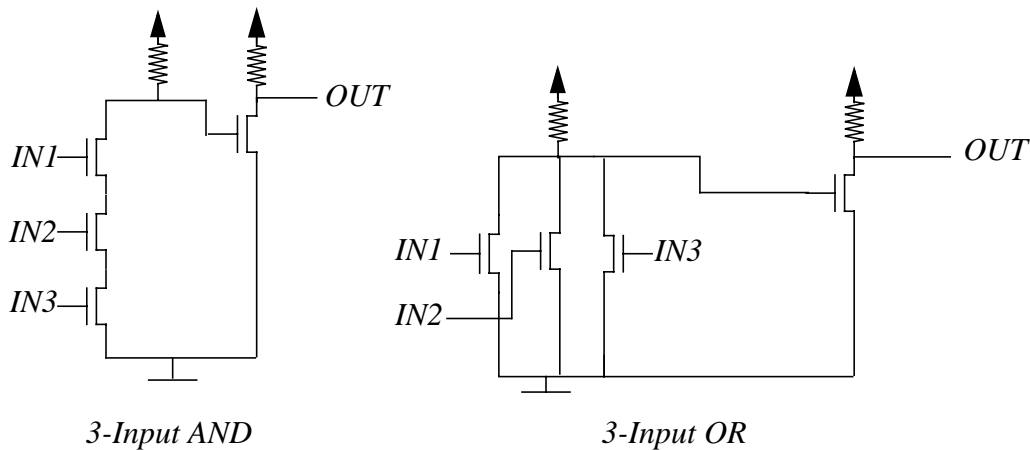
circuit(c) Nested logic gates work the same way provided that the static discipline is satisfied. In this circuit, we simply replace the input $IN1$ in circuit (b) by the output of circuit (a). The result is

$$OUT = \overline{\overline{(IN1 + IN2 \cdot IN3)} \cdot (IN4 + IN5)}$$

- (b) Note that an OR gate can be made from a NOR gate followed by a NOT gate, and that an AND gate can be made from a NAND gate followed by a NOT gate. Following this reasoning, develop a MOSFET-resistor implementation of a three-input OR gate and a three-input AND gate.

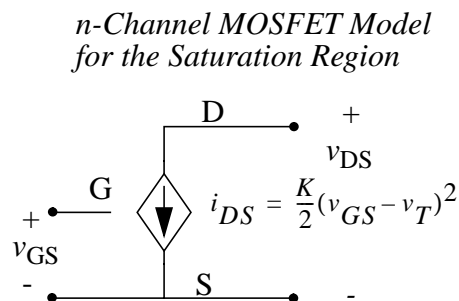
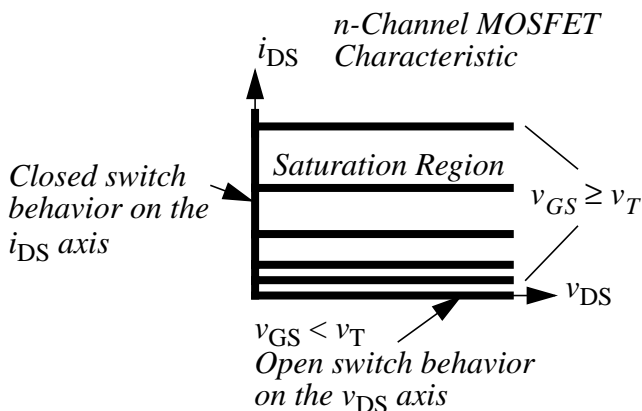
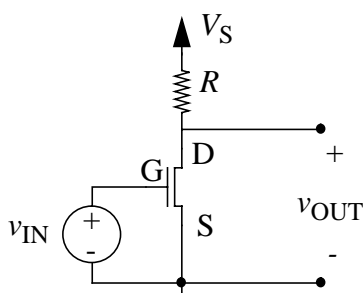
Answer:

AND and OR are implemented by inverting the output of NAND and NOR logic functions. This requires one extra gate for each case.



Problem 4-2: An inverting MOSFET amplifier is shown below, together with an i_{DS} - v_{DS} characteristic for the MOSFET. The characteristic describes ideal switch behavior that is extended to exhibit a saturating drain-source current. For $v_{GS} < v_T$, the MOSFET behaves like an open switch with $i_{DS} = 0$. For $v_{GS} \geq v_T$, the MOSFET behaves like a closed switch with $v_{DS} = 0$ provided that $i_{DS} < 0.5K(v_{GS} - v_T)^2$. However, once i_{DS} reaches $0.5K(v_{GS} - v_T)^2$, which is the maximum current the MOSFET can carry for a given v_{GS} , MOSFET operation enters a saturation region in which the MOSFET behaves as a current source of value $0.5K(v_{GS} - v_T)^2$. Saturated operation is as described by the saturation model given below.

Note that the MOSFET characteristic described above and shown below is simpler than the SCS model presented in class and discussed in the notes. The characteristic shown here has no linear region.



- (a) Determine v_{OUT} as a function of v_{IN} for $0 \leq v_{IN}$.

Answer:

When there is current going through R , the current is limited by two quantities: either V_S/R or $0.5K(v_{GS} - v_T)^2$, whichever is lower. If the limit is V_S/R , then the MOSFET is in the closed-switch region. If the limit is $0.5K(v_{GS} - v_T)^2$, then the MOSFET is in the saturation region.

open-switch region For $v_{GS} \leq v_T$, the MOSFET is open, therefore $v_{OUT} = V_S$.

saturation region When v_{GS} begins to exceed v_T , the quantity $v_{GS} - v_T$ is still small, so the current is limited by $0.5K(v_{GS} - v_T)^2$. This current determines the output voltage, which is given by $v_{OUT} = V_S - 0.5KR(v_{IN} - v_T)^2$.

closed-switch region i_{DS} increases until it reaches V_S/R at some gate voltage v_{IN_T} . Now v_{DS} drops to zeros, and both i_{DS} and v_{DS} are no longer affected by the increase in v_{GS} .

In summary,

$$v_{OUT} = \begin{cases} V_S & 0 \leq v_{IN} \leq v_T \\ V_S - 0.5KR(v_{IN} - v_T)^2 & v_T \leq v_{IN} \leq v_{IN_T} \\ 0 & v_{IN_T} \leq v_{IN} \leq v_{IN_{MAX}} \end{cases}$$

(b) What is the lowest value of v_{IN} for which $v_{OUT} = 0$?

Answer:

The lowest value of v_{IN} for which $v_{OUT} = 0$ occurs when v_{IN} is at the *transition* between the saturation region and the closed-switch region. At this point, the saturation region current limit and the closed-switch region current limit are the same,

$$i_{DS} = \frac{V_S}{R} = 0.5K(v_{IN_T} - v_T)^2$$

Solving for v_{IN_T} we get

$$v_{IN_T} = \sqrt{\frac{2V_S}{KR}} + v_T$$

(c) Assume that $V_S = 15$ V, $R = 15$ k Ω , $v_T = 1$ V and $K = 2$ mA/V². Graph v_{OUT} versus v_{IN} for 0 V $\leq v_{IN} \leq 3$ V.

Answer:

Combining the results of part (a) and (b), we obtain the following equations.

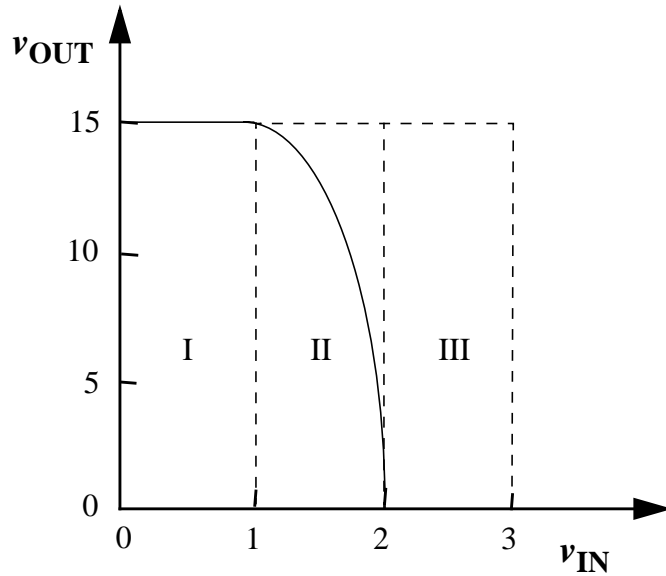
$$v_{OUT} = \begin{cases} 15 & 0 \leq v_{IN} \leq 1 \\ 15 - 15(v_{IN} - 1)^2 & 1 \leq v_{IN} \leq 2 \\ 0 & 2 \leq v_{IN} \leq 3 \end{cases}$$

The graph is shown on the next page.

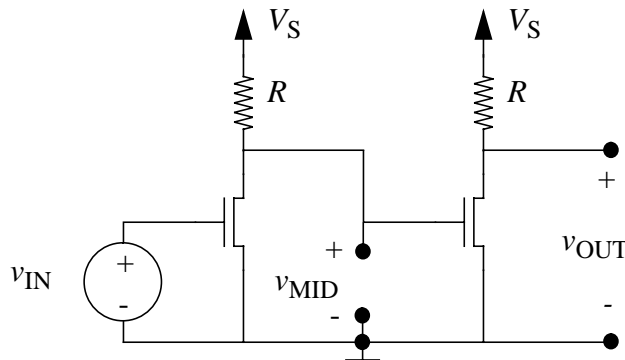
(d) On the input-output graph, identify the regions over which the MOSFET behaves as an open circuit, behaves as a short circuit, and exhibits saturated behavior.

Answer:

Region I is the open switch region, where $v_{OUT} = V_S = 15$. Region II is the saturation region, where v_{OUT} drops according to $V_S - 0.5KR(v_{IN} - v_T)^2$. The MOSFET enters the closed-switch region when $v_{IN} = v_{IN_T} = 2$. In this region, $v_{OUT} = 0$.



Problem 4-3: A two-stage amplifier is shown in the figure below. It is constructed by cascading two one-stage amplifiers of the type studied in Problem 4-2. In analyzing this amplifier, use the MOSFET model described in Problem 4-2.



- (a) The fact that a second amplifier stage is connected to the first amplifier stage does not change the operation of the first stage. That is, the relation between v_{MID} and v_{IN} here is the same as the relation between v_{OUT} and v_{IN} in Problem 4-2. Why? What terminal characteristic of the second MOSFET must change in order for this not to be true?

Answer:

The second amplifier does not change the operation of the first because its input draws no current. If the second amplifier drew current from the first, then the output of the first amplifier would be affected by the input resistance of the second amplifier.

- (b) Derive the relation between v_{MID} and v_{IN} for $0 \leq v_{IN}$, and the relation between v_{OUT} and v_{MID} for $0 \leq v_{MID} \leq V_S$. Hint: see Problem 4-2.

Answer:

Each amplifier obeys the model described in Problem 4-2.

For the first amplifier,

$$v_{\text{MID}} = \begin{cases} V_S & 0 \leq v_{\text{IN}} \leq v_T \\ V_S - 0.5KR(v_{\text{IN}} - v_T)^2 & v_T \leq v_{\text{IN}} \leq v_{\text{IN}_T} \\ 0 & v_{\text{IN}_T} \leq v_{\text{IN}} \leq v_{\text{IN}_{\text{MAX}}} \end{cases}$$

For the second amplifier,

$$v_{\text{OUT}} = \begin{cases} V_S & 0 \leq v_{\text{MID}} \leq v_T \\ V_S - 0.5KR(v_{\text{MID}} - v_T)^2 & v_T \leq v_{\text{MID}} \leq v_{\text{MID}_T} \\ 0 & v_{\text{MID}_T} \leq v_{\text{MID}} \leq v_{\text{MID}_{\text{MAX}}} \end{cases}$$

(c) Derive the relation between v_{OUT} and v_{IN} for $0 \leq v_{\text{IN}}$.

Answer:

This part is slightly trickier. Since the two inverters are in series, we should expect three regions of operations: low $v_{\text{IN}} \Rightarrow$ low v_{OUT} , nonlinear transition, and high $v_{\text{IN}} \Rightarrow$ high v_{OUT} . To compute the boundary values between the regions, we first need to find the values of v_{MID} that cause transition in v_{OUT} , then we can solve for the v_{IN} values that produce those particular v_{MID} values.

low-low region $v_{\text{OUT}} = 0$ for $v_{\text{MID}_T} \leq v_{\text{MID}} \leq v_{\text{MID}_{\text{MAX}}}$. This corresponds to $0 \leq v_{\text{IN}} \leq v_{\text{IN}_1}$ where

$$v_{\text{MID}_T} = V_S - 0.5KR(v_{\text{IN}_1} - v_T)^2$$

solving for v_{IN_1} we get

$$v_{\text{IN}_1} = \sqrt{\frac{2(V_S - v_{\text{MID}_T})}{KR}} + v_T$$

saturation region The second amplifier is in the saturation region for $v_T \leq v_{\text{MID}} \leq v_{\text{MID}_T}$. This corresponds to the input voltage range $v_{\text{IN}_1} \leq v_{\text{IN}} \leq v_{\text{IN}_2}$, where v_{IN_2} is given by

$$v_T = V_S - 0.5KR(v_{\text{IN}_2} - v_T)^2$$

Solving for v_{IN_2} we get

$$v_{\text{IN}_2} = \sqrt{\frac{2(V_S - v_T)}{KR}} + v_T$$

Furthermore, in this region

$$v_{\text{OUT}} = V_S - 0.5KR(v_{\text{MID}} - v_T)^2$$

substituting

$$v_{\text{MID}} = V_S - 0.5KR(v_{\text{IN}} - v_T)^2$$

into the previous equation, we get

$$v_{\text{OUT}} = V_S - 0.5KR(V_S - 0.5KR(v_{\text{IN}} - v_T)^2 - v_T)^2$$

high-high region $v_{\text{OUT}} = V_S$ for $v_{\text{MID}} \leq v_T$, or equivalently, $v_{\text{IN}} \geq v_{\text{IN}_2}$

In summary,

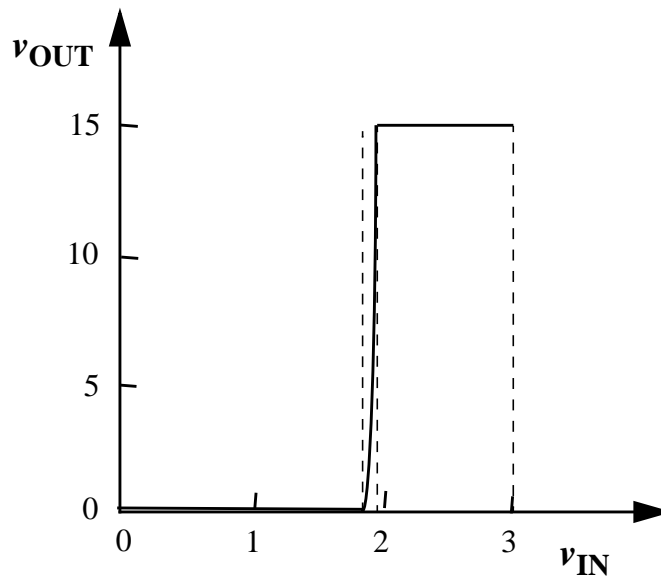
$$v_{\text{OUT}} = \begin{cases} 0 & 0 \leq v_{\text{IN}} \leq v_{\text{IN}_1} \\ V_S - 0.5KR(V_S - 0.5KR(v_{\text{IN}} - v_T)^2 - v_T)^2 & v_{\text{IN}_1} \leq v_{\text{IN}} \leq v_{\text{IN}_2} \\ V_S & v_{\text{IN}_2} \leq v_{\text{IN}} \leq v_{\text{IN}_{\text{MAX}}} \end{cases}$$

- (d) Using the numerical parameters given in Problem 4-2, graph v_{OUT} versus v_{IN} for $0 \text{ V} \leq v_{\text{IN}} \leq 3 \text{ V}$. Compare this graph to the input-output graph found in Problem 4-2, and explain the differences.

Answer:

Using the formulas derived in part (c), we find

$$v_{\text{OUT}} = \begin{cases} 0 & 0 \leq v_{\text{IN}} \leq 1.93 \\ -2925 + 6300(v_{\text{IN}} - 1)^2 - 3375(v_{\text{IN}} - 1)^4 & 1.93 \leq v_{\text{IN}} \leq 1.97 \\ 15 & 1.97 \leq v_{\text{IN}} \leq 3 \end{cases}$$



Note that the transition region of this two-stage amplifier is much narrower than that of the single-stage amplifier in Problem 4-2. This is because when the second amplifier is saturated, the first amplifier is also saturated. Since v_{MID} is the output of the first stage, its range maps into a much smaller range of v_{IN} values.

Problem 4-4: This problem studies the small-signal analysis of the MOSFET amplifier studied in Problem 4-3.

- (a) First consider biasing the amplifier. Determine V_{IN} , the bias component of v_{IN} , so that v_{OUT} is biased to V_{OUT} where $0 < V_{OUT} < V_S$. Find V_{MID} , the bias component of v_{MID} in the process. Hint: see Problem 4-3.

Answer:

$$\begin{aligned} V_{MID} &= V_S - I'_D R \\ &= V_S - 0.5KR(V_{IN} - v_T)^2 \end{aligned}$$

$$\begin{aligned} V_{OUT} &= V_S - I''_D R \\ &= V_S - 0.5KR(V_{MID} - v_T)^2 \end{aligned}$$

From above we can solve for V_{MID} ,

$$V_{MID} = \sqrt{\frac{2(V_S - V_{OUT})}{KR}} + v_T$$

Similarly,

$$\begin{aligned} V_{IN} &= \sqrt{\frac{2(V_S - V_{MID})}{KR}} + v_T \\ &= \sqrt{\frac{2(V_S - (\sqrt{\frac{2(V_S - V_{OUT})}{KR}} + v_T))}{KR}} + v_T \end{aligned}$$

- (b) Next, let $v_{IN} = V_{IN} + v_{in}$ where v_{in} is considered to be a small perturbation of v_{IN} around V_{IN} . Make the substitution for v_{IN} and linearize the resulting expression for v_{OUT} . Your answer should take the form $v_{OUT} = V_{OUT} + v_{out}$, where v_{out} takes the form $v_{out} = Gv_{in}$. Note that v_{out} is the small-signal output and G is the small-signal gain. Derive an expression for G .

Answer:

Let $v_{IN} = V_{IN} + v_{in}$, we first solve for the current i'_D going through the first amplifier,

$$\begin{aligned} i'_D &= .5K(V_{IN} + v_{in} - v_T)^2 \\ &= .5K(V_{IN} - v_T)^2 + Kv_{in}(V_{IN} - v_T) + .5Kv_{in}^2 \\ &\approx .5K(V_{IN} - v_T)^2 + Kv_{in}(V_{IN} - v_T) \\ &= I'_D + i'_d \end{aligned}$$

v_{MID} is related to i'_D by the following equations:

$$\begin{aligned}
v_{\text{MID}} &= V_{\text{S}} - (I_{\text{D}}' + i_{\text{d}}')R \\
&= V_{\text{S}} - .5KR(V_{\text{IN}} - v_{\text{T}})^2 - RKv_{\text{in}}(V_{\text{IN}} - v_{\text{T}})
\end{aligned}$$

Now we solve for the current i_{D}'' , which goes through the second amplifier,

$$\begin{aligned}
i_{\text{D}}'' &= .5K(v_{\text{MID}} - v_{\text{T}})^2 \\
&= .5K(V_{\text{S}} - .5KR(V_{\text{IN}} - v_{\text{T}})^2 - RKv_{\text{in}}(V_{\text{IN}} - v_{\text{T}}) - v_{\text{T}})^2 \\
&= .5K[V_{\text{S}} - .5KR(V_{\text{IN}} - v_{\text{T}})^2 - v_{\text{T}}]^2 \\
&\quad - [V_{\text{S}} - .5KR(V_{\text{IN}} - v_{\text{T}})^2 - v_{\text{T}}][RK^2(V_{\text{IN}} - v_{\text{T}})]v_{\text{in}} \\
&\quad + .5K^3R^2(V_{\text{IN}} - v_{\text{T}})^2v_{\text{in}}^2 \\
&\approx .5K[V_{\text{S}} - .5KR(V_{\text{IN}} - v_{\text{T}})^2 - v_{\text{T}}]^2 \\
&\quad - [V_{\text{S}} - .5KR(V_{\text{IN}} - v_{\text{T}})^2 - v_{\text{T}}][RK^2(V_{\text{IN}} - v_{\text{T}})]v_{\text{in}}
\end{aligned}$$

Finally we relate v_{OUT} to v_{IN} ,

$$\begin{aligned}
v_{\text{OUT}} &= V_{\text{S}} - i_{\text{D}}''R \\
&= V_{\text{S}} - .5KR[V_{\text{S}} - .5KR(V_{\text{IN}} - v_{\text{T}})^2 - v_{\text{T}}]^2 \\
&\quad + K^2R^2[V_{\text{S}} - .5KR(V_{\text{IN}} - v_{\text{T}})^2 - v_{\text{T}}](V_{\text{IN}} - v_{\text{T}})v_{\text{in}} \\
&= V_{\text{OUT}} + v_{\text{out}} \\
&= V_{\text{OUT}} + G_m v_{\text{in}}
\end{aligned}$$

where $G_m = K^2R^2[V_{\text{S}} - .5KR(V_{\text{IN}} - v_{\text{T}})^2 - v_{\text{T}}](V_{\text{IN}} - v_{\text{T}})$.

- (c) For what value of V_{IN} is v_{OUT} biased to $V_{\text{OUT}} = V_{\text{S}}/2$? For this value of V_{IN} , evaluate G using the numerical parameters given in Problem 4-2. You should find that this gain is the slope of the input-output graph from Problem 4-3 evaluated at the bias point.

Answer:

The equation derived in part (a) gives us $V_{\text{IN}} = 1.941$, and the final equation in part (b) yields $G_m = 608$.

In part (d) of Problem 4-3 we find that the large signal

$$v_{\text{OUT}} = -2925 + 6300(v_{\text{IN}} - 1)^2 - 3375(v_{\text{IN}} - 1)^4$$

Taking the derivative of the above we get

$$\frac{dv_{\text{OUT}}}{dv_{\text{IN}}} = 12600(v_{\text{IN}} - 1) - 13500(v_{\text{IN}} - 1)^3$$

Evaluating the above equation at $V_{\text{IN}} = 1.941$ yields $\frac{dv_{\text{OUT}}}{dv_{\text{IN}}} = 608$.

This shows that G_m equals to the slope of the input-output graph evaluated at the bias point.