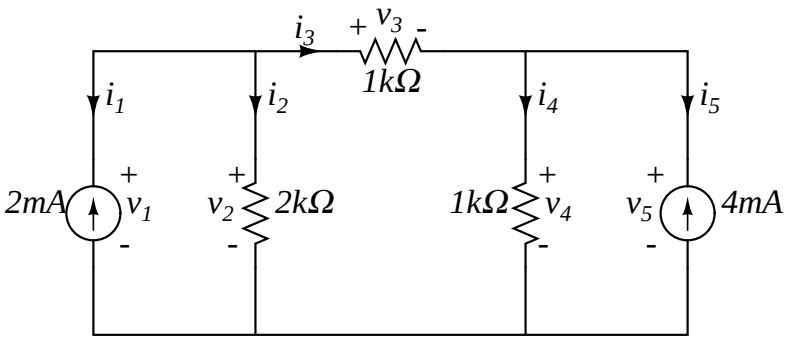
Massachusetts Institute of Technology
Department of Electrical Engineering and Computer Science

6.002 – Electronic Circuits
Spring 2002

Homework #3

Issued 2/20/02 – Due 2/27/02

Exercise 3.1: Find all branch voltages and all branch currents in the network shown below. Hint: use superposition and other simplifications. Also, find the power dissipated in each network element, and show that the total power dissipated across the network is zero.

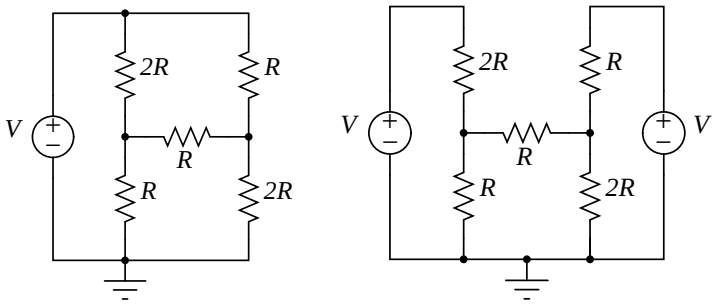


Exercise 3.2: When a particular network having a single port is connected to a 2 kΩ resistor, its port voltage is 2 V. When the same network is connected to a 6 kΩ resistor, its port voltage is 3 V. Determine the Thevenin and Norton equivalents of the network.

Exercise 3.3: This exercise applies two different analyses to determine the unknown node voltages in Network (A) shown below. It illustrates that the direct method of analysis is not always the simplest.

(A) Use the node method to find the two unknown node voltages in Network (A).

(B) First, explain why Network (A) may be re-drawn as network (B). Second, combine the left source in Network (B) with the two left-most resistors to form their Thevenin equivalent and redraw the resulting network. Third, combine the right source with the two right-most resistors to form their Thevenin equivalent and again redraw the resulting network. Finally, using superposition, determine the two unknown node voltages in the thrice re-drawn version of Network (A) thereby completing the analysis.



Problem 3.1: This problem examines the operation and design of the digital logic circuit shown below. It is constructed with two identical pull-up resistors and four identical MOSFETs, and it implements the Boolean expression OUT = (IN1 · IN2) + IN3. Assume that each MOSFET behaves as a switch with threshold voltage V_{T} and on-state resistance R_{ON}.

(A) Assume that the logic circuit functions properly. For each of the eight input logic value combinations, determine the state (ON or OFF) of the four MOSFETs (M1, M2, M3 and M4), the output logic value, and the voltages at the gate and drain of M4. Organize the results in a table having ten columns: the three input logic values, the output logic value, the four MOSFET states and the two voltages.

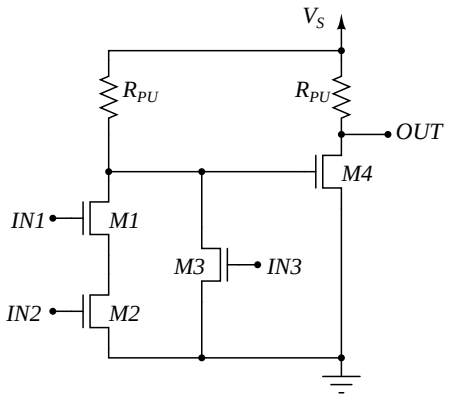
(B) Based on the results of Part (A), what inequalities must V_{T} satisfy so that the voltage at the gate of M4 produces the desired state of M4?

(C) Based on the results of Part (A), what voltage inequalities must be satisfied so that the output voltage at the drain of M4 satisfies the static discipline defined by V_{OH} and V_{OL}?

(D) Assume that the voltages at the three inputs (IN1, IN2 and IN3) satisfy the static discipline defined by V_{IH} and V_{IL}. Based on the results of Part (A), what voltage inequalities must V_{T} satisfy so that the three input voltages produce the desired states of M1, M2 and M3?

(E) Organize the inequalities into a minimal string of inequalities that must be satisfied in order for the digital circuit to function properly and conform to the static discipline.

(F) Assuming that the logic circuit is designed according to the results of Part (E), determine which combinations of input logic values lead to the maximum and minimum power dissipation in the logic circuit.



Problem 3.2: This problem studies the synthesis of a circuit that implements a two-input exclusive-or gate. The Boolean logic function that the two-input exclusive-or gate provides is $\mathrm{OUT} = (\mathrm{IN1} \cdot \overline{\mathrm{IN2}}) + (\overline{\mathrm{IN1}} \cdot \mathrm{IN2}) = (\mathrm{IN1} + \mathrm{IN2}) \cdot (\overline{\mathrm{IN1} \cdot \mathrm{IN2}})$. Thus, the output is true if one or the other input is true, but not both.

(A) Use truth tables to prove DeMorgan's Law. DeMorgan's Law states that $\overline{\mathrm{A} \cdot \mathrm{B}} = \overline{\mathrm{A}} + \overline{\mathrm{B}}$, and equivalently that $\overline{\mathrm{A} + \mathrm{B}} = \overline{\mathrm{A}} \cdot \overline{\mathrm{B}}$.

(B) Using only inverters and two-input nor gates, synthesize an NMOS circuit that implements the two-input exclusive-or gate. This can be done with as few as eight n-channel MOSFETs and five pull-up resistors. Hint: use DeMorgan's Law.

Problem 3.3: This problem examines digital logic circuits in which logic values are represented by positive currents, much like relay logic. Specifically, the logic value 0 is represented by a low-valued current, and the logic value 1 is represented by a high-valued current. The logic circuits are implemented with the current-controlled switch defined below. The switch *opens* when its labeled control current equals or exceeds the threshold current i_{T}, and *closes* otherwise. The control current can be any current in the logic circuit. Note that the switch is imperfect, and has a nonzero off-state conductance, G_{OFF}. Also, assume that i_{T} satisfies $0 < i_{\mathrm{T}} < I_{\mathrm{S}}$, where I_{S} is the supply current.

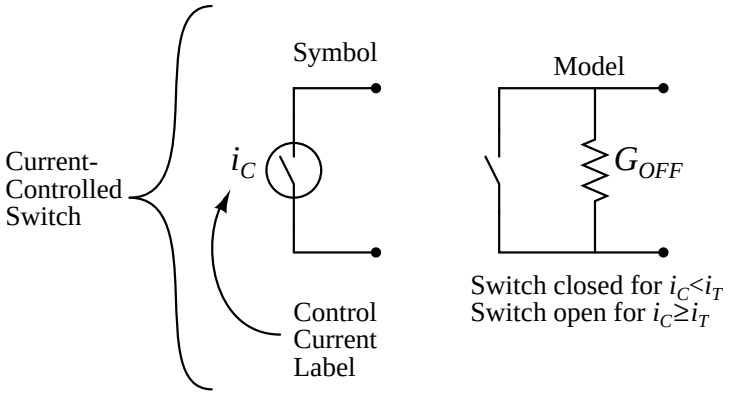
(A) Consider Circuit #1 which is formed with a current-controlled switch, a current supply, and a bypass conductor having conductance G_{BP}. Sketch and clearly label a graph of i_{OUT} as a function of i_{IN} for $0 \leq i_{\mathrm{IN}} \leq I_{\mathrm{S}}$.

(B) Circuit #1 is to satisfy a static discipline defined by I_{L} and I_{H}, where $0 < I_{\mathrm{L}} < I_{\mathrm{H}} < I_{\mathrm{S}}$. That is, for both i_{IN} and i_{OUT}, a valid logic 0 lies between 0 and I_{L}, and a valid logic 1 lies between I_{H} and I_{S}. In this case, within what current range must i_{T} lie, and what is the maximum acceptable value for G_{OFF}?

(C) Consider Circuit #2 with $G_{\mathrm{OFF}} = 0$. Assume that i_{IN1}, i_{IN2} and i_{IN3} each equals 0 when representing the logic value 0, and I_{S} when representing the logic value 1. Derive a truth table for the input-output behavior of the circuit.

(D) Consider Circuit #2 again but with $G_{\mathrm{OFF}} > 0$. Assume that all controlled switches open or close in the same manner as they did in Part (C) for all sets of input currents. Determine the combination of inputs IN1, IN2 and IN3 that results in maximum power dissipation in the circuit.

(E) Consider Circuit #2 again with $G_{\mathrm{OFF}} > 0$. What relation between G_{OFF}, G_{BP}, i_{T} and I_{S} is necessary and sufficient for all controlled switches to open or close in the same manner as they did in Part (C) for all sets of input currents.



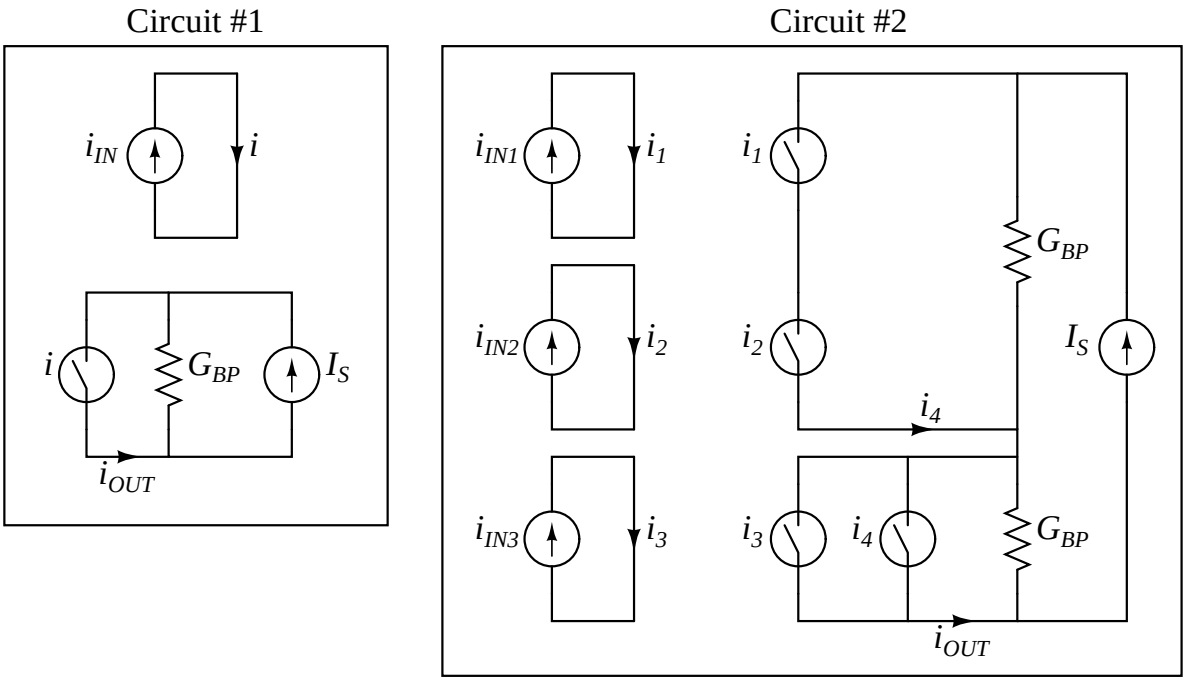


Figure for Problem 3.3