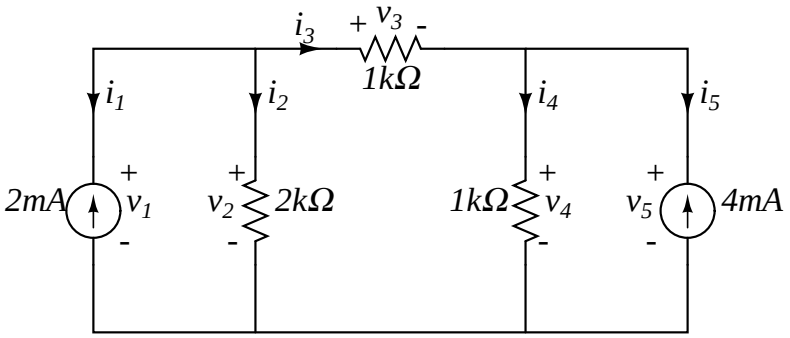
Massachusetts Institute of Technology
Department of Electrical Engineering and Computer Science

6.002 – Electronic Circuits
Spring 2002

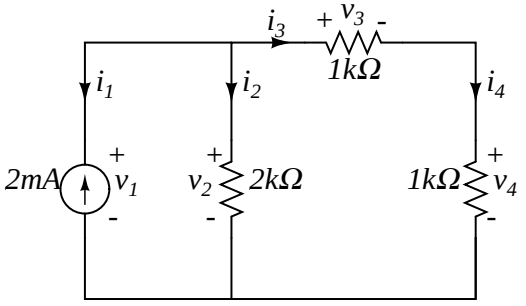
Homework #3 Solutions

Exercise 3.1: Find all branch voltages and all branch currents in the network shown below. Hint: use superposition and other simplifications. Also, find the power dissipated in each network element, and show that the total power dissipated across the network is zero.



Answer: To find the branch voltages and currents, fist use superposition to find the branch currents, and then use the currents to find the branch voltages using the device laws. For the purposes of this solution, i_n represents the total branch current, $i_{n(2mA)}$ represents the contribution from the 2 mA source to i_n, and $i_{n(4mA)}$ represents the contribution from the 4 mA source.

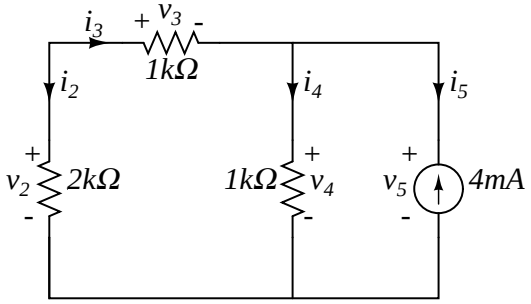
First, remove the 4 mA source from the circuit to get the circuit below. We see immediately that



$i_{3(2mA)} = i_{4(2mA)}$. The resistance in the $i_{2(2mA)}$ and $i_{3,4(2mA)}$ branches are equal, so the 2 mA current splits evenly between the two. The current components from the 2 mA source are then:

$$\begin{array}{lllllllll} i_{1(2mA)} & = & \text{-2 mA}; & i_{3(2mA)} & = & \text{1 mA}; & i_{5(2mA)} & = & \text{0 mA}; \\ i_{2(2mA)} & = & \text{1 mA}; & i_{4(2mA)} & = & \text{1 mA}. & & & \end{array}$$

Next, remove the 2 mA source from the circuit to get the figure below. Again, there is a current divider is formed by the resulting resistor network, with $3k\Omega$ in one branch, and $1k\Omega$ in the other.



Notice that $i_{2(4mA)} = -i_{3(4mA)}$. From the current divider behavior we arrive at the following branch current components:

$$\begin{array}{llllll} i_{1(4mA)} & = & 0 \text{ mA}; & i_{3(4mA)} & = & \text{-1 mA}; \quad i_{5(4mA)} = \text{-4 mA}; \\ i_{2(4mA)} & = & 1 \text{ mA}; & i_{4(4mA)} & = & 3 \text{ mA}. \end{array}$$

Using superposition, we sum the currents contributed by each source for each branch, and find the following total branch currents:

$$\begin{array}{llllll} i_1 & = & \text{-2 mA}; & i_3 & = & 0 \text{ mA}; \quad i_5 = \text{-4 mA}; \\ i_2 & = & 2 \text{ mA}; & i_4 & = & 4 \text{ mA}. \end{array}$$

The device law for a resistor ($V = IR$) is used to find the branch voltages. Note that $v_1 = v_2$ and $v_4 = v_5$, because the corresponding branches are in parallel. Also, because $i_3 = 0$, we should see that $v_3 = 0 \Rightarrow v_1 = v_2 = v_4 = v_5$. Therefore,

$$\begin{array}{llllll} v_1 & = & 4 \text{ V}; & v_3 & = & 0 \text{ V}; \quad v_5 = 4 \text{ V}; \\ v_2 & = & 4 \text{ V}; & v_4 & = & 4 \text{ V}. \end{array}$$

The power dissipated across each element is defined to be the branch current through the element multiplied by the voltage across that element. Therefore,

$$\begin{array}{llllll} P_1 & = & \text{-8 mW}; & P_3 & = & 0 \text{ mW}; \quad P_5 = \text{-16 mW}; \\ P_2 & = & 8 \text{ mW}; & P_4 & = & 16 \text{ mW}. \end{array}$$

Summing these powers shows that the total power dissipated across the network is 0 W. The current sources provide the same power that the resistors dissipate.

Exercise 3.2: When a particular network having a single port is connected to a 2 kΩ resistor, its port voltage is 2 V. When the same network is connected to a 6 kΩ resistor, its port voltage is 3 V. Determine the Thevenin and Norton equivalents of the network.

Answer: These voltage-current pairs must appear on the v-i characteristics of the network; see the graph at the end of the solution. We can equate R_{eq} to the ratio of the incremental change in the terminal voltage divided by the incremental change in the terminal current; ie $\rightarrow R_{eq}$ is just the slope of the v-i line. The currents given in the problem statement are coming *out* of the network which is opposite the definition of current in a Thevenin equivalent circuit so we have to multiply the currents by -1. This gives:

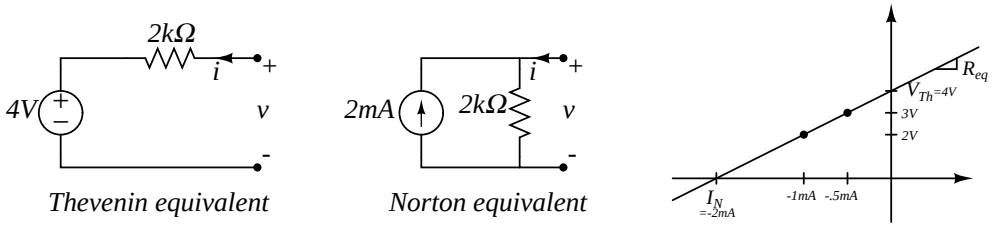
$$R_{eq} = \frac{v_2 - v_1}{i_2 - i_1} = \frac{3V - 2V}{-\frac{3V}{6k\Omega} - (-\frac{2V}{2k\Omega})} = \frac{1V}{.5mA} = 2k\Omega$$

Now, using R_{eq} and the current through one of the test resistors, we can find V_{Th}.

$$\begin{aligned} \frac{V_{Th}}{2k\Omega + R_{eq}} &= 1mA \\ \frac{V_{Th}}{2k\Omega + 2k\Omega} &= 1mA \\ V_{Th} &= 1mA * 4k\Omega \\ V_{Th} &= 4V \end{aligned}$$

The Norton equivalent current, I_N, is just $\frac{V_{Th}}{R_{eq}}$, which is $2mA$.

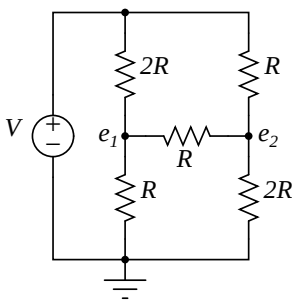
The resulting networks, along with the v-i transfer curve are shown below.



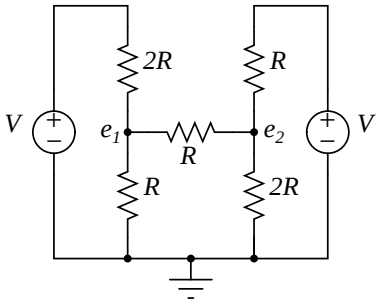
Exercise 3.3: This exercise applies two different analyses to determine the unknown node voltages in Network (A) shown below. It illustrates that the direct method of analysis is not always the simplest.

(A) Use the node method to find the two unknown node voltages in Network (A).

(B) First, explain why Network (A) may be re-drawn as network (B). Second, combine the left source in Network (B) with the two left-most resistors to form their Thevenin equivalent and redraw the resulting network. Third, combine the right source with the two right-most resistors to form their Thevenin equivalent and again redraw the resulting network. Finally, using superposition, determine the two unknown node voltages in the thrice re-drawn version of Network (A) thereby completing the analysis.



Network (A)



Network (B)

Answer:

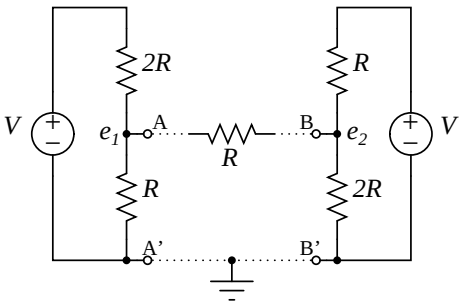
(A) We write KCL at nodes e_1 and e_2 with all currents into the node summing to zero

$$@e_1 \qquad \frac{V-e_1}{2R}+\frac{e_2-e_1}{R}-\frac{e_1}{R}=0 \qquad @e_2 \qquad \frac{V-e_2}{R}+\frac{e_1-e_2}{R}-\frac{e_2}{2R}=0$$

Solving these two equations for the node voltages,

$$e_1=\frac{3}{7}V \qquad \text{and} \qquad e_2=\frac{4}{7}V$$

(B) From the point of view of either node e_1 or e_2, the wire between the top 2R and R resistors just sets that node voltage to V. If we look at network B and write the KCL equations, the results are the same as network A. However, now we can form Thevenin circuits to the left of A-A' and to the right of B-B' below.

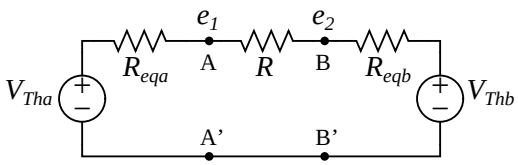


Looking to the left of A-A', V_{TH} can be calculated by using a voltage divider and R_{eq} is just R $\|$ 2R. Similar calculations for the circuit to the right of B-B' yield the following results.

$$V_{Tha}=V/3 \qquad R_{eqa}=2R/3$$

$$V_{Thb}=2V/3 \qquad R_{eqb}=2R/3$$

So our new circuit looks like this



Solving by superposition, if we keep the left source on and turn the right source off:

$$e_1=\frac{R+R_{eqb}}{R_{eqa}+R+R_{eqb}}V_{Tha}$$

$$e_2 = \frac{R_{eqb}}{R_{eqa} + R + R_{eqb}} V_{Tha}$$

and vice versa:

$$e_1 = \frac{R_{eqa}}{R_{eqa} + R + R_{eqb}} V_{Thb}$$

$$e_2 = \frac{R_{eqa} + R}{R_{eqa} + R + R_{eqb}} V_{Thb}$$

Adding the results we get:

$$e_1 = \frac{3}{7} V$$

$$e_2 = \frac{4}{7} V$$

Problem 3.1: This problem examines the operation and design of the digital logic circuit shown below. It is constructed with two identical pull-up resistors and four identical MOSFETs, and it implements the Boolean expression $\text{OUT} = (\text{IN1} \cdot \text{IN2}) + \text{IN3}$. Assume that each MOSFET behaves as a switch with threshold voltage V_{T} and on-state resistance R_{ON}.

(A) Assume that the logic circuit functions properly. For each of the eight input logic value combinations, determine the state (ON or OFF) of the four MOSFETs (M1, M2, M3 and M4), the output logic value, and the voltages at the gate and drain of M4. Organize the results in a table having ten columns: the three input logic values, the output logic value, the four MOSFET states and the two voltages.

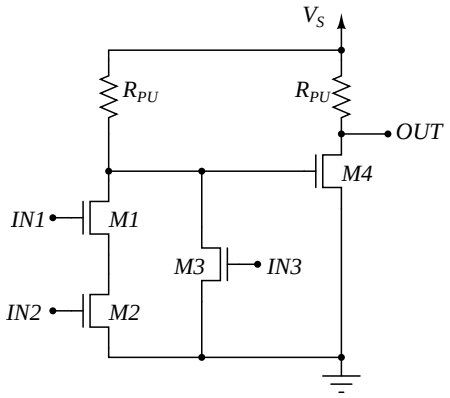
(B) Based on the results of Part (A), what inequalities must V_{T} satisfy so that the voltage at the gate of M4 produces the desired state of M4?

(C) Based on the results of Part (A), what voltage inequalities must be satisfied so that the output voltage at the drain of M4 satisfies the static discipline defined by V_{OH} and V_{OL}?

(D) Assume that the voltages at the three inputs (IN1, IN2 and IN3) satisfy the static discipline defined by V_{IH} and V_{IL}. Based on the results of Part (A), what voltage inequalities must V_{T} satisfy so that the three input voltages produce the desired states of M1, M2 and M3?

(E) Organize the inequalities into a minimal string of inequalities that must be satisfied in order for the digital circuit to function properly and conform to the static discipline.

(F) Assuming that the logic circuit is designed according to the results of Part (E), determine which combinations of input logic values lead to the maximum and minimum power dissipation in the logic circuit.



Answer:

(A) Constructing the table is fairly straightforward. When M1 and M2, or M3 are ON, their respective R_{ON} resistances form a voltage divider with R_{PU} at M4's gate. A voltage divider is also formed at the output terminal when M4 is on. When there isn't a path to ground through the MOSFETs, no current flows through the respective pullup resistors, and the terminal voltages are "pulled up" to V_{S}.

Inputs			MOSFET State				M4 Voltages		
$IN1$	$IN2$	$IN3$	M1	M2	M3	M4	V_G	V_D	OUT
0	0	0	OFF	OFF	OFF	ON	V_{S}	$\frac{R_{\mathrm{ON}}}{R_{\mathrm{ON}}+R_{\mathrm{PU}}}V_{\mathrm{S}}$	0
0	0	1	OFF	OFF	ON	OFF	$\frac{R_{\mathrm{ON}}}{R_{\mathrm{ON}}+R_{\mathrm{PU}}}V_{\mathrm{S}}$	V_{S}	1
0	1	0	OFF	ON	OFF	ON	V_{S}	$\frac{R_{\mathrm{ON}}}{R_{\mathrm{ON}}+R_{\mathrm{PU}}}V_{\mathrm{S}}$	0
0	1	1	OFF	ON	ON	OFF	$\frac{R_{\mathrm{ON}}}{R_{\mathrm{ON}}+R_{\mathrm{PU}}}V_{\mathrm{S}}$	V_{S}	1
1	0	0	ON	OFF	OFF	ON	V_{S}	$\frac{R_{\mathrm{ON}}}{R_{\mathrm{ON}}+R_{\mathrm{PU}}}V_{\mathrm{S}}$	0
1	0	1	ON	OFF	ON	OFF	$\frac{R_{\mathrm{ON}}}{R_{\mathrm{ON}}+R_{\mathrm{PU}}}V_{\mathrm{S}}$	V_{S}	1
1	1	0	ON	ON	OFF	OFF	$\frac{2R_{\mathrm{ON}}}{2R_{\mathrm{ON}}+R_{\mathrm{PU}}}V_{\mathrm{S}}$	V_{S}	1
1	1	1	ON	ON	ON	OFF	$\frac{\frac{2}{3}R_{\mathrm{ON}}}{\frac{2}{3}R_{\mathrm{ON}}+R_{\mathrm{PU}}}V_{\mathrm{S}}$	V_{S}	1

(B) V_{T} must be less than the supply voltage in order for the MOSFETS to turn on properly when V_{S} is applied to their gates. V_{T} must also be greater than the largest logical 0 voltage applied to the gate of M4. This voltage is applied when IN1=IN2=1, and IN3=0. So the two inequalities are:

$$\begin{aligned} V_{\mathrm{T}} &< V_{\mathrm{S}} \\ V_{\mathrm{T}} &> \frac{2R_{\mathrm{ON}}}{2R_{\mathrm{ON}}+R_{\mathrm{PU}}}V_{\mathrm{S}} \end{aligned}$$

(C) The logical 1 output voltage provided by M4 already satisfies the V_{OH} constraint, because $V_{\mathrm{OH}} \leq V_{\mathrm{S}}$. When M4 is turned on (OUT = 0), the output voltage is $V_{\mathrm{S}}\frac{R_{\mathrm{ON}}}{R_{\mathrm{ON}}+R_{\mathrm{PU}}}$, which must be less than V_{OL}. So the inequalities are:

$$\begin{aligned} V_{\mathrm{OH}} &< V_{\mathrm{S}} \\ V_{\mathrm{OL}} &> \frac{R_{\mathrm{ON}}}{R_{\mathrm{ON}}+R_{\mathrm{PU}}}V_{\mathrm{S}} \end{aligned}$$

(D) To satisfy the static discipline for M2 and M3, $V_{\mathrm{T}} > V_{\mathrm{IL}}$, and $V_{\mathrm{T}} < V_{\mathrm{IH}}$. If we look carefully at M1 however, we notice that its source is not connected to ground. When M2 is on and carrying current, its drain (M1's source) is raised above ground by the voltage divider formed by R_{PU} and the R_{ON} of M1 and M2. If V_{IH} is applied to the gate of M1, then M1's $v_{\mathrm{gs}} = V_{\mathrm{IH}} - V_{\mathrm{S}}\frac{R_{\mathrm{ON}}}{2R_{\mathrm{ON}}+R_{\mathrm{PU}}}$. This quantity is less than V_{IH}, and V_{T} must also be less than this for M1 to operate properly. The inequalities are then:

$$V_{\mathrm{T}} > V_{\mathrm{IL}}$$

$$V_T < V_{IH} - V_S \frac{R_{ON}}{2R_{ON} + R_{PU}} < V_{IH}$$

(E) The inequality $V_T < V_S$ from part (B) can be discarded, because we have a tighter restriction from part (D). It is not clear if we can discard the other, because it depends on the relative values of I_L and the second term in inequality from (B). Part (C)'s inequalities must also be preserved, so the full set of inequalities is:

$$\begin{aligned} V_{OH} &< V_S \\ V_{OL} &> \frac{R_{ON}}{R_{ON} + R_{PU}} V_S \\ V_T &> \max\left(\frac{2R_{ON}}{2R_{ON} + R_{PU}} V_S, V_{IL}\right) \\ V_T &< V_{IH} - V_S \frac{R_{ON}}{2R_{ON} + R_{PU}} \end{aligned}$$

(F) The least power is dissipated when there is the most resistance in all paths from power to ground. The most power is dissipated when the lowest resistance is present between power and ground.

If all of the paths on the left side of the circuit (M1 and M2, or M3) are turned off, then M4 is turned on. The total resistance is then $R_{PU} + R_{ON(M4)}$. If both M1 and M2 are turned on, though, M4 is turned off, and $R_{PU} + R_{ON(M1)} + R_{ON(M2)}$ is the only path from V_S to ground. If M3 is left off, this gives the least current flow, and therefore the lowest power dissipation.

Now to find the largest power dissipation, look for the smallest resistance possible from power to ground. The parallel combination of the R_{ON}s from M1, M2, and M3 is much smaller than the R_{ON} of M4. This provides the largest current flow, and therefor the largest power dissipation.

The combination of inputs that lead to these cases are then:

Power	IN1	IN2	IN3
minimum	1	1	0
maximum	1	1	1

Problem 3.2: This problem studies the synthesis of a circuit that implements a two-input exclusive-or gate. The Boolean logic function that the two-input exclusive-or gate provides is $\text{OUT} = (\text{IN1} \cdot \overline{\text{IN2}}) + (\overline{\text{IN1}} \cdot \text{IN2}) = (\text{IN1} + \text{IN2}) \cdot (\overline{\text{IN1} \cdot \text{IN2}})$. Thus, the output is true if one or the other input is true, but not both.

(A) Use truth tables to prove DeMorgan's Law. DeMorgan's Law states that $\overline{\text{A} \cdot \text{B}} = \overline{\text{A}} + \overline{\text{B}}$, and equivalently that $\overline{\text{A} + \text{B}} = \overline{\text{A}} \cdot \overline{\text{B}}$.

(B) Using only inverters and two-input nor gates, synthesize an NMOS circuit that implements the two-input exclusive-or gate. This can be done with as few as eight n-channel MOSFETs and five pull-up resistors. Hint: use DeMorgan's Law.

Answer:

(A) The truth tables for the 4 logic functions are shown below. Notice that $\overline{A \cdot B} = \overline{A} + \overline{B}$, and equivalently that $\overline{A + B} = \overline{A} \cdot \overline{B}$.

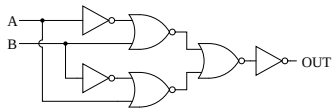
$\overline{A \cdot B}$			=	$\overline{A} + \overline{B}$		
A	B	OUT		A	B	OUT
0	0	1		0	0	1
0	1	1	=	0	1	1
1	0	1		1	0	1
1	1	0		1	1	0

$\overline{A + B}$			=	$\overline{A} \cdot \overline{B}$		
A	B	OUT		A	B	OUT
0	0	1		0	0	1
0	1	0	=	0	1	0
1	0	0		1	0	0
1	1	0		1	1	0

(B) The approach here is to use DeMorgan's Law to substitute (N)OR functions for (N)AND functions. DeMorgan's Law can be rewritten as $A \cdot B = \overline{\overline{A} + \overline{B}}$. Applying this law to both terms of the first form of the given Boolean function yields

$$OUT = \overline{\overline{\overline{IN1} + IN2} + \overline{IN1 + \overline{IN2}}}$$

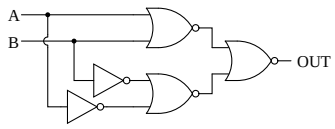
From this it follows that one implementation is:



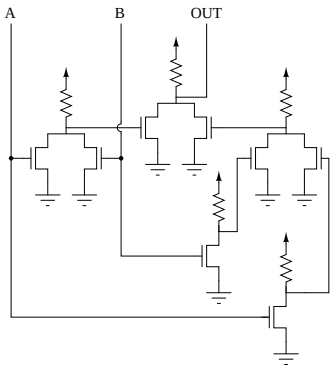
Applying the rewritten form of DeMorgan's Law twice to the second form of the given Boolean function yields

$$OUT = \overline{\overline{\overline{IN1 + IN2} + \overline{\overline{IN1} + \overline{IN2}}}}$$

From this it follows that a second implementation is



This implementation used fewer gates. Its NMOS implementation is



Problem 3.3: This problem examines digital logic circuits in which logic values are represented by positive currents, much like relay logic. Specifically, the logic value 0 is represented by a low-valued current, and the logic value 1 is represented by a high-valued current. The logic circuits are implemented with the current-controlled switch defined below. The switch *opens* when its labeled control current equals or exceeds the threshold current i_{T}, and *closes* otherwise. The control current can be any current in the logic circuit. Note that the switch is imperfect, and has a nonzero off-state conductance, G_{OFF}. Also, assume that i_{T} satisfies $0 < i_{\mathrm{T}} < I_{\mathrm{S}}$, where I_{S} is the supply current.

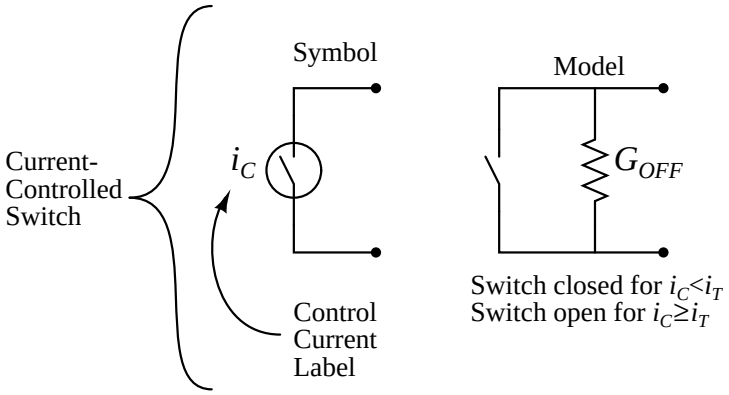
(A) Consider Circuit #1 which is formed with a current-controlled switch, a current supply, and a bypass conductor having conductance G_{BP}. Sketch and clearly label a graph of i_{OUT} as a function of i_{IN} for $0 \leq i_{\mathrm{IN}} \leq I_{\mathrm{S}}$.

(B) Circuit #1 is to satisfy a static discipline defined by I_{L} and I_{H}, where $0 < I_{\mathrm{L}} < I_{\mathrm{H}} < I_{\mathrm{S}}$. That is, for both i_{IN} and i_{OUT}, a valid logic 0 lies between 0 and I_{L}, and a valid logic 1 lies between I_{H} and I_{S}. In this case, within what current range must i_{T} lie, and what is the maximum acceptable value for G_{OFF}?

(C) Consider Circuit #2 with $G_{\mathrm{OFF}} = 0$. Assume that i_{IN1}, i_{IN2} and i_{IN3} each equals 0 when representing the logic value 0, and I_{S} when representing the logic value 1. Derive a truth table for the input-output behavior of the circuit.

(D) Consider Circuit #2 again but with $G_{\mathrm{OFF}} > 0$. Assume that all controlled switches open or close in the same manner as they did in Part (C) for all sets of input currents. Determine the combination of inputs IN1, IN2 and IN3 that results in maximum power dissipation in the circuit.

(E) Consider Circuit #2 again with $G_{\mathrm{OFF}} > 0$. What relation between G_{OFF}, G_{BP}, i_{T} and I_{S} is necessary and sufficient for all controlled switches to open or close in the same manner as they did in Part (C) for all sets of input currents.



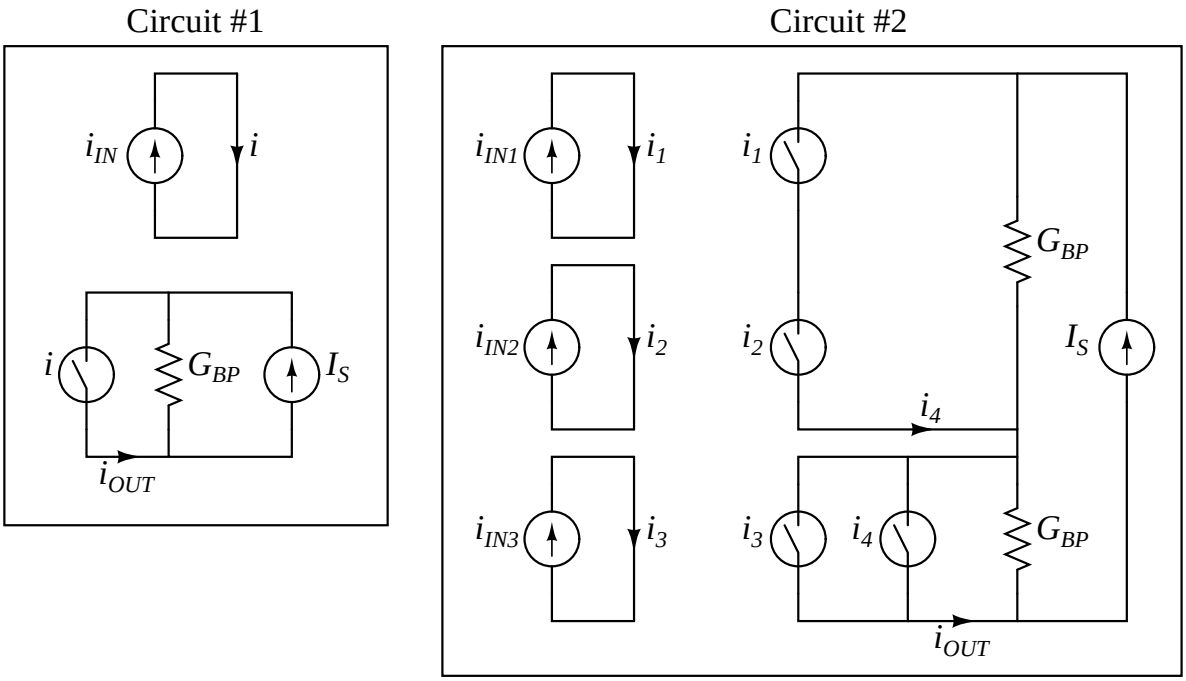
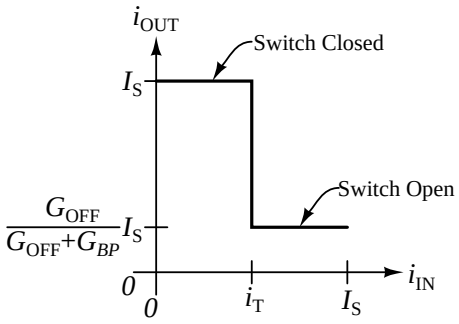


Figure for Problem 3.3

Answer:

(A) The output characteristic of Circuit #1 is graphed below. When $i = i_{\mathrm{IN}} < i_{\mathrm{T}}$ the switch is closed, and shorts out the bypass conductance G_{BP} and the off-state conductance G_{OFF}. All of the current flows through the switch, so $i_{\mathrm{OUT}} = I_{\mathrm{S}}$. When i_{IN} becomes greater than or equal to i_{T}, the switch opens, and a current divider forms between G_{OFF} and G_{BP}. The resulting $i_{\mathrm{OUT}} = \frac{G_{\mathrm{OFF}}}{G_{\mathrm{OFF}}+G_{\mathrm{BP}}} I_{\mathrm{S}}$.



(B) In order to preserve the static discipline, i_{T} must satisfy the inequality $I_{\mathrm{L}} < i_{\mathrm{T}} < I_{\mathrm{H}}$. In addition, we must ensure that the output current of switch satisfies the two inequalities $i_{\mathrm{OUT}} > I_{\mathrm{H}}$ and $i_{\mathrm{OUT}} < I_{\mathrm{L}}$ when the switch is closed and open, respectively. The first equality is already satisfied, as $i_{\mathrm{OUT}} = I_{\mathrm{S}} > I_{\mathrm{H}}$ when the switch is closed. When the switch is open, $i_{\mathrm{OUT}} = \frac{G_{\mathrm{OFF}}}{G_{\mathrm{OFF}}+G_{\mathrm{BP}}} I_{\mathrm{S}}$ as we found in part (A). Making this quantity less than I_{L}, and rearranging some terms, we find:

$$G_{\mathrm{OFF}} < \frac{I_{\mathrm{L}} G_{\mathrm{BP}}}{I_{\mathrm{S}} - I_{\mathrm{L}}}$$

(C) In order for i_{OUT} to be a logical 1 (high-valued current), either switch 3 or 4 must be closed, or either i_3 or i_4 must be a logical 0 to close their respective switches. For i_3 to be a logical 0, i_{IN3} must be a logical 0. For i_4 to be a logical 0, either i_1 or i_2 have to be a logical 1 to open their respective switches. The logic function implemented by this circuit is then: $i_{\mathrm{IN1}} + i_{\mathrm{IN2}} + \overline{i_{\mathrm{IN3}}}$. The truth table is given below.

i_{IN1}	i_{IN2}	i_{IN3}	i_{OUT}
0	0	0	1
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	1

(D) Because the power from the source is given by $P = V_{\mathrm{S}} * I_{\mathrm{S}}$, the largest power dissipation occurs when the smallest conductance is connected across the current source I_S so that V_{S} is largest. Ideally, all the switches should be open in order to avoid shorting any of the conductances. However, if switches 1 and 2 are open, it means that switch 4 is closed, shorting out all of the conductances in the lower half of the circuit. If we turn switch 4 off by closing switches 1 and

2, the conductances in the top half of the circuit are shorted. The total conductance is less in the top half of the circuit because parallel conductances add, while series conductances add as the reciprocal of the sum of their reciprocals. The combination of inputs that produces the lowest conductance, and hence the highest power, is:

$$i_{\mathrm{IN1}} = 1 \quad i_{\mathrm{IN2}} = 1 \quad i_{\mathrm{IN3}} = 0 \text{ or } 1$$

It does not matter whether or not switch 3 is on, because switch 4 is already closed.

(E) The currents i_1,i_2, and i_3 will always satisfy the static discipline provided that $I_{\mathrm{L}} < I_{\mathrm{T}} < I_{\mathrm{H}}$. Therefor it is i_4 that determines the relationship between G_{OFF}, G_{BP}, i_{T}, and I_{S}.

When switches 1 and 2 are closed, i_4 will carry all of I_{S}, because the switches are perfect shorts when closed. When the switches are open, i_4 must be less than I_{T} to ensure that switch 4 is closed. It is not necessary to satisfy the static discipline internally, just at the inputs and outputs of the circuit. The largest conductance in this branch occurs when one of the switches if closed and the other is open. The current divider formed by G_{OFF} and G_{BP} gives $i_4 = I_{\mathrm{S}} \frac{G_{\mathrm{OFF}}}{G_{\mathrm{BP}}+G_{\mathrm{OFF}}}$. With a little algebra we find:

$$\begin{aligned} i_4 = I_{\mathrm{S}} \frac{G_{\mathrm{OFF}}}{G_{\mathrm{BP}} + G_{\mathrm{OFF}}} &< I_{\mathrm{T}} \\ G_{\mathrm{OFF}} &< \frac{I_{\mathrm{T}} G_{\mathrm{BP}}}{I_{\mathrm{S}} - I_{\mathrm{T}}} \end{aligned}$$

Not needing to adhere to the static discipline internally was not covered in lecture. To satisfy the static discipline everywhere, i_4 must be less than I_{L}. The resulting restriction on G_{OFF} is:

$$G_{\mathrm{OFF}} < \frac{I_{\mathrm{L}} G_{\mathrm{BP}}}{I_{\mathrm{S}} - I_{\mathrm{L}}}$$

The problem didn't specify that we ensure i_{OUT} also satisfies the static discipline defined by I_{L} and I_{H}. To use this particular circuit with others like it, we need to ensure that i_{OUT} does satisfy the static discipline. The maximum G_{OFF} conductance in parallel with G_{BP} is 2 times larger on the bottom half of the circuit than on the top half. That is $i_{\mathrm{OUT}} = I_{\mathrm{S}} \frac{2G_{\mathrm{OFF}}}{G_{\mathrm{BP}}+2G_{\mathrm{OFF}}}$ The resulting constraint is then:

$$G_{\mathrm{OFF}} < \frac{I_{\mathrm{L}} G_{\mathrm{BP}}}{2(I_{\mathrm{S}} - I_{\mathrm{L}})}$$