Massachusetts Institute of Technology
Department of Electrical Engineering and Computer Science

6.002 – Electronic Circuits
Spring 2002

Homework #4

Issued 2/27/02 – Due 3/6/02

Exercise 4.1:   Consider the logic circuit that implements OUT $= \overline{\text{IN1} + \overline{(\text{IN2} \cdot \overline{\text{IN3}})}}$. Express OUT as a function of IN1, IN2 and IN3 in the form of a truth table. Also, implement this logic circuit using logic symbols, and using a small number of n-channel MOSFETs and pull-up resistors.

Exercise 4.2:   A Norton equivalent network is used to excite a nonlinear resistor as shown below. The graphical i-v characteristic that defines the nonlinear resistor is also shown below. Determine the terminal current i_{NR} and the terminal voltage v_{NR} of the nonlinear resistor for all values of I_{N}. Hint: consider using load-line analysis to gain insight.
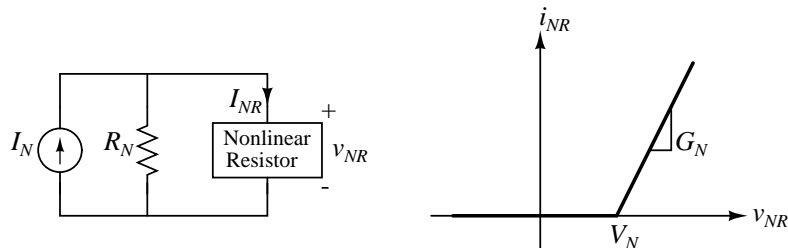

Problem 4.1:   Following the node method, develop a set of simultaneous equations for the networks shown below that can be solved to determine the unknown node voltages. Express the set of equations in the form

$$G \begin{bmatrix} e_1 \\ e_2 \\ e_3 \end{bmatrix} = S$$

where G is a 3×3 array of conductance terms and S is a 3×1 vector of terms involving the *independent* sources. You need not solve the set of equations for the node voltages.
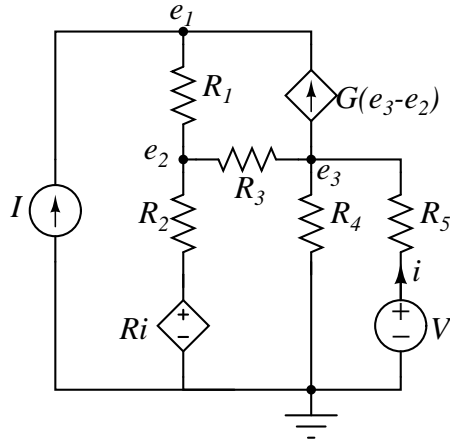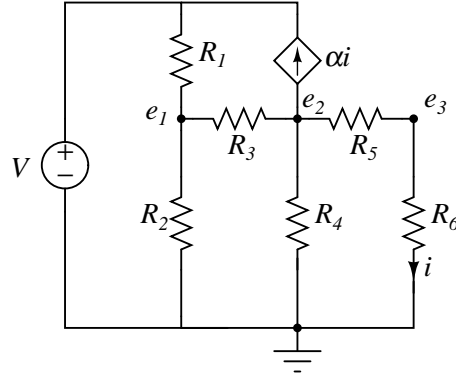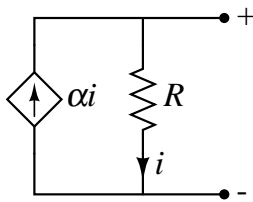
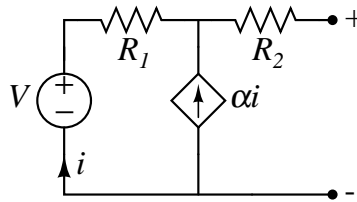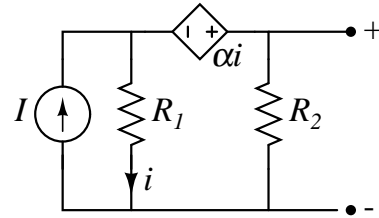Network (A)   Network (B)

Problem 4.2:   Determine the Thevenin equivalent of each network shown below. Note that these networks contain dependent sources.

Network (A)   Network (B)   Network (C)
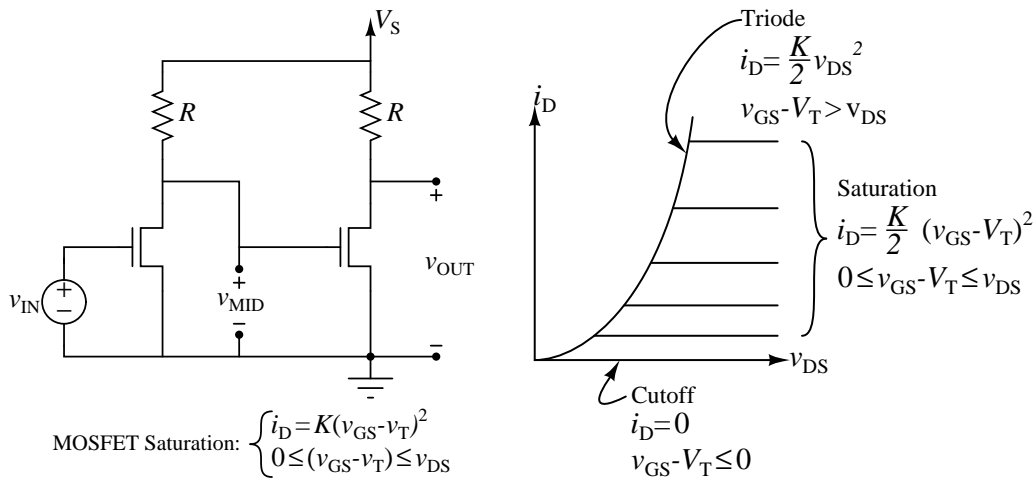
Problem 4.3:   This problem studies the two-stage n-channel MOSFET amplifier shown below. The two stages are built with identical MOSFETs and pull-up resistors. A simplified model for the MOSFET is also given below. The simplification is that the triode region of operation is compressed onto the curve $i_\mathrm{D} = Kv_\mathrm{DS}^2/2$, which becomes a common curve of operation for $v_\mathrm{GS} - V_\mathrm{T} > v_\mathrm{DS}$. Hint a load-line analysis may help solve this problem.

(A) Determine the range of v_IN over which MOSFET M1 operates in cutoff. Also, determine v_MID for this operating range.

(B) Assuming that MOSFET M1 operates in its saturation region, determine v_MID as a function of v_IN. Also, determine the range of v_MID and the range of v_IN that correspond to the saturated operation of MOSFET M1.

(C) For values of v_IN that are above the range found in Part (B), MOSFET M1 operates in its triode region, which in the model below is compressed onto the curve $i_\mathrm{D} = Kv_\mathrm{DS}^2/2$. Determine v_MID for v_IN in this range of operation.

(D) Using the results of Parts (A), (B) and (C), determine v_OUT as a function of v_MID for the cutoff, saturation and triode regions of operation of MOSFET M2. For each region, state the corresponding operating range of v_MID and v_OUT.

(E) Assuming that both MOSFETs operate in their saturation regions, determine v_OUT as a function of v_IN. Also, determine the range of v_MID and then the corresponding range of v_IN over

which both MOSFETs operate in their saturation regions.

(F) Determine the small-signal gain of the amplifier as a function of the operating-point input V_{IN} assuming that this operating point falls within the range found in Part (E). That is, determine $dv_{\text{OUT}}/dv_{\text{IN}}$ evaluated at V_{IN}.

(G) Let $K = 0.02$ A/V^2, $R_{\text{D}} = 1$ kΩ, $V_{\text{S}} = 10$V and $V_{\text{T}} = 1$ V. Plot v_{MID} as a function of v_{IN} for $0 \leq v_{\text{IN}} \leq 3$ V. On the same graph, plot v_{OUT} as a function of v_{IN} over the same range of v_{IN}. Hint: this is particularly simple if you are familiar with MatLab on Athena. Observe the differences of the two plots.

Save a copy of your solutions to help with Homework #5.

MOSFET Saturation: $\begin{cases} i_{\text{D}} = K(v_{\text{GS}} - v_{\text{T}})^2 \\ 0 \leq (v_{\text{GS}} - v_{\text{T}}) \leq v_{\text{DS}} \end{cases}$

Problem 4.4: An NPN bipolar junction transistor (NPN BJT) is a three-terminal device. Its terminals are referred to as the base, the collector and the emitter. The symbol for the NPN BJT is shown below, along with the voltage and current definitions for this BJT when it is viewed as a two-port device. Here, the Base-Emitter port acts as a control port and the Collector-Emitter port acts as a power port, much like the Gate-Source and Drain-Source ports of an n-channel MOSFET, respectively.

Figures 1 and 2 below describe the *greatly* idealized behavior of an NPN BJT in terms of its port variables. Figure 1 describes the behavior of the control port, and shows how i_{B} is related to v_{BE}. Figure 2 describes the behavior of the power port, and shows how i_{C} is related to v_{CE} for various values of i_{B}. In general, for $i_{\text{B}} > 0$ and $v_{\text{CE}} > 0$, $i_{\text{C}} = \beta i_{\text{B}}$ where β is a gain constant.

This problem investigates the use of the NPN BJT described by Figures 1 and 2 to construct an amplifier. The amplifier is shown in Figure 3. Assume that $V_{\text{S}} > V_{\text{D}}$.

(A) Determine i_{B} as a function of v_{IN}. Sketch and clearly label the result. Hint: a load-line analysis might provide useful insight given the nonlinear behavior shown in Figure 1.

(B) Determine v_{OUT} as a function of i_{B}; note that $v_{\text{OUT}} = v_{\text{CE}}$ for the amplifier shown in Figure 3. Sketch and clearly label the result. Hint: a load-line analysis might provide useful insight given the nonlinear behavior shown in Figure 2.

(C) Combine the results of Parts (A) and (B) to determine v_{OUT} as a function of v_{IN}. Sketch and
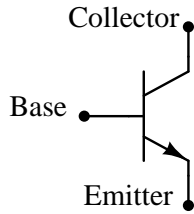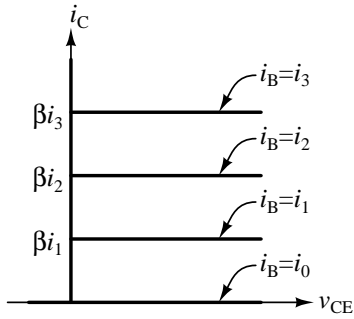
clearly label the result.

Symbol

Collector

Base

Emitter

Two-Port Definitions

i_C +

v_{CE}

+

v_{BE} i_B

-

Figure 1

i_B

V_D v_{BE}

Figure 2

i_C

βi_3 $i_B = i_3$

βi_2 $i_B = i_2$

βi_1 $i_B = i_1$

$i_B = i_0$

v_{CE}

Figure 3

R_C

V_S

R_B

+

v_{IN}

v_{OUT}

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