Massachusetts Institute of Technology
Department of Electrical Engineering and Computer Science

6.002 – Electronic Circuits
Spring 2002

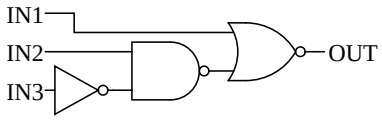
Homework #4 Solutions

Exercise 4.1: Consider the logic circuit that implements $\text{OUT} = \overline{\text{IN1} + \overline{(\text{IN2} \cdot \overline{\text{IN3}})}}$. Express OUT as a function of IN1, IN2 and IN3 in the form of a truth table. Also, implement this logic circuit using logic symbols, and using a small number of n-channel MOSFETs and pull-up resistors.

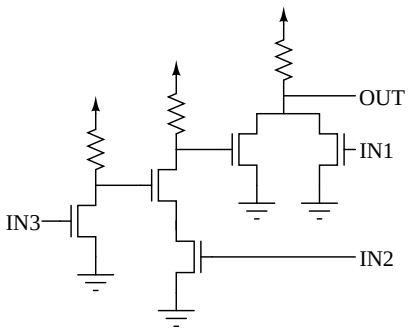
Answer: To write out the truth table, it is easiest to first use DeMorgan's Law to rewrite the expression in the following form $\text{OUT} = \overline{\text{IN1} + \overline{\text{IN2}} + \text{IN3}}$. This always evaluates to a logical zero except when all the terms in the OR are logical 0s. The truth table is

IN1	IN2	IN3	OUT
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	0

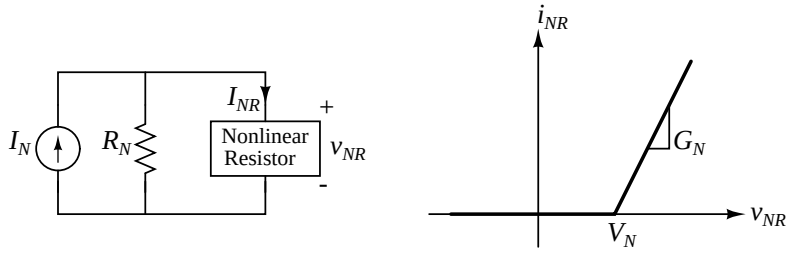
The circuit that implements this can be easily built with one 2-input NOR gate, one 2-input NAND gate, and one inverter, directly from the expression. The logic symbol implementation is



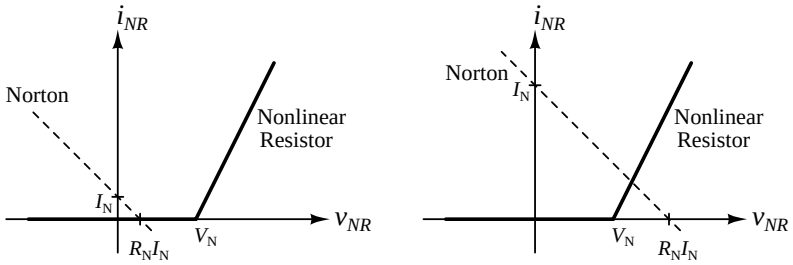
Replacing the logic symbols with their NMOS logic counterparts gives the circuit



Exercise 4.2: A Norton equivalent network is used to excite a nonlinear resistor as shown below. The graphical i-v characteristic that defines the nonlinear resistor is also shown below. Determine the terminal current $i_{\rm NR}$ and the terminal voltage $v_{\rm NR}$ of the nonlinear resistor for all values of $I_{\rm N}$. Hint: consider using load-line analysis to gain insight.



Answer: Consider using load line analysis. There are two different cases, one when $R_{\rm N}I_{\rm N} \leq V_{\rm N}$ and one when $R_{\rm N}I_{\rm N} \geq V_{\rm N}$. The load lines are draw in the figure below



$R_{\rm N}I_{\rm N} \leq V_{\rm N}$ $\qquad$ $R_{\rm N}I_{\rm N} \geq V_{\rm N}$

Now continue with the math. The first case, when $R_{\rm N}I_{\rm N} \leq V_{\rm N}$, is easy: $i_{\rm NR} = 0$ so $v_{\rm NR} = R_{\rm N}I_{\rm N}$. The second case is the non trivial one. The current through the nonlinear resistor is proportional to $v_{\rm NR} - V_{\rm N} \Rightarrow i_{\rm NR} = G_{\rm N}(v_{\rm NR} - V_{\rm N})$. Writing KCL at the positive terminal of the nonlinear resistor yields $0 = -I_{\rm N} + \frac{v_{\rm NR}}{R_{\rm N}} + G_{\rm N}(v_{\rm NR} - V_{\rm N})$. Solving for $v_{\rm NR}$ gives

$$v_{\rm NR} = \frac{I_{\rm N} + V_{\rm N}G_{\rm N}}{\frac{1}{R_{\rm N}} + G_{\rm N}} \quad \text{when} \quad R_{\rm N}I_{\rm N} \geq V_{\rm N}$$

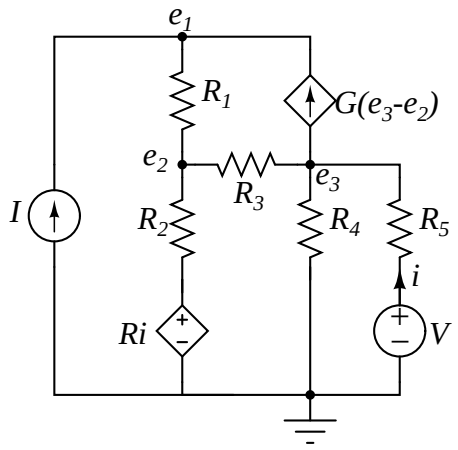
Substituting in the expression for $i_{\rm NR}$ in terms of $v_{\rm NR}$ above, we find

$$i_{\rm NR} = \frac{R_{\rm N}I_{\rm N} - V_{\rm N}}{\frac{1}{G_{\rm N}} + 1} \quad \text{when} \quad R_{\rm N}I_{\rm N} \geq V_{\rm N}$$

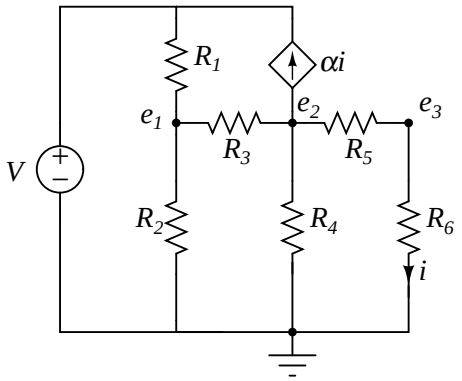
Problem 4.1: Following the node method, develop a set of simultaneous equations for the networks shown below that can be solved to determine the unknown node voltages. Express the set of equations in the form

$$G \begin{bmatrix} e_1 \\ e_2 \\ e_3 \end{bmatrix} = S$$

where G is a 3×3 array of conductance terms and S is a 3×1 vector of terms involving the *independent* sources. You need not solve the set of equations for the node voltages.



Network (A)



Network (B)

Answer: We develop our conduction matrix by performing KCL at the nodes having unknown voltages: e_1, e_2, and e_3. As always, we are given the choice of summing currents entering or leaving the node. For this problem, we will be setting the sum of the currents *leaving* the node to zero.

Network (A)

For Network (A), we apply KCL to the nodes at which the unknown node voltages are defined. At e_1:

$$G_1(e_1 - e_2) - I - G(e_3 - e_2) = 0$$

At e_2:

$$G_1(e_2 - e_1) + G_2(e_2 - Ri) + G_3(e_2 - e_3) = 0$$

We can relate i to the node voltages and conductances:

$$i = G_5(V - e_3)$$

which we can substitute into the KCL equation at e_2:

$$G_1(e_2 - e_1) + G_2(e_2 - RG_5(V - e_3)) + G_3(e_2 - e_3) = 0$$

Finally, at e_3

$$G_3(e_3 - e_2) + G_4(e_3 - 0) + G(e_3 - e_2) + G_5(e_3 - V) = 0$$

We can now put the three KCL equations in a standard form:

$$e_1(G_1) + e_2(G - G_1) + e_3(-G) = I$$

$$e_1(-G_1) + e_2(G_1 + G_2 + G_3) + e_3(G_2RG_5 - G_3) = G_2RG_5V$$

$$e_1(0) + e_2(-G_3 - G) + e_3(G_3 + G_4 + G + G_5) = G_5V$$

This can be easily formatted to yield the conduction matrix:

$$\begin{bmatrix} G_1 & G - G_1 & -G \\ -G_1 & G_1 + G_2 + G_3 & G_2G_5R - G_3 \\ 0 & -G_3 - G & G + G_3 + G_4 + G_5 \end{bmatrix} \begin{bmatrix} e_1 \\ e_2 \\ e_3 \end{bmatrix} = \begin{bmatrix} I \\ G_2G_5RV \\ G_5V \end{bmatrix}$$

Network (B)

Similarly, for Network (B), we apply KCL to the nodes at which the unknown node voltages are defined. At e_1:

$$G_1(e_1 - V) + G_2(e_1 - 0) + G_3(e_1 - e_2) = 0$$

At e_2:

$$G_3(e_2 - e_1) + G_4(e_2 - 0) + G_5(e_2 - e_3) + \alpha i = 0$$

We can relate i to the node voltages and conductances:

$$i = G_6(e_3 - 0)$$

which we can substitute into in the KCL equation at e_2:

$$G_3(e_3 - e_1) + G_4(e_2 - 0) + G_5(e_2 - e_3) + \alpha G_6(e_3 - 0) = 0$$

Finally, at e_3:

$$G_5(e_3 - e_2) + G_6(e_3 - 0) = 0$$

We can now put the three KCL equations in a standard form:

$$e_1(G_1 + G_2 + G_3) + e_2(-G_3) + e_3(0) = VG_1$$

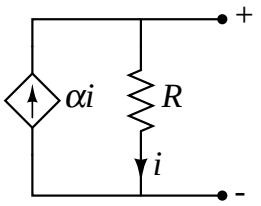
$$e_1(-G_3) + e_2(G_3 + G_4 + G_5) + e_3(-G_5 + G_6) = 0$$

$$e_1(0) + e_2(-G_5) + e_3(G_5 + G_6) = 0$$

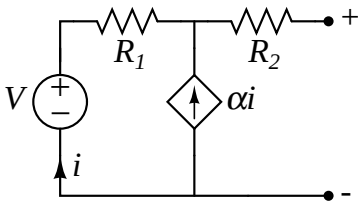
This can be easily formatted to yield the conduction matrix:

$$\begin{bmatrix} G_1 + G_2 + G_3 & -G_3 & 0 \\ -G_3 & G_3 + G_4 + G_5 & -G_5 + \alpha G_6 \\ 0 & -G_5 & G_5 + G_6 \end{bmatrix} \begin{bmatrix} e_1 \\ e_2 \\ e_3 \end{bmatrix} = \begin{bmatrix} VG_1 \\ 0 \\ 0 \end{bmatrix}$$

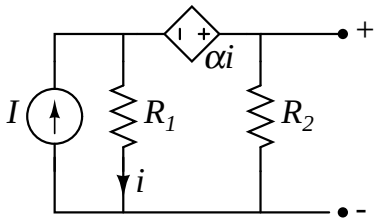
Problem 4.2: Determine the Thevenin equivalent of each network shown below. Note that these networks contain dependent sources.



Network (A)



Network (B)

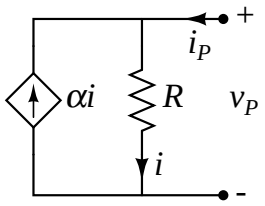


Network (C)

Answer:

Network (A)

To find the Thevenin equivalent circuit, we perform nodal analysis, given a value of v_{P} and i_{P} at the output ports, as labeled in the circuit below.



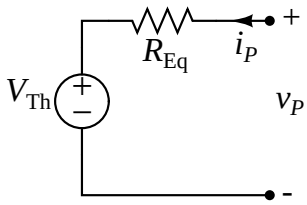
Note that i and i_{P} in the figure are not the same currents. Ultimately, we wish to find a function relating i_{P} and v_{P} in terms of the resistor R and the characteristic coefficient α. The voltage v_{P} is equal to the voltage drop across the resistor R, which means $v_{\mathrm{P}} = Ri$. Writing KCL at the top node of the circuit give

$$\alpha i - i + i_{\mathrm{P}} = 0$$

Solving for i and using the relation $i = \frac{v_{\mathrm{P}}}{R}$, we find:

$$i_{\mathrm{P}} = \frac{1-\alpha}{R} v_{\mathrm{P}}$$

Consider the general Thevenin equivalent circuit below.



Solving for v_{P} and i_{P} using $V = IR$ produces:

$$v_{\mathrm{P}} - V_{\mathrm{Th}} = R_{\mathrm{eq}} i_{\mathrm{P}}$$

or

$$i_{\mathrm{P}} = \frac{1}{R_{\mathrm{eq}}} \cdot v_{\mathrm{P}} - \frac{V_{\mathrm{Th}}}{R_{\mathrm{eq}}.}$$

This function has to be equivalent to the one we found for the dependent source circuit because the Thevenin equivalent circuit has the same v-i relationship at its terminals, by definition. This empowers us to relate coefficients in the two equations. We know that the coefficients of the v_{P} term in each equation must be the same if the circuits are to be equivalent:

$$\frac{1}{R_{eq}} = \frac{1-\alpha}{R}$$

which gives us:

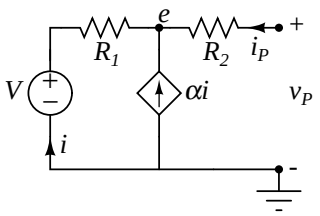
$$R_{\mathrm{eq}} = \frac{R}{1-\alpha}$$

There is no constant term in our equation for i_{P}, which means

$$V_{\mathrm{Th}} = 0$$

Network (B)

Again, to find the Thevenin equivalent circuit, we perform nodal analysis, given a value of v_{P} and i_{P} at the output ports, as labeled in the circuit below.



Again, we want to find an equation relating i_{P} and v_{P} in terms of the voltage source, V, the resistors, R_1 and R_2, and the characteristic coefficient, α. First, we designate a ground node which allows us to define the node voltage, e, as shown on the above figure. Performing KCL on the currents *entering* the node e, we get:

$$i + \alpha i + i_{\mathrm{P}} = 0$$

We can use $V = IR$ to obtain the additional relationships:

$$\frac{V - e}{R_1} = i$$

and

$$\frac{v_{\mathrm{P}} - e}{R_2} = i_{\mathrm{P}} \Rightarrow e = v_{\mathrm{P}} - i_{\mathrm{P}} R_2$$

Substituting these two equations into the original one above gives us an equation relating i_{P} and v_{P}:

$$i_{\mathrm{P}} = \frac{1}{\frac{R_1}{1+\alpha} + R_2} \cdot v_{\mathrm{P}} - \frac{V}{\frac{R_1}{1+\alpha} + R_2}$$

Now we can use the result from part (A) expressing i_{P} in terms of v_{P} in the Thevenin equivalent circuit to relate coefficients again to find V_{Th} and R_{Eq}.

We know that the coefficients of the v_{P} term in each equation must be the same if the circuits are to be equivalent:

$$\frac{1}{R_{\mathrm{eq}}} = \frac{1}{\frac{R_1}{1+\alpha} + R_2}$$

which gives us:

$$R_{\mathrm{eq}} = \frac{R_1}{1+\alpha} + R_2$$

Similarly, we know that constant terms in both equations must be equivalent:

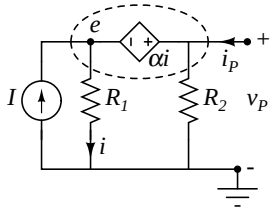
$$\frac{V_{\mathrm{Th}}}{R_{\mathrm{eq}}} = \frac{V}{\frac{R_1}{1+\alpha} + R_2}$$

Solving for V_{Th}, we get:

$$V_{\mathrm{Th}} = V$$

Network (C)

Again, we follow the same method as for the other two networks. We define a ground node, node voltages, and a port voltage and current as in the figure below.



Notice that the voltage e at the left node is just $v_\mathrm{P} - \alpha i$. The area enclosed by the dotted line in the figure above can be considered a supernode. Writing KCL for the currents leaving that node gives:

$$-i_\mathrm{P} + \frac{v_\mathrm{P}}{R_2} + i - I = 0$$

From $V = IR$ we can write

$$i = \frac{v_\mathrm{P} - \alpha i}{R_1}$$

We can rewrite this to find i as a function of v_P

$$i = \frac{v_\mathrm{P}}{R_1 + \alpha}$$

This can be substituted into the KCL expression above to find:

$$i_\mathrm{P} = \left(\frac{1}{R_2} + \frac{1}{R_1 + \alpha}\right) v_\mathrm{P} - I$$

Again we can use the fact that this equation must be equivalent to the Thevenin circuit equation

$$i_\mathrm{P} = \frac{1}{R_\mathrm{eq}} \cdot v_\mathrm{P} - \frac{V_\mathrm{Th}}{R_\mathrm{eq}}.$$

From this we find:

$$R_\mathrm{eq} = \left(\frac{1}{R_2} + \frac{1}{R_1 + \alpha}\right)^{-1} = (R_1 + \alpha)||R_2$$

$$V_\mathrm{Th} = I \cdot ((R_1 + \alpha)||R_2)$$

Problem 4.3: This problem studies the two-stage n-channel MOSFET amplifier shown below. The two stages are built with identical MOSFETs and pull-up resistors. A simplified model for the MOSFET is also given below. The simplification is that the triode region of operation is compressed onto the curve $i_D = Kv_{DS}^2/2$, which becomes a common curve of operation for $v_{GS} - V_T > v_{DS}$. Hint a load-line analysis may help solve this problem.

(A) Determine the range of v_{IN} over which MOSFET M1 operates in cutoff. Also, determine v_{MID} for this operating range.

(B) Assuming that MOSFET M1 operates in its saturation region, determine v_{MID} as a function of v_{IN}. Also, determine the range of v_{MID} and the range of v_{IN} that correspond to the saturated operation of MOSFET M1.

(C) For values of v_{IN} that are above the range found in Part (B), MOSFET M1 operates in its triode region, which in the model below is compressed onto the curve $i_D = Kv_{DS}^2/2$. Determine v_{MID} for v_{IN} in this range of operation.

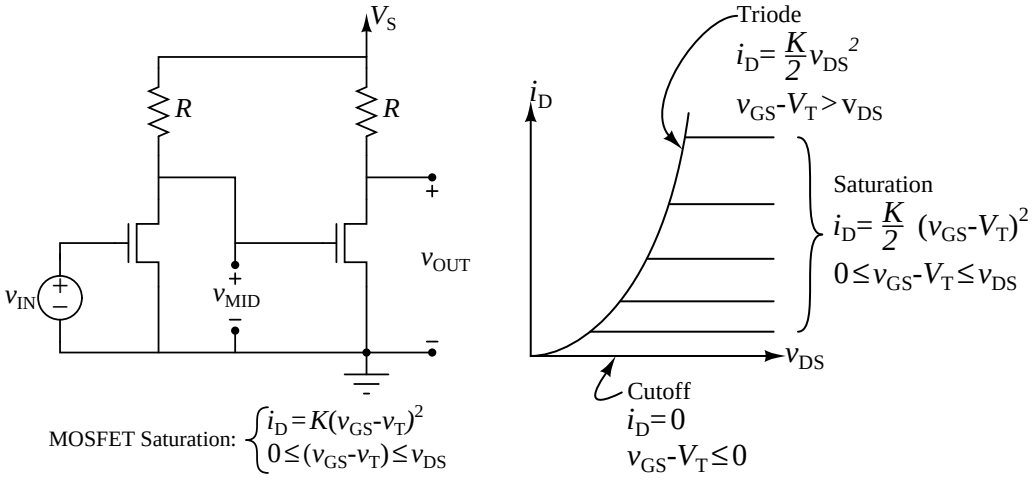
(D) Using the results of Parts (A), (B) and (C), determine v_{OUT} as a function of v_{MID} for the cutoff, saturation and triode regions of operation of MOSFET M2. For each region, state the corresponding operating range of v_{MID} and v_{OUT}.

(E) Assuming that both MOSFETs operate in their saturation regions, determine v_{OUT} as a function of v_{IN}. Also, determine the range of v_{MID} and then the corresponding range of v_{IN} over which both MOSFETs operate in their saturation regions.

(F) Determine the small-signal gain of the amplifier as a function of the operating-point input V_{IN} assuming that this operating point falls within the range found in Part (E). That is, determine dv_{OUT}/dv_{IN} evaluated at V_{IN}.

(G) Let $K = 0.02$ A/V^2, $R_D = 1$ kΩ, $V_S = 10$V and $V_T = 1$ V. Plot v_{MID} as a function of v_{IN} for $0 \le v_{IN} \le 3$ V. On the same graph, plot v_{OUT} as a function of v_{IN} over the same range of v_{IN}. Hint: this is particularly simple if you are familiar with MatLab on Athena. Observe the differences of the two plots.

Save a copy of your solutions to help with Homework #5.



Answer:

(A) For MOSFET M1, $v_{GS} = v_{IN}$. The MOSFET operates in the cutoff region for $v_{GS} - V_T < 0$. This means that M1 is in cutoff for $v_{IN} < V_T$. When M1 is in cutoff, $i_D = 0$. With no current through the pull-up resistor, $v_{MID} = V_S$.

(B) For the first MOSFET, we have $v_{MID} = v_{DS}$ and $v_{IN} = v_{GS}$. Also, we can write $(V_S - v_{MID}) = i_D R$. Setting this value for i_D equal to the expression for i_D when the MOSFET is in saturation gives the following equation:

$$V_S - v_{MID} = \frac{RK}{2}(v_{IN} - v_T)^2$$

or

$$v_{MID} = V_S - \frac{RK}{2}(v_{IN} - v_T)^2$$

For MOSFET M1 to be operating in its saturation regime, the inequality $v_{MID} \geq v_{IN} - V_T$ must be satisfied. When $v_{MID} = v_{IN} - V_T$, M1 leaves the saturation region, and enters the triode region. When $0 = v_{IN} - V_T$, M1 leaves the saturation region and enters the cutoff region. Finding v_{IN} corresponding to the triode/saturation region border is a matter of solving the quadratic equation

$$v_{IN} - V_T = V_S - \frac{RK}{2}(v_{IN} - V_T)^2$$

To simplify the math, we'll solve this for $v_{IN} - V_T$, and just add V_T to the result to find v_{IN}. Using the quadratic formula, we find

$$v_{IN} = \frac{-1 + \sqrt{1 + 2RKV_S}}{RK} + V_T$$

The positive sign was chosen for the square root term in order to ensure that $v_{IN} - V_T > 0$. The analysis of the cutoff/saturation region border is taken from Part (A). The ranges for v_{MID} and v_{IN} for which M1 is in the saturation regime are then

$$V_T \leq v_{IN} \leq \frac{-1 + \sqrt{1 + 2RKV_S}}{RK} + V_T$$

$$\frac{-1 + \sqrt{1 + 2RKV_S}}{RK} \leq v_{MID} \leq V_S$$

(C) We know from above that $v_{MID} = V_S - R \cdot i_D$. The v_{DS} of M1 is v_{MID}, so we can rewrite this equation as:

$$v_{MID} = V_S - \frac{RK}{2} v_{MID}^2$$

Using the quadratic formula to solve this equation for v_{MID} gives:

$$v_{MID} = \frac{-1 + \sqrt{1 + 2RKV_S}}{RK}$$

Note that this is the lower bound for v_{MID} found in Part (B).

(D) The two amplifier stages are identical, which means that the input-output charecteristics of both stages will be identical. The answers from parts (A), (B), and (C) can be reused. Replace v_{IN} with v_{MID} and v_{MID} with v_{OUT} to obtain:

Cutoff	
Input Range	$v_{\mathrm{MID}} - V_{\mathrm{T}} < 0$
Output Range	$v_{\mathrm{OUT}} = V_{\mathrm{S}}$

Saturation	
Input Range	$0 \leq v_{\mathrm{MID}} - V_{\mathrm{T}} \leq \frac{-1+\sqrt{1+2RKV_{\mathrm{S}}}}{RK}$
Output Range	$\frac{-1+\sqrt{1+2RKV_{\mathrm{S}}}}{RK} \leq v_{\mathrm{OUT}} \leq V_{\mathrm{S}}$
Output Function	$v_{\mathrm{OUT}} = V_{\mathrm{S}} - \frac{RK}{2}(v_{\mathrm{MID}} - V_{\mathrm{T}})^2$

In Triode	
Input Range	$v_{\mathrm{MID}} - V_{\mathrm{T}} > \frac{-1+\sqrt{1+2RKV_{\mathrm{S}}}}{RK}$
Output Range	$v_{\mathrm{OUT}} = \frac{-1+\sqrt{1+2RKV_{\mathrm{S}}}}{RK}$

(E) With both MOSFETS in their saturation regimes, we know that $v_{\mathrm{MID}} = V_{\mathrm{S}} - \frac{RK}{2}(v_{\mathrm{IN}} - V_{\mathrm{T}})^2$ and $v_{\mathrm{OUT}} = V_{\mathrm{S}} - \frac{RK}{2}(v_{\mathrm{MID}} - V_{\mathrm{T}})^2$. These two equations can be combined to yield:

$$v_{\mathrm{OUT}} = V_{\mathrm{S}} - \frac{RK}{2}(V_{\mathrm{S}} - V_{\mathrm{T}} - \frac{RK}{2}(v_{\mathrm{IN}} - V_{\mathrm{T}})^2)^2$$

From part (D), we know that for MOSFET M2 to be in the saturation regime, $0 \leq v_{\mathrm{MID}} - V_{\mathrm{T}} \leq \frac{-1+\sqrt{1+2RKV_{\mathrm{S}}}}{RK}$. From part B, we know that while M1 is in the saturation regime, $\frac{-1+\sqrt{1+2RKV_{\mathrm{S}}}}{RK} \leq v_{\mathrm{MID}} \leq V_{\mathrm{S}}$, and $0 \leq v_{\mathrm{IN}} - V_{\mathrm{T}} \leq \frac{-1+\sqrt{1+2RKV_{\mathrm{S}}}}{RK}$. The tightest restrictions on v_{MID} are then:

$$\max\left(V_{\mathrm{T}}, \frac{-1+\sqrt{1+2RKV_{\mathrm{S}}}}{RK}\right) \leq v_{\mathrm{MID}} \leq \min\left(V_{\mathrm{S}}, \frac{-1+\sqrt{1+2RKV_{\mathrm{S}}}}{RK} + V_{\mathrm{T}}\right)$$

For the purposes of this solution (and the numbers given in part (G)), we will consider this to reduce to:

$$V_{\mathrm{T}} \leq v_{\mathrm{MID}} \leq \frac{-1+\sqrt{1+2RKV_{\mathrm{S}}}}{RK} + V_{\mathrm{T}}$$

Using the expression we found in part (A) for v_{MID} as a function of v_{IN}, we find that:

$$V_{\mathrm{T}} + \sqrt{\frac{2}{RK}(V_{\mathrm{S}} - V_{\mathrm{T}})} \geq v_{\mathrm{IN}} \geq V_{\mathrm{T}} + \sqrt{\frac{2}{RK}\left(V_{\mathrm{S}} - V_{\mathrm{T}} - \frac{-1+\sqrt{1+2RKV_{\mathrm{S}}}}{RK}\right)}$$

(F) We know that $V_{\mathrm{OUT}} = V_{\mathrm{S}} - \frac{RK}{2}(v_{\mathrm{MID}} - V_{\mathrm{T}})^2$. Using the chain rule, we can write:

$$\frac{dv_{\mathrm{OUT}}}{dv_{\mathrm{IN}}} = -RK(V_{\mathrm{MID}} - V_{\mathrm{T}})\frac{dv_{\mathrm{MID}}}{dv_{\mathrm{IN}}}$$

Likewise:

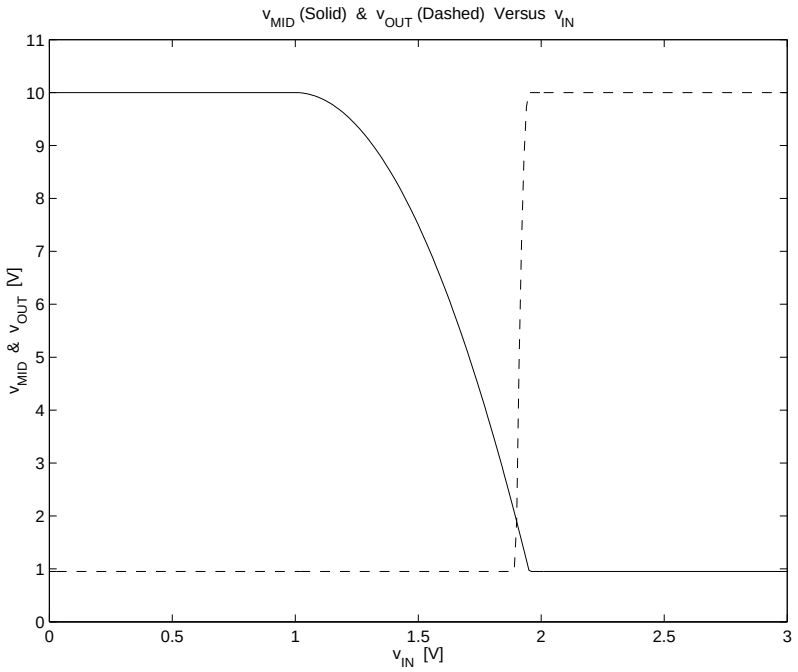
$$\frac{dv_{\mathrm{MID}}}{dv_{\mathrm{IN}}} = -RK(V_{\mathrm{IN}} - V_{\mathrm{T}})$$

Using this answer in the equation above gives:

$$\frac{dv_{\mathrm{OUT}}}{dv_{\mathrm{IN}}} = R^2K^2(V_{\mathrm{MID}} - V_{\mathrm{T}})(V_{\mathrm{IN}} - V_{\mathrm{T}})$$

Notice that this is just the product of the small-signal gain of each stage.

(G) Shown below is the graph created using the MatLab code attached to the end of the solutions.



Problem 4.4: An NPN bipolar junction transistor (NPN BJT) is a three-terminal device. Its terminals are referred to as the base, the collector and the emitter. The symbol for the NPN BJT is shown below, along with the voltage and current definitions for this BJT when it is viewed as a two-port device. Here, the Base-Emitter port acts as a control port and the Collector-Emitter port acts as a power port, much like the Gate-Source and Drain-Source ports of an n-channel MOSFET, respectively.

Figures 1 and 2 below describe the *greatly* idealized behavior of an NPN BJT in terms of its port variables. Figure 1 describes the behavior of the control port, and shows how i_{B} is related to v_{BE}. Figure 2 describes the behavior of the power port, and shows how i_{C} is related to v_{CE} for various values of i_{B}. In general, for $i_{\mathrm{B}} > 0$ and $v_{\mathrm{CE}} > 0$, $i_{\mathrm{C}} = \beta i_{\mathrm{B}}$ where β is a gain constant.

This problem investigates the use of the NPN BJT described by Figures 1 and 2 to construct an amplifier. The amplifier is shown in Figure 3. Assume that $V_{\mathrm{S}} > V_{\mathrm{D}}$.

(A) Determine i_{B} as a function of v_{IN}. Sketch and clearly label the result. Hint: a load-line analysis might provide useful insight given the nonlinear behavior shown in Figure 1.

(B) Determine v_{OUT} as a function of i_{B}; note that $v_{\mathrm{OUT}} = v_{\mathrm{CE}}$ for the amplifier shown in Figure 3. Sketch and clearly label the result. Hint: a load-line analysis might provide useful insight given the nonlinear behavior shown in Figure 2.

(C) Combine the results of Parts (A) and (B) to determine $v_{\rm OUT}$ as a function of $v_{\rm IN}$. Sketch and clearly label the result.

Symbol **Two-Port Definitions** **Figure 1**

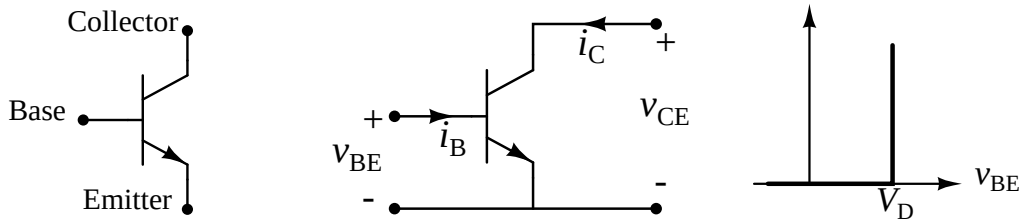
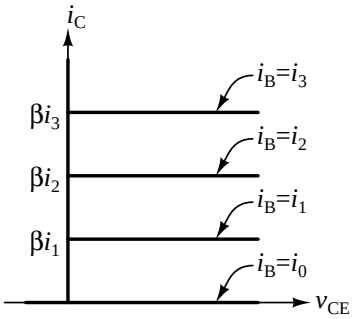
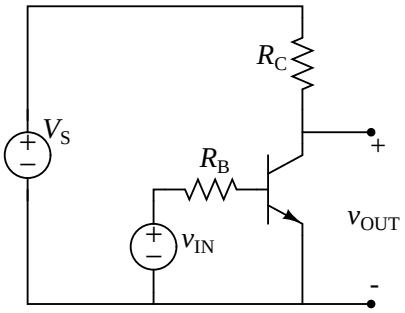


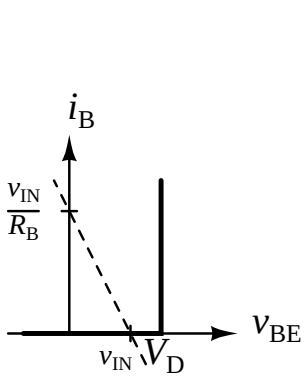
Figure 2 **Figure 3**



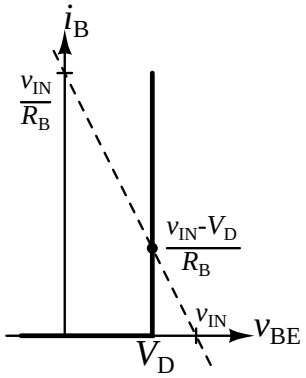


Answer:

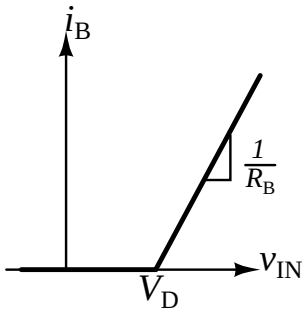
(A) There are two cases for the load line, as shown in the two figures below. When $v_{\rm IN} < V_{\rm D}$ no current flows into the base of the transistor. When $v_{\rm IN} > V_{\rm D}$ $v_{\rm BE}$ is constant, and $i_{\rm b} = \frac{v_{\rm IN} - V_{\rm D}}{R_{\rm B}}$.



Load Line
$v_{\rm IN} < V_{\rm D}$



Load Line
$v_{\rm IN} > V_{\rm D}$



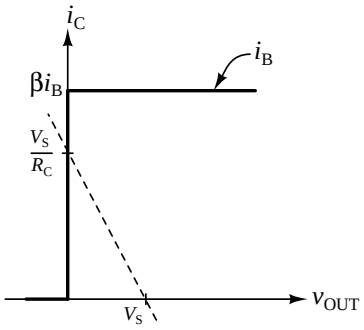
$i_{\rm B}$ vs $v_{\rm IN}$

(B) By inspection, we can write $v_{\rm OUT} = V_{\rm S} - R_{\rm C} \cdot i_{\rm C}$. From Figure 2 above, we can rewrite this as $v_{\rm OUT} = V_{\rm S} - R_{\rm C} \cdot \beta i_{\rm B}$. There are two different load lines to consider, one when $\frac{V_{\rm S}}{R_{\rm C}} \leq \beta i_{\rm B}$, and one when $\frac{V_{\rm S}}{R_{\rm C}} > \beta i_{\rm B}$. The load line analysis for this amplifier is drawn below. When $i_{\rm C} = 0$,

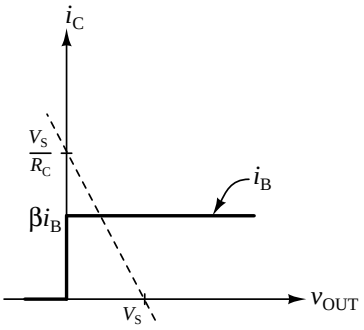
$v_{OUT} = V_S$. As i_C increases, v_{OUT} decreases (imagine the βi_B line traveling up the y axis, the intersection of it and the load line moving towards $v_{OUT} = 0$). Once $\beta i_B \geq \frac{V_S}{R_C}$, i_C remains constant at $\frac{V_S}{R_C}$, and $v_{OUT} = 0$. This gives:

$$\begin{array}{lcll} v_{OUT} & = & V_S & \text{when } i_B = 0 \\ v_{OUT} & = & V_S - R_C \beta i_B & \text{when } 0 < i_B \leq \frac{V_S}{\beta R_C} \\ v_{OUT} & = & 0 & \text{when } \frac{V_S}{\beta R_C} < i_B \end{array}$$

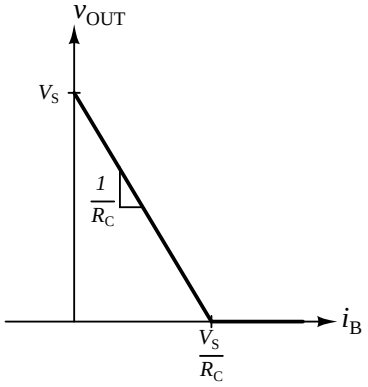
Load Line
$\frac{V_S}{R_C} \leq \beta i_B$



Load Line
$\frac{V_S}{R_C} > \beta i_B$



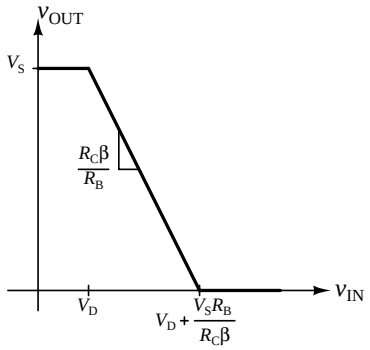
v_{OUT} vs i_B



(C) From part (A), we know that $i_b = \frac{v_{IN} - V_D}{R_B}$ when $v_{IN} > V_D$, and $i_B = 0$ when $v_{IN} < V_D$. Substituting this in to our result from part (B) gives:

$$\begin{array}{lcll} v_{OUT} & = & V_S & \text{when } v_{IN} \leq V_D \\ v_{OUT} & = & V_S - R_C \beta \frac{v_{IN} - V_D}{R_B} & \text{when } V_D < v_{IN} < V_D + \frac{V_S R_B}{\beta R_C} \\ v_{OUT} & = & 0 & \text{when } V_D + \frac{V_S R_B}{\beta R_C} \leq v_{IN} \end{array}$$

The sketch looks like:



Matlab Code for problem 4.3(G)

```
% MatLab Script For PS#4 Problem 4.3(G)

% Define Constants

k = 0.02;
r = 1e3;
vs = 10;
vt = 1;

% Compute A Constant For Convenience

vx = (-1+sqrt(2*r*k*vs+1))/(r*k);

% Define Input Space

vin = linspace(0,3,301);

% M1 Cutoff Region

for i = 1:length(vin),
  vmid(i) = vs;
end

% M1 Saturation Region

for i = 1:length(vin),
  if ((vt <= vin(i)) & (vin(i) <= vt+vx)), vmid(i) = vs - 0.5*r*k*(vin(i)-vt)^2; end;
end

% M1 Triode Region

for i = 1:length(vin),
  if vt+vx <= vin(i), vmid(i) = vx; end;
end

% M2 Cutoff Region

for i = 1:length(vmid),
  vout(i) = vs;
end

% M2 Saturation Region

for i = 1:length(vmid),
  if ((vt <= vmid(i)) & (vmid(i) <= vt+vx)), vout(i) = vs - 0.5*r*k*(vmid(i)-vt)^2; end;
end
```

```
% M2 Triode Region

for i = 1:length(vmid),
  if vt+vx <= vmid(i), vout(i) = vx; end;
end

% Plot Results

plot(vin,vmid)
hold
plot(vin,vout,'--')
title('v_{MID} (Solid) & v_{OUT} (Dashed) Versus v_{IN}')
xlabel('v_{IN} [V]')
ylabel('v_{MID} & v_{OUT} [V]')
```