Exercise 6.1: Consider an amplifier with an input-output relation that takes the form \( v_{\text{OUT}} = V_A (v_{\text{IN}} / V_B)^5 \), where \( V_A \) and \( V_B \) are voltage constants. Determine its output bias voltage \( V_{\text{OUT}} \) and its small-signal gain \( v_{\text{out}} / v_{\text{in}} \) for a given input bias voltage \( V_{\text{IN}} \).

Exercise 6.2: Find the capacitance of the all-capacitor network, and the inductance of the all-inductor network, shown below.

![Diagram of circuits]
Problem 6.1: This problem studies the propagation delay of digital signals through the inverter shown below. Assume that the MOSFET in the inverter acts as a switch with on-state resistance $R_{ON}$. The inverter is loaded with a capacitor, having capacitance $C_G$, that models the combined input capacitance of the logic gates connected to its output. Assume that the inverter obeys the static discipline defined in part by $V_{OL}$ and $V_{OH}$.

(A) Assume that the MOSFET has been off for a very long time. At $t = 0$, $v_{IN}$ turns the MOSFET on. Determine $v_G(t)$ for $t \geq 0$.

(B) How long does it take $v_G(t)$ to pass by $V_{OL}$? This delay is the fall time of the inverter.

(C) Assume that the MOSFET has been on for a very long time. At $t = 0$, $v_{IN}$ turns the MOSFET off. Determine $v_G(t)$ for $t \geq 0$.

(D) How long does it take $v_G(t)$ to pass by $V_{OH}$? This delay is the rise time of the inverter.

(E) How can the fall and rise times be shortened via the design of $R_{PU}$? What limits the extent to which this design path may be followed?
**Problem 6.2:** In the circuit shown below, a MOSFET and an external resistor having resistance $R_X$ are used to control the current $i_R$ in the winding of a relay. Here, the relay is modeled as a series inductor and resistor having inductance $L_R$ and resistance $R_R$, respectively. The MOSFET may be modeled as an ideal switch.

(A) At $t = 0$, $v_{IN}$ turns the MOSFET on so that $v_{DS} = 0$. Determine $i_R(t)$ for $t \geq 0$ given that $i_R(t = 0) = 0$.

(B) Next, at $t = T$, $v_{IN}$ turns the MOSFET off. Determine both $i_R(t)$ and $v_{DS}(t)$ for $t \geq T$. Hint: $i_R(t)$ is continuous at $t = T$.

(C) Sketch and clearly label graphs of both $i_R(t)$ and $v_{DS}(t)$ for $t \geq 0$ assuming that $T \approx 5L_R/R_R$ and $R_X = R_R$.

(D) The relay control circuit would be less expensive without the external resistor, which may be “removed” from the circuit by considering the limit $R_X \to \infty$. Why might such a cost reduction be unwise?

![Circuit Diagram](image-url)
**Problem 6.3:** At $t = 0^-$, the networks shown below have zero initial state. That is, the capacitor voltage $v(t)$ and the inductor current $i(t)$ are both zero at $t = 0^-$. At $t = 0$, the voltage source produces an impulse of area $A$, and the current source produces an impulse of area $Q$.

(A) Derive the differential equation that relates $v(t)$ to $I(t)$ and $i(t)$ to $V(t)$. Hint: consider using Thevenin or Norton equivalent networks to simplify the work.

(B) Find the capacitor voltage $v(t)$ and the inductor current $i(t)$ at both $t = 0^+$ and $t = \infty$. One way to find the states at $t = 0^+$ is to integrate the corresponding differential equations from $t = 0^-$ to $t = 0^+$ under the assumption that each state remains finite during that time; you should justify this assumption. Then, substitute the initial conditions at $t = 0^-$ into the results to determine the states at $t = 0^+$. Try to determine the states at $t = \infty$ through physical, rather than mathematical, reasoning.

(C) Next, find the time constant by which each state goes from its initial value at $t = 0^+$ to its final value at $t = \infty$.

(D) Using the previous results, and without necessarily solving the differential equations directly, construct $v(t)$ and $i(t)$ for $t \geq 0$.

(E) Verify that the solutions to Part (D) are correct by substituting them into the differential equation found in Part (A).