

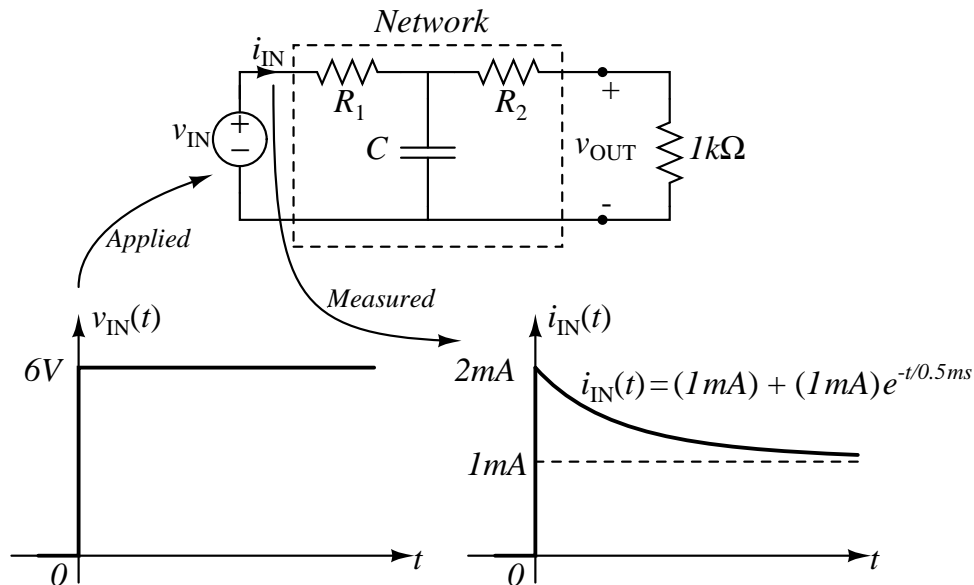
Massachusetts Institute of Technology  
Department of Electrical Engineering and Computer Science

6.002 – Electronic Circuits  
Spring 2002

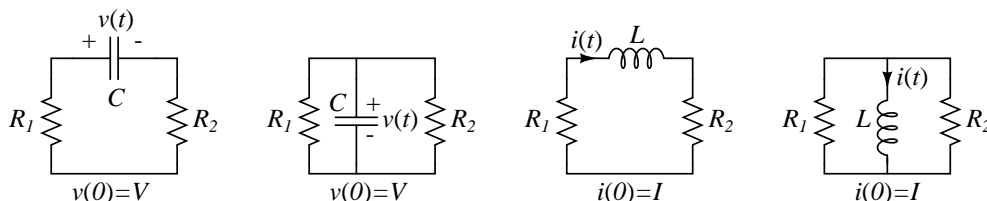
Homework #7

Issued 3/20/02 – Due 4/3/02

**Exercise 7.1:** The network shown below has two ports, two resistors and one capacitor. The resistor values  $R_1$  and  $R_2$ , and the capacitor value  $C$ , are all unknown. Also shown below is the result of an experiment performed on the network in which one port is driven with the voltage step  $v_{IN}$  at  $t = 0$ , and the other port is loaded with a  $1\text{ k}\Omega$  resistor. Using the experimental result, which consists of the measured current  $i_{IN}$ , find the values  $R_1$ ,  $R_2$  and  $C$ . Also, find the voltage  $v_{OUT}$  across the load resistor for  $t \geq 0$ . In doing so, assume that the network capacitor is uncharged prior to  $t = 0$ .

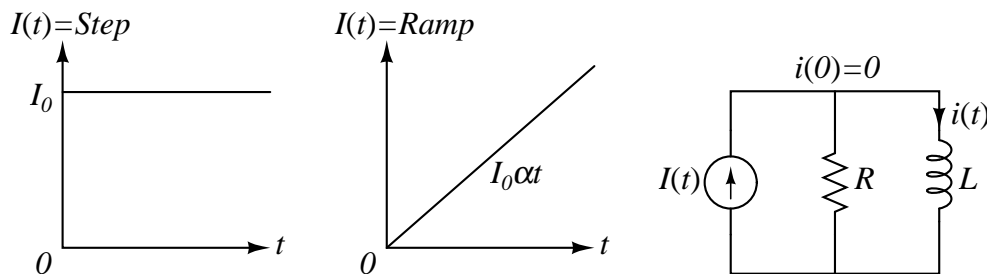


**Exercise 7.2:** Each network shown below has a non-zero initial state at  $t = 0$ , as indicated. Find the network states for  $t \geq 0$ . Hint: what equivalent resistance is in parallel with each capacitor or inductor, and what decay time results from this combination?



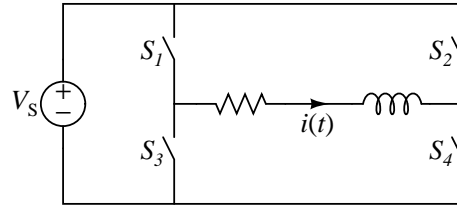
**Problem 7.1:** This problem examines the relation between transient responses of linear systems. The network shown below is first driven by a current step at  $t = 0$ , then driven by a current ramp at  $t = 0$ , and finally driven by the current step plus the current ramp at  $t = 0$ . In the first two cases, the inductor has zero initial current, as indicated.

- Find the inductor current  $i(t)$  in response to the current step shown below. Assume that  $i(0) = 0$ .
- Find the inductor current  $i(t)$  in response to the current ramp shown below. Again assume that  $i(0) = 0$ .
- The step input can be constructed from the ramp input according to  $I_{\text{Step}}(t) = \frac{1}{\alpha} \frac{d}{dt} I_{\text{Ramp}}(t)$ . Show that their respective responses are related in a similar manner.
- Would the result from Part C hold if  $i(0) \neq 0$ ? Why or why not?
- Finally, find the inductor current  $i(t)$  in response to the current step plus the current ramp, that is to  $I(t) = I_0(1 + \alpha t)$  for  $t \geq 0$ . This time assume that  $i(0) = i_0$ . Hint: think superposition.

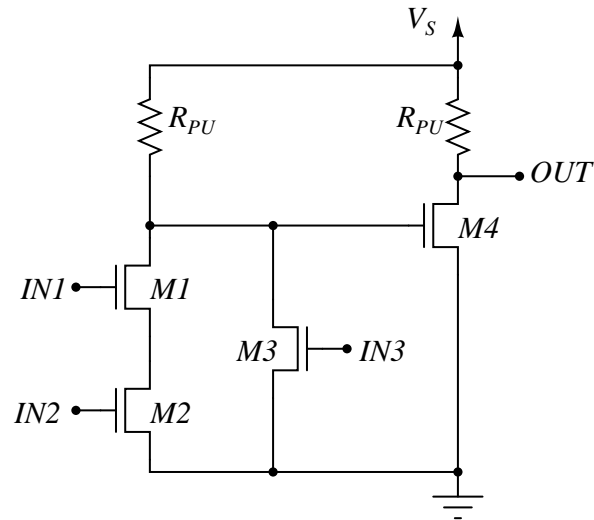


**Problem 7.2:** The circuit shown below can be used to regulate the current through an inductor. Typical applications include the regulation of currents in motors, solenoids and loud speakers, all of which have inductive windings. We will analyze the circuit assuming that it operates in a cyclic manner with switching period  $T$ . During the first part of each period, which lasts for a duration  $DT$ , switches S1 and S4 are on while switches S2 and S3 are off. During the second part of each switching period, which lasts for a duration  $(1 - D)T$ , switches S1 and S4 are off while switches S2 and S3 are on. Note that  $0 \leq D \leq 1$ .

- Assume that  $D$  is constant and that the circuit has been operating long enough to reach a cyclic steady state by  $t = 0$ , at which point a new switching period begins. In terms of the unknown  $i(0)$ , determine  $i(t)$  for  $0 \leq t \leq T$ .
- Use your result from Part (A), and the fact that the circuit operates in a cyclic steady state to determine  $i(0)$ . Note that with this result, and that from Part (A),  $i(t)$  is completely determined.
- Find the average value of  $i(t)$  over the period  $0 \leq t \leq T$ . Hint: is it necessary to average the result from Part A, or is there a faster method to find the average?
- Suppose that the circuit has been operating with  $D \equiv D_1$  for a time long enough to reach a cyclic steady state by  $t = 0$ . Suppose that  $D$  switches to  $D = D_2$  at  $t = 0$ , just as a new switching period begins. In this case, determine  $i(t)$  for  $t \geq 0$ . Hint: can you use your result from Parts (A) and (B) as a particular solution over the interval  $0 \leq t$ ?



**Problem 7.3:** Consider the digital logic circuit from Problem 3.1. Model each MOSFET with the switch-resistor model, and let the on-state resistance  $R_{ON}$  satisfy  $R_{ON} \ll R_{PU}$ . Further assume that MOSFET M4 has a gate-to-source capacitance  $C_{GS}$ . Given that the inputs IN1, IN2 and IN3 cycle through the combinations 000, 001, 010, 011, 100, 101, 110, 111, determine the average power dissipated by the logic circuit. Assume that each input combination is held for the period  $T$  with  $T \gg R_{PU}C_{GS}$ . Make appropriate simplifications based on the inequalities for  $R_{ON}$  and  $T$ .



**Problem 7.4:** Develop a CMOS logic circuit that implements  $OUT = \overline{IN1 + \overline{IN2} \cdot \overline{IN3}}$ . Hint, review your answer to Exercise 4.1 first.