Massachusetts Institute of Technology
Department of Electrical Engineering and Computer Science

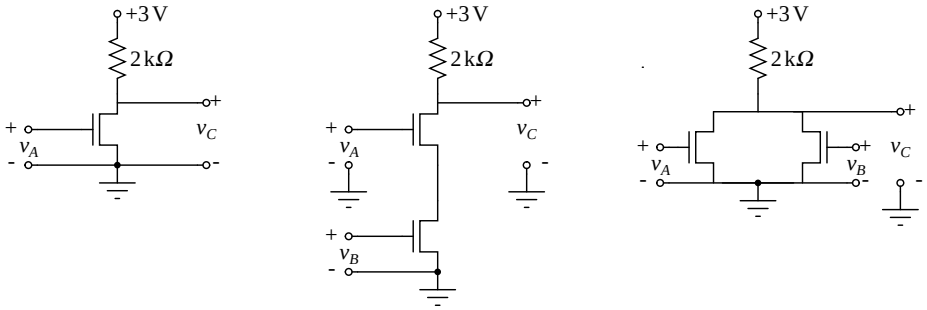
6.002 – Circuits and Electronics
Spring 2003

Handout S03-007 - Homework #1

Issued: Wed. Feb 5
Due: Fri. Feb 14

In Problems 1.1 and 1.2 use the convention that a logical one corresponds to a high voltage level and a logical zero corresponds to a low voltage level. Assume that the high voltage level is much greater than the threshold voltage. When the voltage v_A associated with the Boolean variable A is high (3 volts), $A = 1$; when v_A is low (≈ 0 volts), $A = 0$. The same relationship holds with v_C and C.

Problem 1.1:

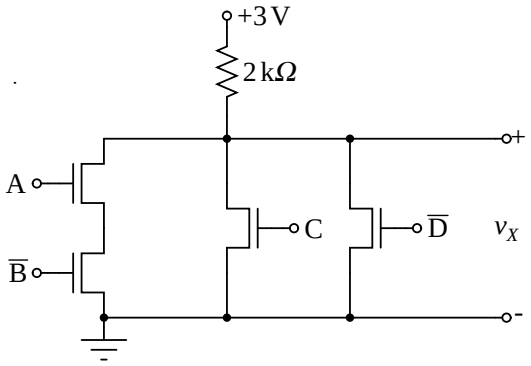


(*i*) (*ii*) (*iii*)

1) For each circuit above, generate a truth table which shows how the output depends on the input(s).

2) Assume that the "on" resistance of the MOSFETs is 100Ω. What is the value of the output voltage v_C for $C = 0$ and for $C = 1$?

Problem 1.2:

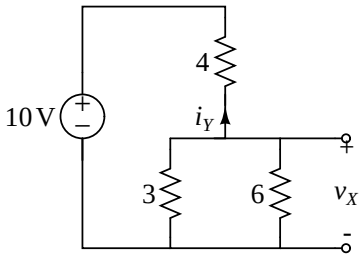


1) Generate a truth table which shows the dependence of x on A,B,C, and D.

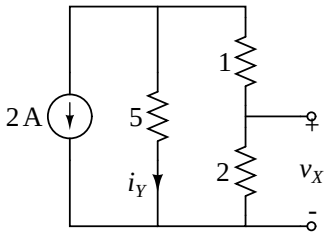
2) Assume that the "on" resistance of the MOSFETs is 100Ω. What is the range of possible values for the 0 state of the output voltage v_X?

3) What is the maximum power requirement of this circuit?

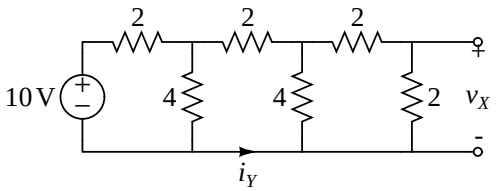
Problem 1.3: What is the value of the voltage v_X and the curent i_Y in each of the following circuits? All resistance values are in Ω.



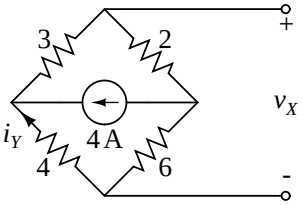
(*i*)



(*ii*)

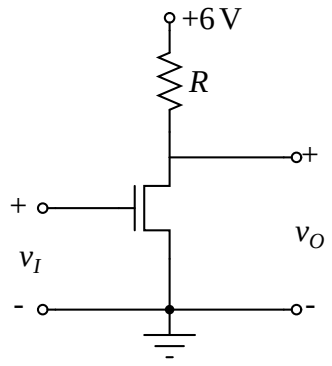


(*iii*)



(*iv*)

Problem 1.4: Consider the inverter below:



Assume that the FET has an "on" resistance of 200Ω and a threshold voltage of 2.5 ± 0.1V. The ± 0.1 deviation accounts for device-to-device variations. The static discipline for the chip in which this FET will be used is

$$\text{INPUT} \begin{cases} v_{IH} = 4\text{V} \\ v_{IL} = 2\text{V} \end{cases} \qquad \text{OUTPUT} \begin{cases} v_{OH} = 5\text{V} \\ v_{OL} = 0.5\text{V} \end{cases}$$

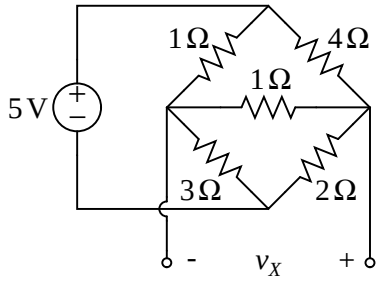
1) If R is too small, the inverter will not satisfy the static discipline. What is the minimum permissable value of R?

2) What are the noise margins for each logical state of the input?

3) What is the width of the forbidden region?

4) What part(s) of the staic discipline would you change to make the 0 and 1 noise margins equal? How does this change the forbidden region?

Problem 1.5: Determine the voltage v_X in the circuit below. **Hint:** Define a reference node and write a pair of node equations.



Problem 1.6: For the circuit below, write a set of three KCL equations sufficient to solve for the node to reference voltages e_1,e_2, and e_3. Express your equations in the form:

$$\begin{aligned} [\cdots]e_1 - [\cdots]e_2 - [\cdots]e_3 &= \text{source terms} \\ -[\cdots]e_1 + [\cdots]e_2 - [\cdots]e_3 &= \text{source terms} \\ -[\cdots]e_1 - [\cdots]e_2 + [\cdots]e_3 &= \text{source terms} \end{aligned}$$

where the brackets contain sums of conductances.
Do <u>not</u> solve these equations!