NOTES FOR 6.002 LECTURE # 12, TUESDAY, MARCH 12, 2003

LABORATORY #2 THIS WEEK!

- CIRCUITS NO MORE COMPLEX THAN IN THE FIRST LAB.
- BUILD AND CHANGE CIRCUIT WITH THE POWER OFF.
- IF YOUR CIRCUIT DOESN'T WORK, CHECK WIRING FIRST, IF THAT DOESN'T FIX IT, CHANGE THE FET.

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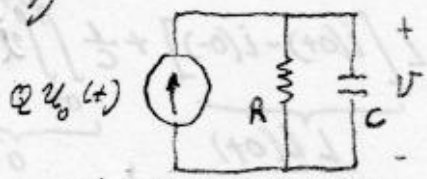
READ 12.1 - 12.3

FURTHER ILLUSTRATION OF THE HANDLING OF IMPULSE EXCITATIONS AND OTHER SINGULARITY FUNCTIONS.

1)



AT $t = 0-$, $v(0-) = +V_1$
(INITIAL CHARGE ON C)

IF THE CURRENT IMPULSE WERE TO GO INTO R, v WOULD BE A VOLTAGE IMPULSE - NOT POSSIBLE GIVEN THE PARALLEL CAPACITOR. THUS IT FLOWS INTO C, CHANGING THE VOLTAGE BY $+Q/C$.

MORE FORMALLY, DE AT $t=0$ IS:

$$Q u_0(t) = \frac{v}{R} + C\frac{dv}{dt}$$ INTEGRATE THROUGH $t=0$

$$\int_{0-}^{0+} Q u_0(t)\,dt = \frac{1}{R}\int_{0-}^{0+} v\,dt + Cv\Big|_{0-}^{0+}$$

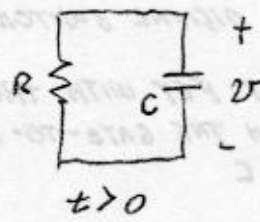
$\int_{0-}^{0+} Q u_0(t)\,dt = Q$

$\frac{1}{R}\int_{0-}^{0+} v\,dt = 0$ BECAUSE THE INTEGRAND IS FINITE AND THE INTERVAL IS INFINITESIMAL.

THUS $\frac{Q}{C} = v(0+) - v(0-)$

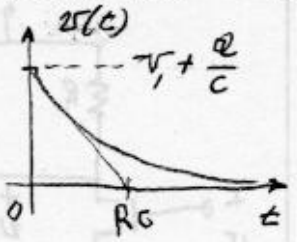
OR $\underline{v(0+) = Q/C + V_1}$

FOR $t > 0$ THE CURRENT SOURCE IS ZERO. CIRCUIT IS:



$t > 0$

THE INITIAL VOLTAGE $v(0+)$ DECAYS EXPONENTIALLY WITH A TIME CONSTANT RC.



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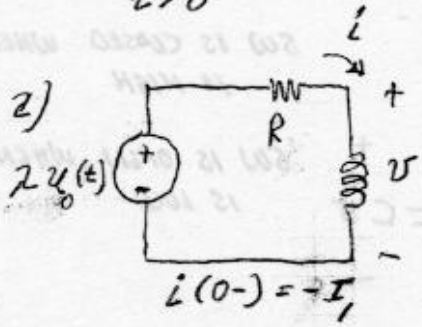
2)



$i(0-) = +I_1$

D.E. AT $t=0$

$$\lambda u_0(t) = Ri + L\frac{di}{dt}$$ INTEGRATE THROUGH $t=0$

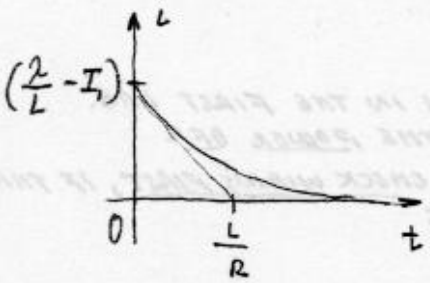
$$\lambda = R\int_{0-}^{0+} i\,dt + Li\Big|_{0-}^{0+}$$ THUS $\left[i(0+) - i(0-)\right] = \frac{\lambda}{L}$

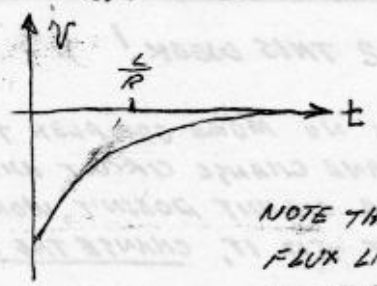
OR $\underline{i(0+) = \lambda/L - I_1}$

THE CURRENT DECAYS EXPONENTIALLY WITH A TIME CONSTANT L/R:

$$i(t) = \left(\frac{\lambda}{L} - I_1\right) e^{-\frac{tR}{L}} \quad t > 0$$

THE VOLTAGE $v(t)$ IS $v = L\frac{di}{dt} = -\left(\frac{\lambda}{L} - I_1\right)\frac{R}{L}e^{-tR/L} = -\left(\frac{\lambda}{L} - I_1\right)Re^{-\frac{tR}{L}}$

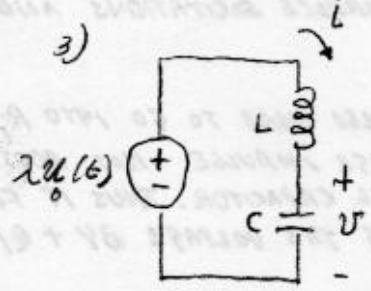




FOR $t>0$, THE INDUCTOR CURRENT DECAYS THROUGH THE RESISTOR

NOTE THAT IF $\frac{\lambda}{L} = I_1$, THE INITIAL FLUX LINKAGE AND ENERGY IN L IS EXACTLY REMOVED BY THE IMPULSE AND THERE IS NO TRANSIENT.

3)



FOR $t<0$ $\begin{cases} i=0 \\ v=0 \end{cases}$

O.E $\lambda u_0(t) = L\frac{di}{dt} + \frac{1}{C}\int i\,dt$ AGAIN INTEGRATE THROUGH $t=0$

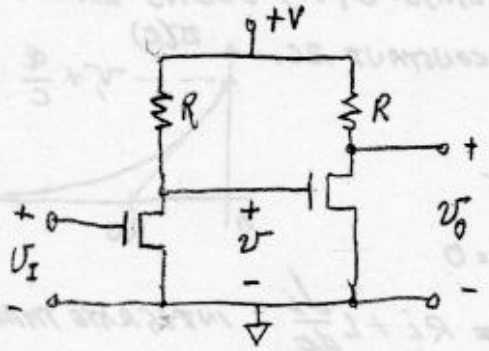
$$\underbrace{\lambda\int_{0^-}^{0^+} u_0(t)\,dt}_{\lambda} = \underbrace{L\left[i(0^+) - i(0^-)\right]}_{Li(0^+)} + \underbrace{\frac{1}{C}\int_{0^-}^{0^+}\int_{0^-}^{0^+} i\,dt\,dt}_{0}$$

$$i(0^+) = \frac{\lambda}{L} \qquad v(0^+) = 0$$

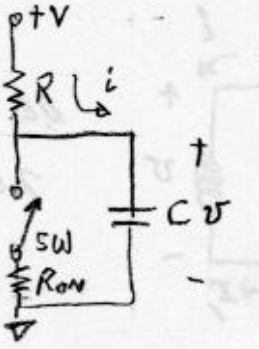
BEHAVIOR FOR $t>0$ IS THE SUBJECT OF LECTURE 13

A GENERALIZATION: OBSERVE THE DIFFERENTIAL EQUATION WITH A IMPULSE AS THE DRIVE. THE IMPULSE IS ABSORBED BY THE HIGHEST ORDER TERM ON THE RIGHT. THAT IS: IN 1), BY $C\,dv/dt$ RATHER THAN v/R. IN 2), BY $L\,di/dt$ RATHER THAN Ri, IN 3) BY $L\,di/dt$ RATHER THAN $\int v\,dt$.

DIFFERENT SUBJECT: ENERGY STORAGE IN DIGITAL SWITCHES



MODEL THE LEFT FET WITH THE SR MODEL, THE RIGHT WITH THE GATE-TO-SOURCE CAPACITANCE C



SW IS CLOSED WHEN v_I IS HIGH

SW IS OPEN WHEN v_I IS LOW

CONSIDER A FULL CYCLE $v_I = 0 \rightarrow v_I = V \rightarrow v_I = 0$

WHAT IS THE POWER DISSIPATION OVER A CYCLE?

WITH SW OPEN THERE IS NO CURRENT IN R, $V = V$ AND THE ENERGY STORED IN C IS $E_A = \frac{1}{2}CV^2$

WHEN SW CLOSES THIS STORED ENERGY IS DISSIPATED ENTIRELY IN THE FET, THAT IS IN R_{ON}. IN THIS STATE THERE IS POWER DISSIPATED IN R:

$$P_B = \frac{V^2}{R} \quad \text{ASSUMING } R_{ON} \ll R$$

WHEN SW OPENS AGAIN THE ENERGY PROVIDED BY THE POWER SOURCE IS:

$E_T = \int_0^\infty V i\,dt$ WHERE i IS THE CURRENT CHARGING C. BY INSPECTION, THE CHARGING CURRENT IS: $i(t) = \frac{V}{R}e^{-t/RC}$ ASSUMING SW OPENS AT $t=0$

THUS $E_T = \frac{V^2}{R}\int_0^\infty e^{-t/RC}\,dt = -\left(\frac{V^2}{R}\right)(RC)\,e^{-t/RC}\Big|_0^\infty = CV^2$ $\quad E_B = CV^2$

AFTER SEVERAL TIME CONSTANTS THE CAPACITOR VOLTAGE IS $V = V$ AND THE STORED ENERGY IS $\frac{1}{2}CV^2$. THE DIFFERENCE BETWEEN E_B AND $CV^2/2$ IS ENERGY DISSIPATED IN R DURING CHARGING.

THE AVERAGE POWER DISSIPATION OVER A CYCLE IS:

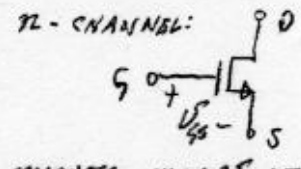
$$P_{AVG} = \frac{CV^2}{T} + \frac{P_B}{2}$$ WHERE T IS THE PERIOD AND BY ASSUMPTION THE SWITCH IS CLOSED FOR HALF THE PERIOD.

THE TERM CV^2/T IS <u>UNAVOIDABLE</u> <u>DISSIPATION</u> IN STATE OPERATION.

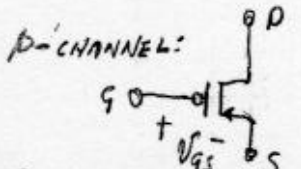
HALF OF IT IS DISSIPATED IN R WHEN C IS CHARGING, AND IT IS INDEPENDENT OF R. THE OTHER HALF IS DISSIPATED IN R_{ON} WHEN C IS DISCHARGED THROUGH R_{ON}.

NOTE THAT THIS UNAVOIDABLE <u>DYNAMIC LOSS</u> VARIES AS V^2 - THUS THE DRIVE TO LOWER OPERATING VOLTAGES AND IS PROPORTIONAL TO THE FREQUENCY OF THE CYCLE $f = 1/T$.

THE STATIC LOSS P_B IS ALWAYS PRESENT IN CIRCUITS USING ONLY N-CHANNEL FETS (NMOS LOGIC). IT CAN BE COMPLETELY ELIMINATED IN CMOS LOGIC IN WHICH THE PULL UP RESISTOR IS REPLACED BY A <u>P-CHANNEL FET.</u>

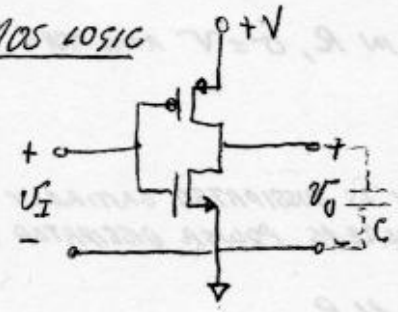


CONDUCTS WHEN $V_{GS} > V_T$ (POSITIVE QUANTITY)



CONDUCTS WHEN $V_{GS} < V_T$ (NEGATIVE QUANTITY)

CMOS LOGIC

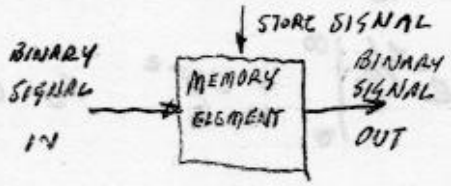


UPPER FET IS p-CHANNEL. LOWER IS n-CHANNEL

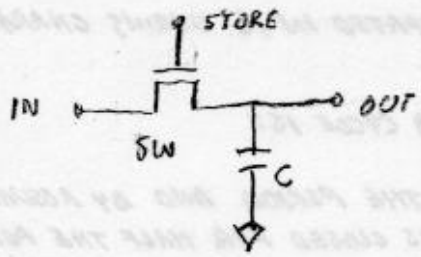
WHEN V_I IS HIGH UPPER IS OFF, LOWER IS ON, BUT V_0 IS LOW THERE IS NO STEADY CURRENT DOWN THE GATE.

WHEN V_I IS LOW, LOWER IS OFF, BUT UPPER IS ON SO THAT V_0 IS HIGH. AGAIN THERE IS NO STATIC CURRENT. $P_B \equiv 0$. THE ONLY DISSIPATION IS DYNAMIC (DURING SWITCHING) AND IS CV^2f

DIGITAL MEMORY - RELIES ON THE ENERGY STORED IN A CAPACITOR.

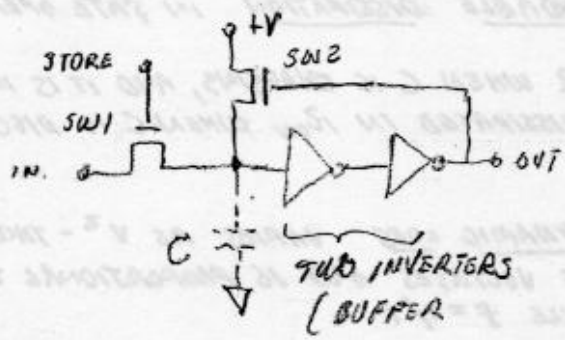


POSSIBLE CIRCUIT:



WHEN SW CLOSES THE HIGH OR LOW VOLTAGE AT IN IS STORED ON C. THE SWITCH CAN BE A FET OPERATED IN THE SWITCHING MODE

PROBLEMS: V_{OUT} DECAYS BECAUSE OF LEAKAGE CURRENTS AND ENERGY LOST WHEN V_{OUT} IS SAMPLED.



AS ABOVE EXCEPT SW2 CLOSES PERIODICALLY WHEN V_{OUT} IS HIGH TO RENEW CHARGE ON C, WHICH CAN BE THE GATE-TO-SOURCE CAPACITANCE OF THE FIRST INVERTER.