**Massachusetts Institute of Technology**
**Department of Electrical Engineering and Computer Science**

**6.002 – Circuits and Electronics**
**Spring 2003**

**Handout S03-056 - Homework #11**

**Issued: Thur. Apr 24**
**Due: Fri. May 2**

## Introduction

This homework assignment focuses on the analysis and design of a system for playing back a digitally-stored audio signal. Additionally, this assignment serves as the pre-lab exercises for Lab #4, which will involve the construction, testing and demonstration of the audio playback system. *Consequently, you should save a copy of your results for use during Lab #4.*

A block diagram of the audio playback system is shown in Figure 1. At the center of the system is a digital memory in which 32,768 samples of the audio signal are stored. Each sample in the memory has a unique numerical address between 0 and 32,767, inclusive. Consecutive samples are stored at consecutive addresses. To obtain 32,768 consecutive samples of the audio signal, 4.096 seconds of continuous analog audio signal are first sampled at an 8-kHz rate. The analog audio samples are then digitized by an 8-bit analog-to-digital converter. That is, the samples are quantized to take on one of 256 possible discrete digital values between 0 and 255, inclusive. Here, the digital value of 0 corresponds to the most positive audio signal level, and the digital value of 255 corresponds to the most negative audio signal level. The resulting digital data is then written into the memory.

To retrieve the stored audio signal samples in sequence at the proper rate, the memory is addressed by a counter which counts from 0 to 32,767 at an 8-kHz rate established by an external clock. After counting to 32,767 the counter returns to 0, and the retrieval process repeats itself. As the memory address increments, the corresponding data appears at the memory output. This data is converted back to an analog voltage in a piecewise constant manner by a digital-to-analog converter.

During the course of recording and playing back the analog audio signal, the signal is sampled in time, quantized in amplitude, and reconstructed in a piecewise constant manner. As you will learn in 6.003, this process introduces undesirable high-frequency components into the signal. To

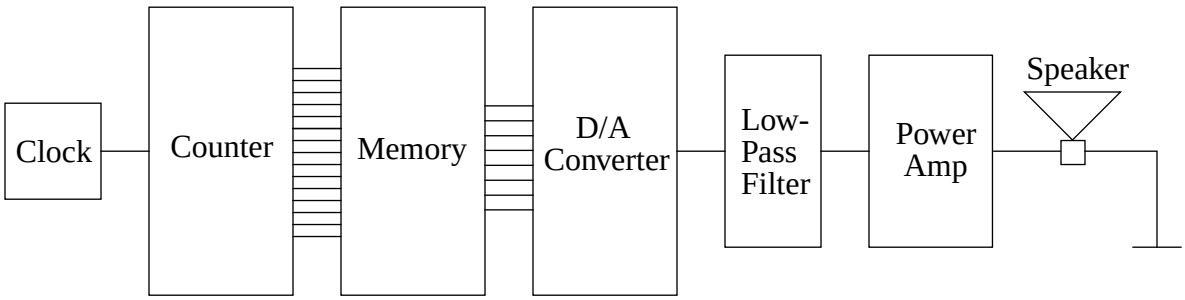


Figure 1: block diagram of the audio playback system

minimize the perceived impact of these components, the signal is filtered by a low-pass filter after it is reconstructed by the digital-to-analog converter. Finally, the signal is amplified by a power amplifier which in turn drives a speaker, or alternatively headphones. The power amplifier is necessary because the low-pass filter is not capable of driving a speaker directly.

In the course of this homework assignment you will analyze and design four of the functional blocks shown in Figure 1. These blocks are the clock, the digital-to-analog converter, the low-pass filter and the power amplifier. In Lab #4, you will construct these blocks and verify that they perform as desired. Then, you will combine them with the counter, the read-only memory and the speaker to construct and demonstrate the entire audio play-back system. Since you will construct the system from the components in your 6.002 lab kit, your design of the blocks must account for the fact that the available components are limited.

### Problem 11.1: The Clock

The circuit shown in Figure 2 is the system clock, which is a square-wave oscillator followed by a CMOS inverter; the inverter functions only as a buffer. The oscillator is constructed from another CMOS inverter, a resistor and a capacitor. Both inverters are powered between the positive supply voltage $V_S$ and ground, and both exhibit the hysteretic input-output characteristic defined in the figure. The inverters are otherwise ideal.

(A) Assume that $v_{CAP}$ has just charged up to $V_H$ so that $v_{OSC}$ has just switched to 0 V. How much time elapses before $v_{CAP}$ decays to $V_L$, which in turn causes $v_{OSC}$ to switch to $V_S$?

(B) Assume that $v_{CAP}$ has just decayed to $V_L$ so that that $v_{OSC}$ has just switched to $V_S$. How much time elapses before $v_{CAP}$ charges up to $V_H$, which in turn causes $v_{OSC}$ to switch to 0 V?

(C) Determine the frequency of the oscillator in terms of $R$, $C$, $V_L$, $V_H$ and $V_S$.

(D) Assume that $V_L = 1.8$V, $V_H = 3.0$V and $V_S = 5.0$V. Choose values for $R$ and $C$ so that the oscillator oscillates at or very near 8-kHz. Since oscillator frequency alone under-specifies $R$ and $C$, there is no single correct choice. Therefore, choose values for $R$ and $C$ that are easily implemented with the components in the 6.002 lab kit.

(E) For the choice of $R$ and $C$ from Part (D), sketch and clearly label a single graph that displays $v_{CAP}$, $v_{OSC}$ and $v_{CLK}$ as a function of time over one period of oscillation.

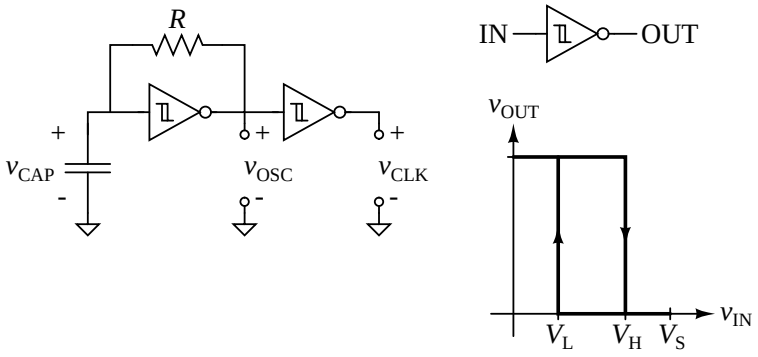


Figure 2: the system clock

**Problem 11.2: The Digital-To-Analog Converter**

The circuit shown in Figure 3 is the digital-to-analog converter. The voltage sources $v_{\mathrm{DB0}}$ through $v_{\mathrm{DB7}}$ represent the voltages supplied by the eight data bits of the digital memory, DB0 through DB7. These voltages will be approximately 5 V when the corresponding data bit is a logical high, and approximately 0 V when the corresponding data bit is a logical low. The voltage $v_{\mathrm{OFF}}$, which is set by a potentiometer, is an offset voltage that is used to center the output of the converter around 0 V. Assume that the op-amp in the converter is ideal.

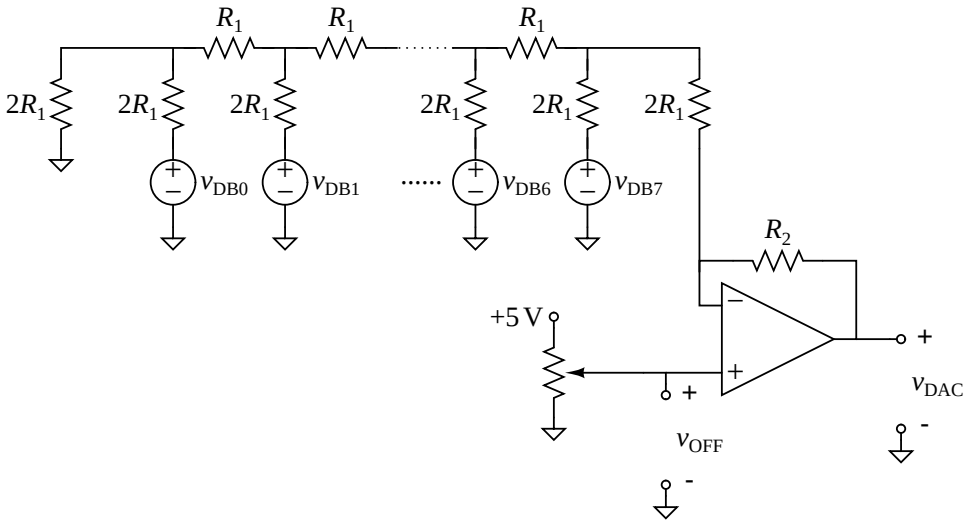


Figure 3: the digital-to-analog converter

(A) Determine $v_{\mathrm{DAC}}$ as a function of $v_{\mathrm{DB0}}$ through $v_{\mathrm{DB7}}$, and $v_{\mathrm{OFF}}$.

**Hint:** Use superposition, and exploit the repetitive nature of the resistive network. It's easiest to start with $v_{\mathrm{DB7}}$.

(B) With $v_{\mathrm{OFF}} = 0\mathrm{V}$, the output of the digital-to-analog converter should span the range of 0 V to -2.5 V. Thus, the output of the converter should be given by

$$v_{\mathrm{DAC}} = -2.5\ \mathrm{V} \sum_{i=0}^{7} \frac{2^i}{255} \mathrm{DB}i$$

where each data bit DB$i$ takes on the numerical value of 1 when high and 0 when low. In this manner, each successive data bit from DB0 to DB7 is given a voltage weighting twice that of the preceding data bit, making it possible for the converter to output voltages from 0 V to -2.5 V in steps of -2.5/255 V. Given this, determine $R_2$ in terms of $R_1$.

The input voltage rating of the speaker is approximately $\pm 1.25$V. Since the low-pass filter has unity voltage gain over the frequency range of interest, the output range of the digital-to-analog converter must be designed to match the speaker rating. This is why the range is chosen to be 0 V to -2.5 V, with $v_{\mathrm{OFF}} = 0$. Note further that the output range of the converter is negative. This is because the converter is based upon the inverting amplifier configuration.

(C) The role of $v_{\mathrm{OFF}}$ is to offset the output of the digital-to-analog converter so that it is centered

around 0 V. That is, with DB0 through DB7 all low, $v_{\rm DAC}$ should be 1.25 V, and with DB0 through DB7 all high, $v_{\rm DAC}$ should be -1.25 V. Given this, what must be the value of $v_{\rm OFF}$?

(D) Assume that $R_1 = 10\text{k}\Omega$. Use the result of Part (B) to determine $R_2$.

### Problem 11.3: The Low-Pass Filter

The circuit shown in Figure 4 is the low-pass filter. It is a second-order filter, and is driven by the output of the digital-to-analog converter. Its purpose is to remove the high-frequency components of the audio signal that result from the sampling, quantization and reconstruction of that signal. Assume that the op-amp in the filter is ideal.

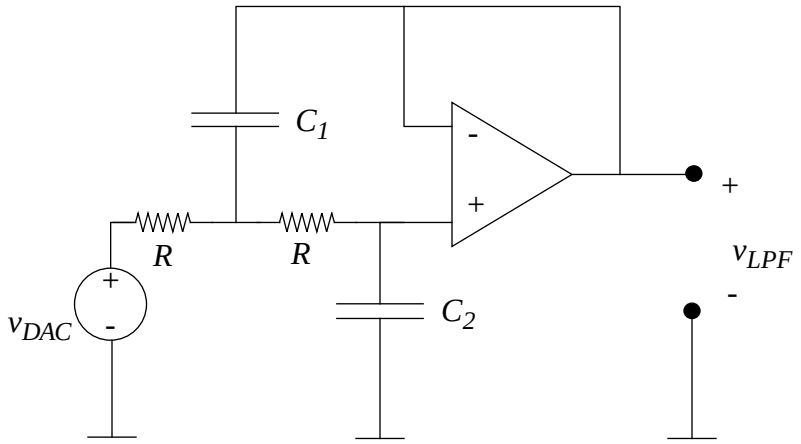


Figure 4: the low-pass filter

(A) Assume that the low-pass filter operates in sinusoidal steady state with $v_{\rm DAC} = \Re\{\tilde{v}_{\rm DAC}e^{j\omega t}\}$ and $v_{\rm LPF} = \Re\{\tilde{v}_{\rm LPF}e^{j\omega t}\}$ where $\tilde{v}_{\rm DAC}$ and $\tilde{v}_{\rm LPF}$ are complex amplitudes. Find the input-output transfer function $H_{\rm LPF}(\omega)$ of the filter where $H_{\rm LPF}(\omega) \equiv \tilde{v}_{\rm LPF}/\tilde{v}_{\rm DAC}$.

**Hint:** Recognize that the negative feedback topology requires that $V_+ = V_- = v_{\rm LPF}$, and write two node equations from which the voltage where the two resistors meet can be eliminated

(B) Using the results of Part (A), find the magnitude and phase of $H_{\rm LPF}(\omega)$.

(C) There is no best design for the low-pass filter to meet the needs of the audio playback system. However, with the appropriate choice of $C_1$, $C_2$ and $R$, the transfer function of one good design will take the form

$$|H_{\rm LPF}(\omega)| = \frac{1}{1 + (\omega/\omega_{\rm LPF})^2}$$

where $\omega_{\rm LPF}$ is a specified frequency. For this design, show that the low-frequency and high frequency asymptotes of $|H_{\rm LPF}(\omega)|$ intersect at $\omega = \omega_{\rm LPF}$, and therefore that $\omega_{\rm LPF}$ is the frequency that delineates the pass band of the low-pass amplifier.

(D) What constraints must be imposed on $C_1$, $C_2$ and $R$ to obtain the low-pass filter transfer function described in Part (C)?

(E) Given that the low-pass filter is to be designed as described in Part (C), use the results of Part (D) to choose values for $C_1$, $C_2$ and $R$ so that $\omega_{\rm LPF} = 2\pi \times 4000$ rad/s. Since the results of

Part (D) under specify $C_1$, $C_2$ and $R$, there is no single correct choice. Therefore, choose $C_1$, $C_2$ and $R$ so that they are easily implemented with the components in the 6.002 lab kit.

(F) Given the choice of $C_1$, $C_2$ and $R$ from Part (E), determine $\omega_{\rm LPF}$, and plot both the log-magnitude and phase of $H_{\rm LPF}(\omega)$ against log-frequency for $2\pi\times10^1$ rad/s $\leq \omega \leq 2\pi\times10^5$ rad/s.

## Problem 11.4: The Power Amplifier

Figure 5 shows the output of the low-pass filter driving the power amplifier, which in turn drives the speaker, or alternatively headphones. The power amplifier is constructed from a high-power op-amp, and is necessary because an ordinary low-power op-amp can not supply the current, and hence the power, required to drive a typical 8 Ω speaker. Because there exists a coupling capacitor at its input, the power amplifier behaves like a highpass filter. In this way, the amplifier is designed to prevent a possibly damaging DC voltage from being applied to the speaker. Such a voltage component could be present in $v_{\rm LPF}$ if, for example, $v_{\rm OFF}$ in the analog-to-digital converter is not properly adjusted to balance the output of the converter.

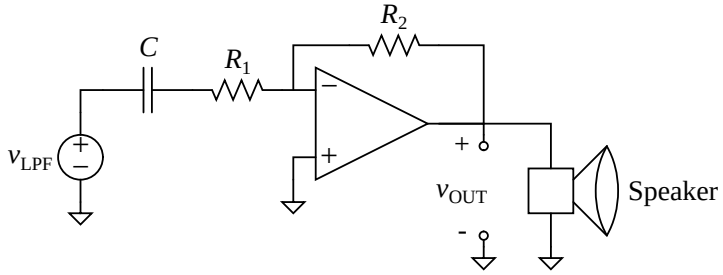


Figure 5: the power amplifier

(A) Assume that the power amplifier operates in sinusoidal steady state with $v_{\rm LPF} = \Re\{\tilde{v}_{\rm LPF}e^{j\omega t}\}$ and $v_{\rm OUT} = \Re\{\tilde{v}_{\rm OUT}e^{j\omega t}\}$ where $\tilde{v}_{\rm LPF}$ and $\tilde{v}_{\rm OUT}$ are complex amplitudes. Find the input-output transfer function $H_{\rm AMP}(\omega)$ of the power amplifier where $H_{\rm AMP}(\omega) \equiv \tilde{v}_{\rm OUT}/\tilde{v}_{\rm LPF}$.

(B) Using the result of Part (A), find the magnitude and phase of $H_{\rm AMP}(\omega)$.

(C) Let $\omega_{\rm AMP}$ be the frequency at which the low-frequency and high-frequency asymptotes of $|H_{\rm AMP}(\omega)|$ intersect. Determine $\omega_{\rm AMP}$ in terms of $R_1$, $R_2$ and $C$.

(D) Choose values for $R_1$, $R_2$ and $C$ so that $\omega_{\rm AMP} \leq 2\pi\times100$Hz, and $|H_{\rm AMP}(\omega)| = 1$ for $\omega \gg \omega_{\rm AMP}$. Since these conditions alone under specify $R_1$, $R_2$ and $C$, there is no single correct choice. Therefore, choose values for $R_1$, $R_2$ and $C$ that are easily implemented with the components in the 6.002 lab kit.

(E) If the original analog signal is recorded with a reduced amplitude, then the power amplifier must compensate by providing greater than unity gain. To provide this gain, $R_2$ is implemented with a fixed resistor in series with a potentiometer. Design such a modification that provides a variable gain of 1 to 5. Note that the 6.002 lab kit has a limited number of potentiometers.

### Problem 11.5: Connecting The Blocks

In the complete audio playback system the output of the digital-to-analog converter is connected directly to the input of the low-pass filter, and the output of the low-pass filter is connected directly to the input of the power amplifier, as shown in Figure 1. Thus, the filter loads the converter, and the amplifier loads the filter. Explain why this loading could be ignored in Problems 2, 3 and 4. That is, explain why the converter, filter and amplifier may each be analyzed and designed in isolation.