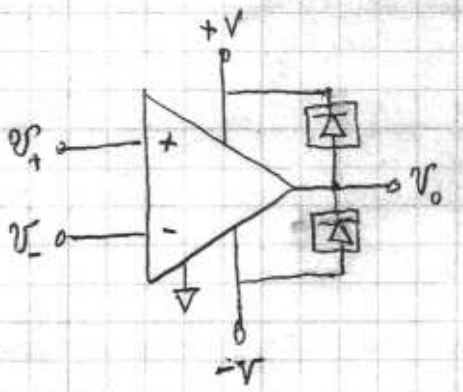
NOTES FOR 6.002 LECTURE #22, MAY 1, 2003

OPERATIONAL AMPLIFIERS IN SATURATION: THE LIMITS ON OUTPUT VOLTAGE ARE EASILY MODELED BY ADDING IDEAL DIODES:



WHEN $V > v_o > -V$ BOTH DIODES ARE REVERSE BIASED OR OFF

WHEN $v_o = +V$ THE UPPER DIODE CLOSES (CONDUCTS) AND CLAMPS v_o AT THIS LEVEL.

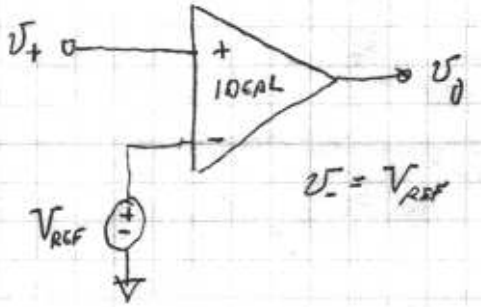
WHEN $v_o = -V$ THE LOWER DIODE CLOSES AND CLAMPS v_o AT THIS LEVEL

IN REALITY THE OP-AMP SATURATES AT SLIGHTLY SMALLER VALUES OF $|v_o|$. THIS DIFFERENCE CAN BE IGNORED IN MOST CASES.

THE MODEL ABOVE APPLIES - AT LEAST IMPLICITLY IN APPLICATIONS SUCH AS SCHMITT TRIGGERS AND OSCILLATORS.

THE NEXT THREE PAGES ARE REPRINTS FROM LECTURE #21

AN OP-AMP CAN BE USED AS A COMPARATOR BY EXPLOITING THE LIMITS ($\pm V_S$, THE SUPPLY VOLTAGES) ON THE OUTPUT VOLTAGE.

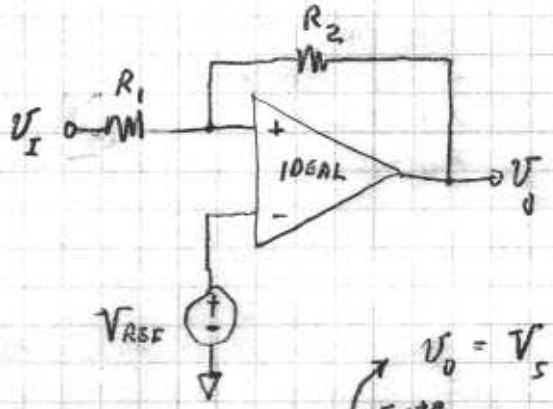


IF $v_+ < V_{REF}$, $v_0 = -V_S$

IF $v_+ > V_{REF}$, $v_0 = +V_S$

SLEW RATE IS VERY HIGH ($\sim 20\ V/\mu sec$)

CONSIDER THE EFFECT OF POSITIVE FEEDBACK AROUND THE COMPARATOR:



$$v_+ = v_I \frac{R_2}{R_1+R_2} + v_0 \frac{R_1}{R_1+R_2} \quad \text{(SUPERPOSITION)}$$

IF $v_+ > V_{REF}$, $v_0 = V_S$

IF $v_+ < V_{REF}$ $v_0 = -V_S$

} TWO STABLE STATES

$v_0 = V_S$ ($v_+ > V_{REF}$) $\rightarrow v_+ < V_{REF}$

$v_0 = -V_S$

ASSUME CIRCUIT IS IN $v_0 = -V_S$. WHAT IS THE CONSTRAINT ON v_I TO STAY THERE?

$$v_+ < V_{REF} \quad \text{OR:} \quad \left(v_I \frac{R_2}{R_1+R_2} - V_S \frac{R_1}{R_1+R_2}\right) < V_{REF}$$

EQUIVALENTLY: $$v_I < V_{REF}\left(\frac{R_1+R_2}{R_2}\right) + V_S \frac{R_1}{R_2}$$

ASSUME CIRCUIT IS IN THE STATE $v_0 = +V_S$. THE CORRESPONDING CONDITION TO STAY THERE IS:

$$v_+ > V_{REF} \quad \text{OR:} \quad v_I > V_{REF}\left(\frac{R_1+R_2}{R_2}\right) - V_S \frac{R_1}{R_2}$$

IN SUMMARY:

CONDITION FOR STAYING IN STATE:

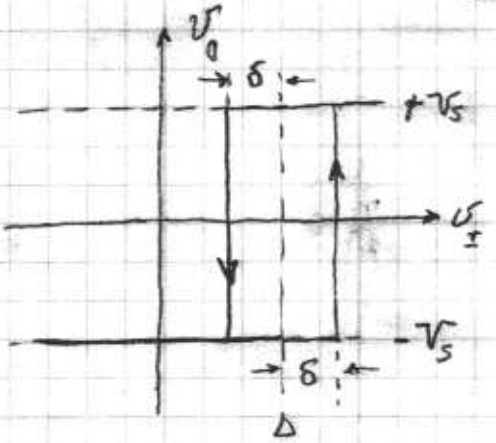
IN $+V_S$ STATE: $v_I > V_{REF}\left(\frac{R_1+R_2}{R_2}\right) - V_S\frac{R_1}{R_2}$

(v_I INCREASE ; v_I DECREASES)

IN $-V_S$ STATE: $v_I < V_{REF}\left(\frac{R_1+R_2}{R_2}\right) + V_S\frac{R_1}{R_2}$

Δ ; $\pm\delta$

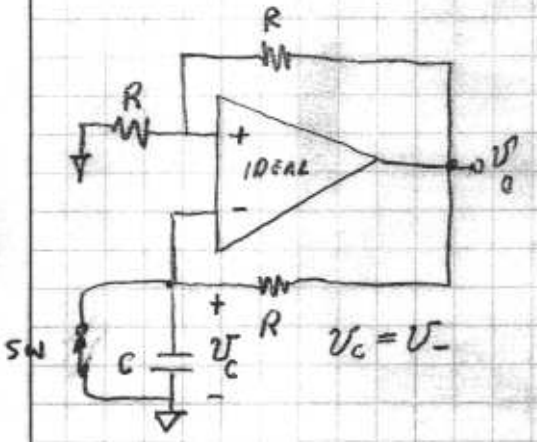
GRAPHICALLY:



HYSTERESIS BY INTENTION

A MEMBER OF A FAMILY OF CIRCUITS KNOWN AS "SCHMITT TRIGGERS"

THIS CIRCUIT, WITH BISTABILITY PRODUCED BY POSITIVE FEEDBACK, CAN EASILY BE MADE INTO A SIGNAL GENERATOR OR OSCILLATOR:



INITIALLY THE SWITCH IS CLOSED

ASSUME CIRCUIT IS IN + STATE I.E. $v_0 = +V_S$

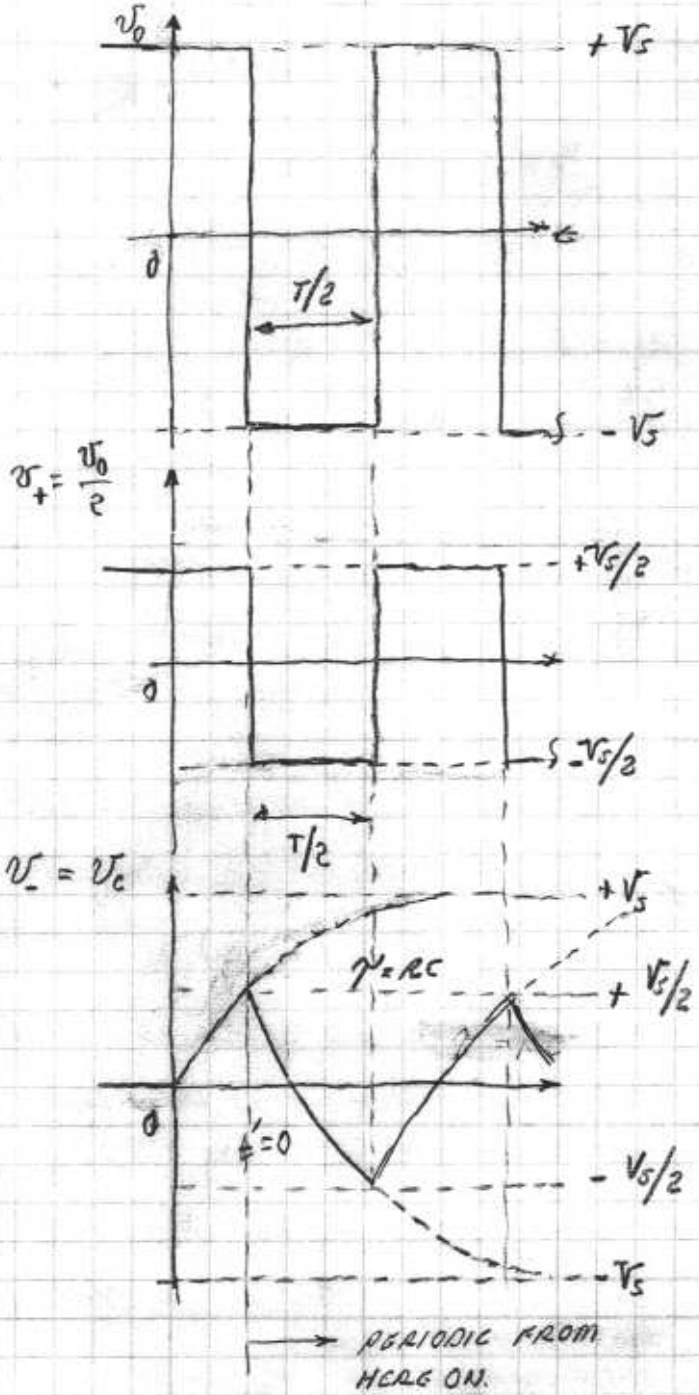
(WITH SWITCH CLOSED CIRCUIT LOOKS LIKE SCHMITT TRIGGER WITH $V_{REF} = 0$)

LET SWITCH OPEN AT $t=0$ v_C INCREASES TOWARD $+V_S$.

WHEN IT REACHES $\frac{V_S}{2}$ $v_C > v_+$ AND STATE CHANGES TO $v_0 = -V_S$

v_C NOW DECREASE TOWARD $-V_S$, WITH THE STATE CHANGING AGAIN WHEN IT REACHES $-\frac{V_S}{2}$ MAKING $v_C < v_+$

AND THE CYCLE CONTINUES



TO DETERMINE THE PERIOD FOCUS ON INTERVAL MARKED $T/2$ AND LET $t' = 0$ AT START OF THIS INTERVAL. BY INSPECTION:

$$v_c(t') = -V_s + \frac{3}{2} V_s e^{-t'/\tau}$$

THIS INTERVAL ENDS WHEN

$v_c(t') = -V_s/2$ OR WHEN

$e^{-t'/\tau} = \frac{1}{3}$ AT THIS TIME $t' = T/2$

$$\frac{T}{2} = \tau \ln 3$$

$$T = 2\tau \ln 3$$

THE CLOCK IN LAB #4 IS DIFFERENT IN DETAIL, BUT RELIES ON POSITIVE FEEDBACK AROUND AN AMPLIFIER, A FET INVERTER, WHICH SATURATES AT BOTH ENDS OF THE TRANSFER CHARACTERISTIC.

THE ANALYSIS PROCEEDS AS IN THE CIRCUIT ABOVE.