OPERATIONAL AMPLIFIERS IN SATURATION: THE LIMITS ON OUTPUT
VOLTAGE ARE EASILY MODELED BY ADDING 100mA DIODES:

\[ V_+ > V_o > -V \] BOTH DIODES
ARE REVERSE BIAS OR OFF

WHEN \[ V = +V \] THE UPPER DIODE
CLOSES (CONDUCTS) AND CLAMPS
\[ V_o \] AT THIS LEVEL.

WHEN \[ V_o = -V \] THE LOWER DIODE
CLOSES AND CLAMPS \[ V_o \] AT THIS LEVEL.

In reality the op-amp saturates at slightly smaller values of
\( V \). This difference can be ignored in most cases.

The model above applies - at least implicitly in applications
such as Schmitt triggers and oscillators.

The next three pages are reprints from Lecture #21.
An op-amp can be used as a comparator by exploiting the limits ($\pm V_S$, the supply voltages) on the output voltage.

\[ \begin{align*} 
U_+ & < V_{\text{ref}} \quad U_0 = -V_S \\
U_+ & > V_{\text{ref}} \quad U_0 = +V_S \\
\text{Slew rate is very high} & \quad (\sim 20 \text{ V/\mu s})
\end{align*} \]

Consider the effect of positive feedback around the comparator:

\[ \begin{align*} 
U_+ & = U_0 \frac{R_2}{R_1 + R_2} + U_0 \frac{R_1}{R_1 + R_2} \quad (\text{superposition}) \\
\text{if } U_+ & > V_{\text{ref}} \quad U_0 = V_S \\
\text{if } U_+ & < V_{\text{ref}} \quad U_0 = -V_S \\
\end{align*} \]

Two stable states

Assume circuit is in $U_0 = -V_S$. What is the constraint on $U_+$ to stay there?

\[ U_+ < V_{\text{ref}} \quad \text{or:} \quad \left( U_0 \frac{R_2}{R_1 + R_2} - V_S \frac{R_1}{R_1 + R_2} \right) < V_{\text{ref}} \]

Equivalently:

\[ U_+ < V_{\text{ref}} \left( \frac{R_1 + R_2}{R_2} \right) + V_S \frac{R_1}{R_2} \]

Assume circuit is in the state $U_0 = +V_S$. The corresponding condition to stay there is:

\[ U_+ > V_{\text{ref}} \quad \text{or:} \quad \left( U_0 \frac{R_2}{R_1 + R_2} + V_S \frac{R_1}{R_2} \right) > V_{\text{ref}} \]
**IN SUMMARY:**

**CONDITION FOR STAYING IN STATE:**

\[
\begin{align*}
\text{IN } +V_S \text{ state:} & \quad U_c^+ > V_{\text{REF}} \left( \frac{R_1 + R_2}{R_2} \right) = U_S \frac{R_1}{R_2} \\
\text{IN } -V_S \text{ state:} & \quad U_c^- < -V_{\text{REF}} \left( \frac{R_1 + R_2}{R_2} \right) + U_S \frac{R_1}{R_2}
\end{align*}
\]

\( \Delta \) decreases

**GRAPHICALLY:**

**Hysteresis by Inception**

A member of a family of circuits known as "Schmitt Triggers".

**THE CIRCUIT, WITH BISTABILITY PRODUCED BY POSITIVE FEEDBACK,**

**CAN EASILY BE MADE INTO A SIGNAL GENERATOR OR OSCILLATOR:**

Initially the switch is closed.

Assume circuit is IN + state i.e. \( U^+_0 = +V_S \)

(WITH SWITCH CLOSED CIRCUIT LOOKS LIKE SCHMITT TRIGGER WITH \( V_{\text{REF}} = 0 \))

Let switch open at \( t = 0 \) \( U_c \) increases toward +V_s.

When it reaches \( \frac{V_S}{2} \) \( U_c \) increases \( U_0 = -V_S \) and

state changes to \( U_0 = -V_S \)

\( U_c \) now decreases toward \(-V_S\), with

the state changing again when it reaches \(-\frac{V_S}{2}\) making \( U_c > U_0 \)

and the cycle continues.
To determine the period $f_0$ on interval marked $T/2$ and let $t' = 0$ at start of this interval.

By inspection:

$$V_c(t') = V_0 + \frac{3}{2} V_5 e^{-t'/T}$$

This interval ends when

$$V_c(t') = -\frac{V_0}{2}$$

or when

$$e^{-t'/T} = \frac{1}{3}$$

At this time

$$t' = T/2$$

$$T = 2 \pi \ln 3$$

The clock in Lab #4 is different in detail, but relies on positive feedback around an amplifier, a FET inverter, which saturates at both ends of the transfer characteristic.

The analysis proceeds as in the circuit above.