## Introduction

This homework assignment focuses on the analysis and design of a system for playing back a digitally-stored audio signal. Additionally, this assignment serves as the pre-lab exercises for Lab #4, which will involve the construction, testing and demonstration of the audio playback system. *Consequently, you should save a copy of your results for use during Lab #4.*

A block diagram of the audio playback system is shown in Figure 1. At the center of the system is a digital memory in which 32,768 samples of the audio signal are stored. Each sample in the memory has a unique numerical address between 0 and 32,767, inclusive. Consecutive samples are stored at consecutive addresses. To obtain 32,768 consecutive samples of the audio signal, 4.096 seconds of continuous analog audio signal are first sampled at an 8-kHz rate. The analog audio samples are then digitized by an 8-bit analog-to-digital converter. That is, the samples are quantized to take on one of 256 possible discrete digital values between 0 and 255, inclusive. Here, the digital value of 0 corresponds to the most positive audio signal level, and the digital value of 255 corresponds to the most negative audio signal level. The resulting digital data is then written into the memory.

To retrieve the stored audio signal samples in sequence at the proper rate, the memory is addressed by a counter which counts from 0 to 32,767 at an 8-kHz rate established by an external clock. After counting to 32,767 the counter returns to 0, and the retrieval process repeats itself. As the memory address increments, the corresponding data appears at the memory output. This data is converted back to an analog voltage in a piecewise constant manner by a digital-to-analog converter.

During the course of recording and playing back the analog audio signal, the signal is sampled in time, quantized in amplitude, and reconstructed in a piecewise constant manner. As you will learn in 6.003, this process introduces undesirable high-frequency components into the signal. To minimize the perceived impact of these components, the signal is filtered by a low-pass filter after it is reconstructed by the digital-to-analog converter. Finally, the signal is amplified by a power amplifier which in turn drives a speaker, or alternatively headphones. The power amplifier is
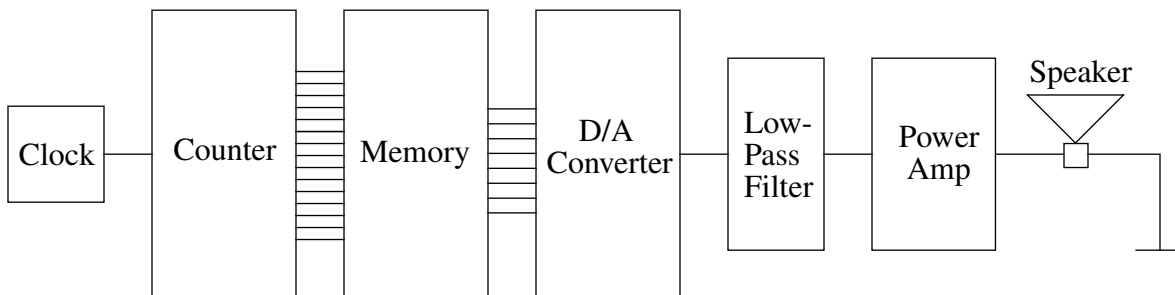


Figure 1: block diagram of the audio playback system

necessary because the low-pass filter is not capable of driving a speaker directly.

In the course of this homework assignment you will analyze and design four of the functional blocks shown in Figure 1. These blocks are the clock, the digital-to-analog converter, the low-pass filter and the power amplifier. In Lab #4, you will construct these blocks and verify that they perform as desired. Then, you will combine them with the counter, the read-only memory and the speaker to construct and demonstrate the entire audio play-back system. Since you will construct the system from the components in your 6.002 lab kit, your design of the blocks must account for the fact that the available components are limited.

## Problem 11.1:    The Clock

The circuit shown in Figure 2 is the system clock, which is a square-wave oscillator followed by a CMOS inverter; the inverter functions only as a buffer. The oscillator is constructed from another CMOS inverter, a resistor and a capacitor. Both inverters are powered between the positive supply voltage $V_S$ and ground, and both exhibit the hysteretic input-output characteristic defined in the figure. The inverters are otherwise ideal.

(A) Assume that $v_{CAP}$ has just charged up to $V_H$ so that $v_{OSC}$ has just switched to 0 V. How much time elapses before $v_{CAP}$ decays to $V_L$, which in turn causes $v_{OSC}$ to switch to $V_S$?

**Answer:**    As shown in the Figure 3, the capacitor now begins to discharge from $V_H$ toward zero. The capacitor voltage is given by

$$v_{CAP} = V_H \cdot e^{-t/RC}$$

We want to solve for the time at which $v_{CAP} = V_L$. This time is denoted by $T_2$ in the figure.

$$V_L = V_H \cdot e^{-T2/RC}$$

Solve to get:

$$T_2 = RC \cdot \ln \frac{V_H}{V_L}$$

(B) Assume that $v_{CAP}$ has just decayed to $V_L$ so that that $v_{OSC}$ has just switched to $V_S$. How much time elapses before $v_{CAP}$ charges up to $V_H$, which in turn causes $v_{OSC}$ to switch to 0 V?
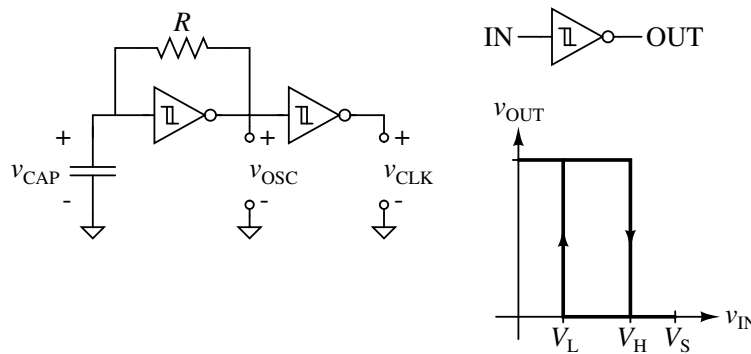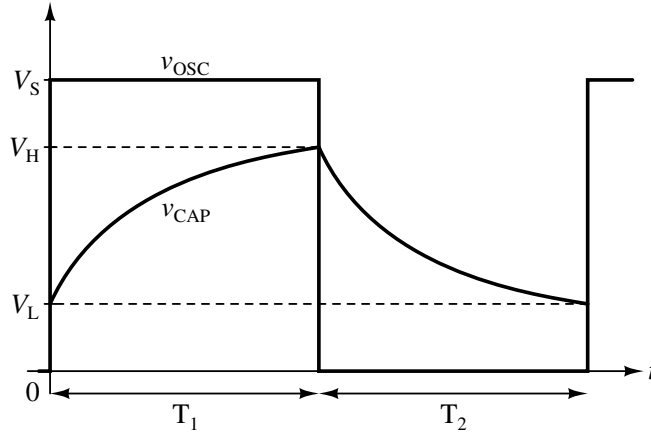


Figure 2: the system clock

Figure 3: Finding $T_1$ and $T_2$

**Answer:**     Now the capacitor starts to charge from $V_L$ toward $V_S$. The solution for the capacitor voltage is:

$$v_{\text{CAP}} = V_S + (V_L - V_S) \cdot e^{-t/RC}$$

We want to solve for the time at which $v_{\text{CAP}}$ reaches $V_H$. This time is denoted by $T1$ in the figure.

$$V_H = V_S + (V_L - V_S) \cdot e^{-T_1/RC}$$

Solve to get

$$T_1 = RC \cdot \ln \frac{V_S - V_L}{V_S - V_H}$$

(C) Determine the frequency of the oscillator in terms of $R$, $C$, $V_L$, $V_H$ and $V_S$.

**Answer:**     The period $T$ of the oscillator is

$$T = T_1 + T_2 = RC \cdot \ln \frac{(V_S - V_L)V_H}{(V_S - V_H)V_L}$$

The frequency $f$ is the inverse of the period and is given by

$$f = \frac{1}{T} = \frac{1}{RC \cdot \ln \frac{(V_S-V_L)V_H}{(V_S-V_H)V_L}}$$

(D) Assume that $V_L = 1.8V$, $V_H = 3.0V$ and $V_S = 5.0V$. Choose values for $R$ and $C$ so that the oscillator oscillates at or very near 8-kHz. Since oscillator frequency alone under-specifies $R$ and $C$, there is no single correct choice. Therefore, choose values for $R$ and $C$ that are easily implemented with the components in the 6.002 lab kit.

**Answer:**     $f = 8$ kHz is equivalent to $T = 1/f = 125\mu s$. Pick $C = .0047\mu F$, we solve for $R$ using the equation in part (C):

$$R = \frac{T}{C \cdot \ln \frac{(V_S-V_L)V_H}{(V_S-V_H)V_L}} = 27\text{k}\Omega$$

which is a standard resistor value.

(E) For the choice of $R$ and $C$ from Part (D), sketch and clearly label a single graph that displays $v_{\mathrm{CAP}}$, $v_{\mathrm{OSC}}$ and $v_{\mathrm{CLK}}$ as a function of time over one period of oscillation.

**Answer:** Using equations developed in (A) and (B) we get $T_1 = 59.6\mu s$ and $T_2 = 64.8\mu s$. We notice that $T_1 \neq T_2$. This does not affect the operation of the clock because the counter is triggered by either the rising or the falling edge, but not both.
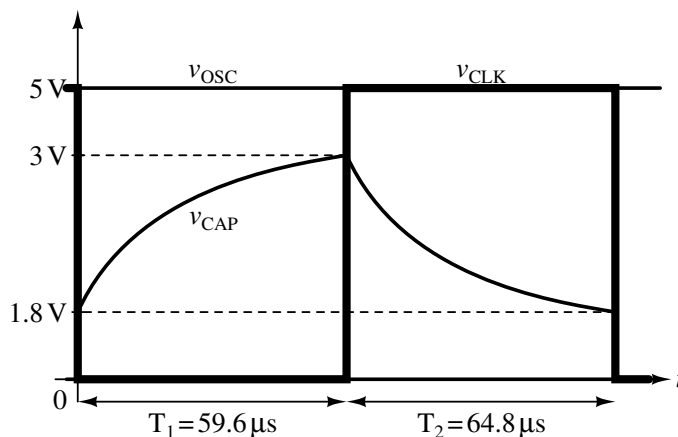


Figure 4: Evaluating $T_1$ and $T_2$

## Problem 11.2: The Digital-To-Analog Converter

The circuit shown in Figure 5 is the digital-to-analog converter. The voltage sources $v_{\mathrm{DB0}}$ through $v_{\mathrm{DB7}}$ represent the voltages supplied by the eight data bits of the digital memory, DB0 through DB7. These voltages will be approximately 5 V when the corresponding data bit is a logical high, and approximately 0 V when the corresponding data bit is a logical low. The voltage $v_{\mathrm{OFF}}$, which is set by a potentiometer, is an offset voltage that is used to center the output of the converter around 0 V. Assume that the op-amp in the converter is ideal.

(A) Determine $v_{\mathrm{DAC}}$ as a function of $v_{\mathrm{DB0}}$ through $v_{\mathrm{DB7}}$, and $v_{\mathrm{OFF}}$.

**Hint:** Use superposition, and exploit the repetitive nature of the resistive network. It's easiest to start with $v_{\mathrm{DB7}}$.

**Answer:** The resistive network at the negative terminal of the op-amp is called an R-2R ladder. We can solve by using the superposition principle. We turn off all the sources except one, say $v_{\mathrm{DB0}}$, and then appyly Thevenin's theorem repeatedly across each "T" node from left to right, as shown in Figure 6

As demonstrated above, the Thevenin voltage is cut by half across each "T" node, and the Thevenin resistance is always $R_1$. Eventually we simplify the network into one source in series with one resistor at the negative terminal of the op-amp. Since we have turned $v_{\mathrm{OFF}}$ off, what we have now is a simple inverting configuration, and the output is given by

$$v_{\mathrm{DAC}} = -\frac{R_2}{3R_1}\frac{v_{\mathrm{DB0}}}{2^8}$$
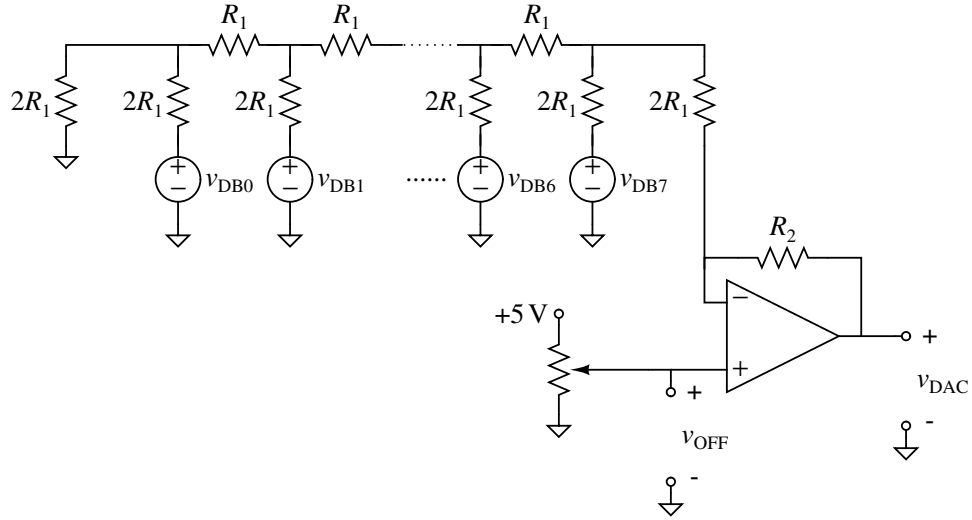
Figure 5: the digital-to-analog converter

Repeating the same procedure for each $v_{\mathrm{DB}i}$, with $v_{\mathrm{OFF}}$ set to zero, we arrive at the following equation:

$$
\begin{aligned}
v_{\mathrm{DAC}} &= -\frac{R_2}{3R_1} \sum_{i=0}^{7} \frac{v_{\mathrm{DB}i}}{2^{8-i}} \\
&= -\frac{R_2}{3R_1} \sum_{i=0}^{7} \frac{2^i}{2^8} v_{\mathrm{DB}i}
\end{aligned}
$$

Next we consider the effect of $v_{\mathrm{OFF}}$, when all of $v_{\mathrm{DB}i}$'s are set to zero. The resistance $R_{\mathrm{T}}$ looking into the R-2R ladder is $R_{\mathrm{T}} = R_1 + 2R_1 = 3R_1$, as shown in Figure 6. It then follows that

$$
v_{\mathrm{DAC}} = v_{\mathrm{OFF}} \left( 1 + \frac{R_2}{3R_1} \right)
$$

Finally, the total solution is

$$
v_{\mathrm{DAC}} = -\frac{R_2}{3R_1} \sum_{i=0}^{7} \frac{2^i}{2^8} v_{\mathrm{DB}i} + v_{\mathrm{OFF}} \left( 1 + \frac{R_2}{3R_1} \right)
$$

(B) With $v_{\mathrm{OFF}} = 0\mathrm{V}$, the output of the digital-to-analog converter should span the range of 0 V to -2.5 V. Thus, the output of the converter should be given by

$$
v_{\mathrm{DAC}} = -2.5 \text{ V} \sum_{i=0}^{7} \frac{2^i}{255} \mathrm{DB}i
$$

where each data bit $\mathrm{DB}i$ takes on the numerical value of 1 when high and 0 when low. In this manner, each successive data bit from DB0 to DB7 is given a voltage weighting twice that of the preceding data bit, making it possible for the converter to output voltages from 0 V to -2.5 V in steps of -2.5/255 V. Given this, determine $R_2$ in terms of $R_1$.
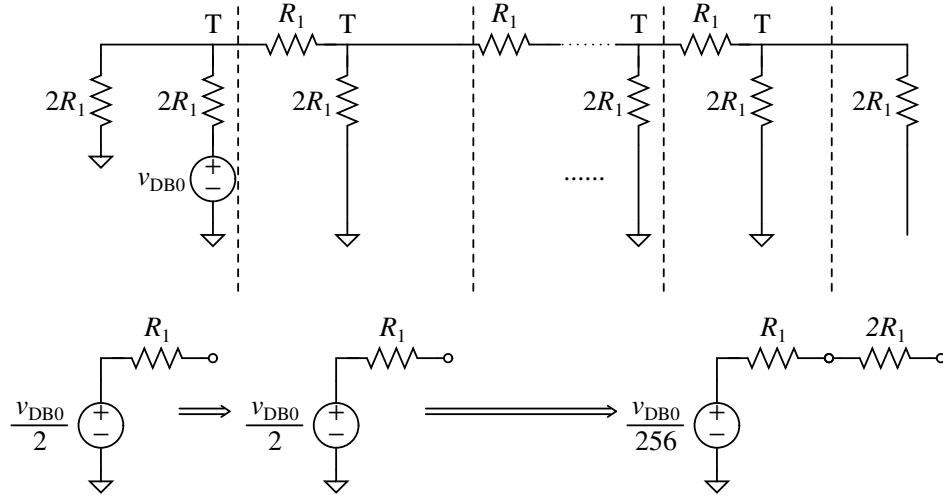
Figure 6: Thevenin equivalent process

The input voltage rating of the speaker is approximately $\pm 1.25$V. Since the low-pass filter has unity voltage gain over the frequency range of interest, the output range of the digital-to-analog converter must be designed to match the speaker rating. This is why the range is chosen to be 0 V to -2.5 V, with $v_{\text{OFF}} = 0$. Note further that the output range of the converter is negative. This is because the converter is based upon the inverting amplifier configuration.

**Answer:**   The $v_{\text{DAC}}$ equation provided must equal the one derived in Part (A). When all the bits are on

$$v_{\text{DAC}} = -2.5\text{V} = -\frac{R_2}{3R_1}\frac{255}{256}5\text{V}$$

Solving for $R_2$ we get

$$R_2 = \frac{3 \cdot 256}{510}R_1 = 1.51R_1$$

(C) The role of $v_{\text{OFF}}$ is to offset the output of the digital-to-analog converter so that it is centered around 0 V. That is, with DB0 through DB7 all low, $v_{\text{DAC}}$ should be 1.25 V, and with DB0 through DB7 all high, $v_{\text{DAC}}$ should be -1.25 V. Given this, what must be the value of $v_{\text{OFF}}$?

**Answer:**   Setting all bits to 0, we get

$$v_{\text{DAC}} = 1.25 = v_{\text{OFF}}\left(1 + \frac{R_2}{3R_1}\right) = v_{\text{OFF}}\left(1 + \frac{256}{510}\right)$$

This gives us

$$v_{\text{OFF}} = 0.83\text{V}$$

(D) Assume that $R_1 = 10\text{k}\Omega$. Use the result of Part (B) to determine $R_2$.

**Answer:**   $R_2$ is found by directly applying the equation found in Part (B):

$$R_2 = 1.51R_1 = 15.1\text{k}\Omega$$

**Problem 11.3:    The Low-Pass Filter**

The circuit shown in Figure 7 is the low-pass filter. It is a second-order filter, and is driven by the output of the digital-to-analog converter. Its purpose is to remove the high-frequency components of the audio signal that result from the sampling, quantization and reconstruction of that signal. Assume that the op-amp in the filter is ideal.
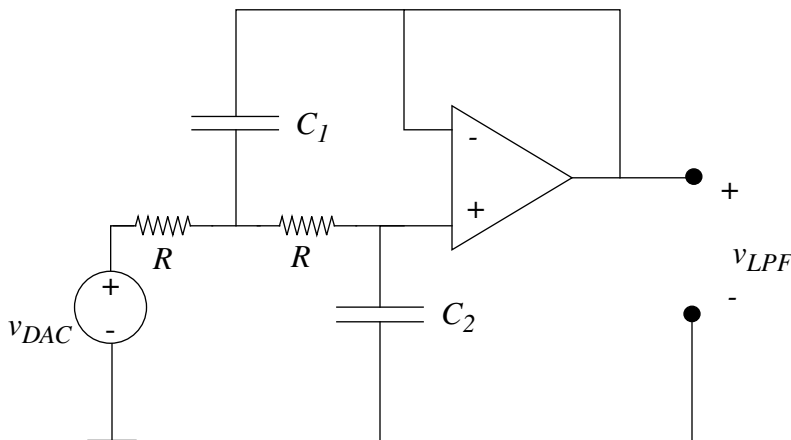


Figure 7: the low-pass filter

(A) Assume that the low-pass filter operates in sinusoidal steady state with $v_{\mathrm{DAC}} = \Re\{\tilde{v}_{\mathrm{DAC}}e^{j\omega t}\}$ and $v_{\mathrm{LPF}} = \Re\{\tilde{v}_{\mathrm{LPF}}e^{j\omega t}\}$ where $\tilde{v}_{\mathrm{DAC}}$ and $\tilde{v}_{\mathrm{LPF}}$ are complex amplitudes. Find the input-output transfer function $H_{\mathrm{LPF}}(\omega)$ of the filter where $H_{\mathrm{LPF}}(\omega) \equiv \tilde{v}_{\mathrm{LPF}}/\tilde{v}_{\mathrm{DAC}}$.

**Hint:**    Recognize that the negative feedback topology requires that $V_+ = V_- = v_{\mathrm{LPF}}$, and write two node equations from which the voltage where the two resistors meet can be eliminated

**Answer:**    Unfortunately, there is no simple way to solve this circuit. We are forced to return to the Node Method. There are three nodes in the circuit, but the Ideal Op-Amp Model allows us to assume that $v_+ = v_- = v_{\mathrm{LPF}}$. By using this simplification, we can avoid writing a node equation for the output node. I am de ning the internal node as $\tilde{e}$.

For the $v_+$ node:

$$\frac{\tilde{v}_{\mathrm{LPF}}}{\frac{1}{j\omega C_2}} + \frac{\tilde{v}_{\mathrm{LPF}} - \tilde{e}}{R} = 0.$$

For the $v_-$ node:

$$\frac{\tilde{v}_{\mathrm{LPF}} - \tilde{e}}{\frac{1}{j\omega C_1}} + \frac{\tilde{v}_{\mathrm{LPF}} - \tilde{e}}{R} + \frac{\tilde{v}_{\mathrm{DAC}} - \tilde{e}}{R} = 0$$

We choose to solve the first equation for $\tilde{e}$ and substitute into the second. Mathematically, it is irrelevant how we solve, but practically, it tends to be easier to solve the most simple equation first, and substitute into more and more complicated expressions.

$$\tilde{e} = \tilde{v}_{\mathrm{LPF}}(1 + j\omega RC_2)$$

Substituting in for $\tilde{e}$ and factoring out a $\tilde{v}_{\mathrm{LPF}}$ gives us:

$$\tilde{v}_{\mathrm{LPF}} \left( \frac{(1 + j\omega RC_2) - 1}{\frac{1}{j\omega C_1}} + \frac{(1 + j\omega RC_2) - 1}{R} + \frac{1 + j\omega RC_2}{R} \right) = \frac{\tilde{v}_{\mathrm{DAC}}}{R}$$

Solving for $\frac{\tilde{v}_{\mathrm{LPF}}}{\tilde{v}_{\mathrm{DAC}}}$ and we have:

$$H_{\mathrm{LPF}}(\omega) = \frac{\tilde{v}_{\mathrm{LPF}}}{\tilde{v}_{\mathrm{DAC}}} = \frac{1}{1 - \omega^2 R^2 C_1 C_2 + 2j\omega RC_2}$$

(B) Using the results of Part (A), find the magnitude and phase of $H_{\mathrm{LPF}}(\omega)$.

**Answer:**

$$|H_{\mathrm{LPF}}(\omega)| \; = \; \frac{1}{\sqrt{(1 - \omega^2 R^2 C_1 C_2)^2 + (2\omega RC_2)^2}}$$

$$\angle H_{\mathrm{LPF}}(\omega) \; = \; 0 - \tan^{-1} \frac{2\omega RC_2}{1 - \omega^2 R^2 C_1 C_2}$$

(C) There is no best design for the low-pass filter to meet the needs of the audio playback system. However, with the appropriate choice of $C_1$, $C_2$ and $R$, the transfer function of one good design will take the form

$$|H_{\mathrm{LPF}}(\omega)| = \frac{1}{1 + (\omega/\omega_{\mathrm{LPF}})^2}$$

where $\omega_{\mathrm{LPF}}$ is a specified frequency. For this design, show that the low-frequency and high frequency asymptotes of $|H_{\mathrm{LPF}}(\omega)|$ intersect at $\omega = \omega_{\mathrm{LPF}}$, and therefore that $\omega_{\mathrm{LPF}}$ is the frequency that delineates the pass band of the low-pass amplifier.

**Answer:** The low and high frequency asymptotes are calculated by including only the lowest and highest order $\omega$ terms respectively. Continue to simplify in this manner until you are left with only one term containing $\omega$.

For $\omega \ll \omega_{\mathrm{LPF}}$ we drop the $\omega$ term because it is much less than 1. The result is very simple:

$$H_{\mathrm{LPF}}(\omega \ll \omega_{\mathrm{LPF}}) \approx 1$$

For $\omega \gg \omega_{\mathrm{LPF}}$ we drop the 1 term because it is much less than $\omega$. The result is still simple:

$$H_{\mathrm{LPF}}(\omega \gg \omega_{\mathrm{LPF}}) \approx \frac{1}{(\omega/\omega_{\mathrm{LPF}})^2}$$

Solving for the intercept of these equations gives the expected $\omega = \omega_{\mathrm{LPF}}$. This is known as the cut-off frequency.

(D) What constraints must be imposed on $C_1$, $C_2$ and $R$ to obtain the low-pass filter transfer function described in Part (C)?

**Answer:** Our current equation for $|H_{\text{LPF}}(\omega)|$ does not look much like our desired result, but let's try multiplying out the denominator.

$$|H_{\text{LPF}}(\omega)| = \frac{1}{\sqrt{1 - 2\omega^2 R^2 C_1 C_2 + (\omega^2 R^2 C_1 C_2)^2 + 4\omega^2 R^2 C_2^2}}$$

If we let $C_1 = C_2 = C$, then we can easily factor that equation.

$$|H_{\text{LPF}}(\omega)| = \frac{1}{\sqrt{1 + 2\omega^2 R^2 C^2 + (\omega^2 R^2 C^2)^2}} = \frac{1}{\sqrt{(1 + \omega^2 R^2 C^2)^2}} = \frac{1}{1 + \omega^2 R^2 C^2}$$

This final form looks a lot more like what we want. We can see that $\omega_{\text{LPF}} = 1/(RC)$.

(E) Given that the low-pass filter is to be designed as described in Part (C), use the results of Part (D) to choose values for $C_1$, $C_2$ and $R$ so that $\omega_{\text{LPF}} = 2\pi \times 4000$ rad/s. Since the results of Part (D) under specify $C_1$, $C_2$ and $R$, there is no single correct choice. Therefore, choose $C_1$, $C_2$ and $R$ so that they are easily implemented with the components in the 6.002 lab kit.

**Answer:** We see that $RC = 1/(2\pi \times 4000) \approx 3.98 \times 10^{-5}$. To choose a good value for $R$ and $C$ we need to consider the parasitic elements in the circuit and the device non-idealities.

There are parasitic capacitances between the pins in the protoboard. Those tend to be on the order of single picofarads. We need our $C$ value to be much larger than that to be resistant to interference.

The resistor choice is effected by the presence of source resistances and input and output resistances of the op-amps. In addition there are parasitic inductances. If the resistance is too small, the parasitic $RLC$ circuits may be under-damped and cause ringing. In general we choose a resistance of a few k$\Omega$. We have an $R = 3.9$k$\Omega$ lets try that.

$R = 3.9$k$\Omega$ requires that $C = .0102\mu$F. Since this is much larger than a picofarad, and we have a $.01\mu$F capacitor in our kit, it seems that these values are a good choice.

Just to check, we see that our $RC = 3.9 \times 10^{-5}$. This is about 2% off of the desired frequency, which is much less than the error of either the resistor or the capacitor.

(F) Given the choice of $C_1$, $C_2$ and $R$ from Part (E), determine $\omega_{\text{LPF}}$, and plot both the log-magnitude and phase of $H_{\text{LPF}}(\omega)$ against log-frequency for $2\pi \times 10^1$ rad/s $\leq \omega \leq 2\pi \times 10^5$ rad/s.

**Answer:** From above we see that $\omega_{\text{LPF}} = 2.56 \times 10^4 = 2\pi \times 4081$ rad/s.

Bode Diagrams for the Low Pass Filter
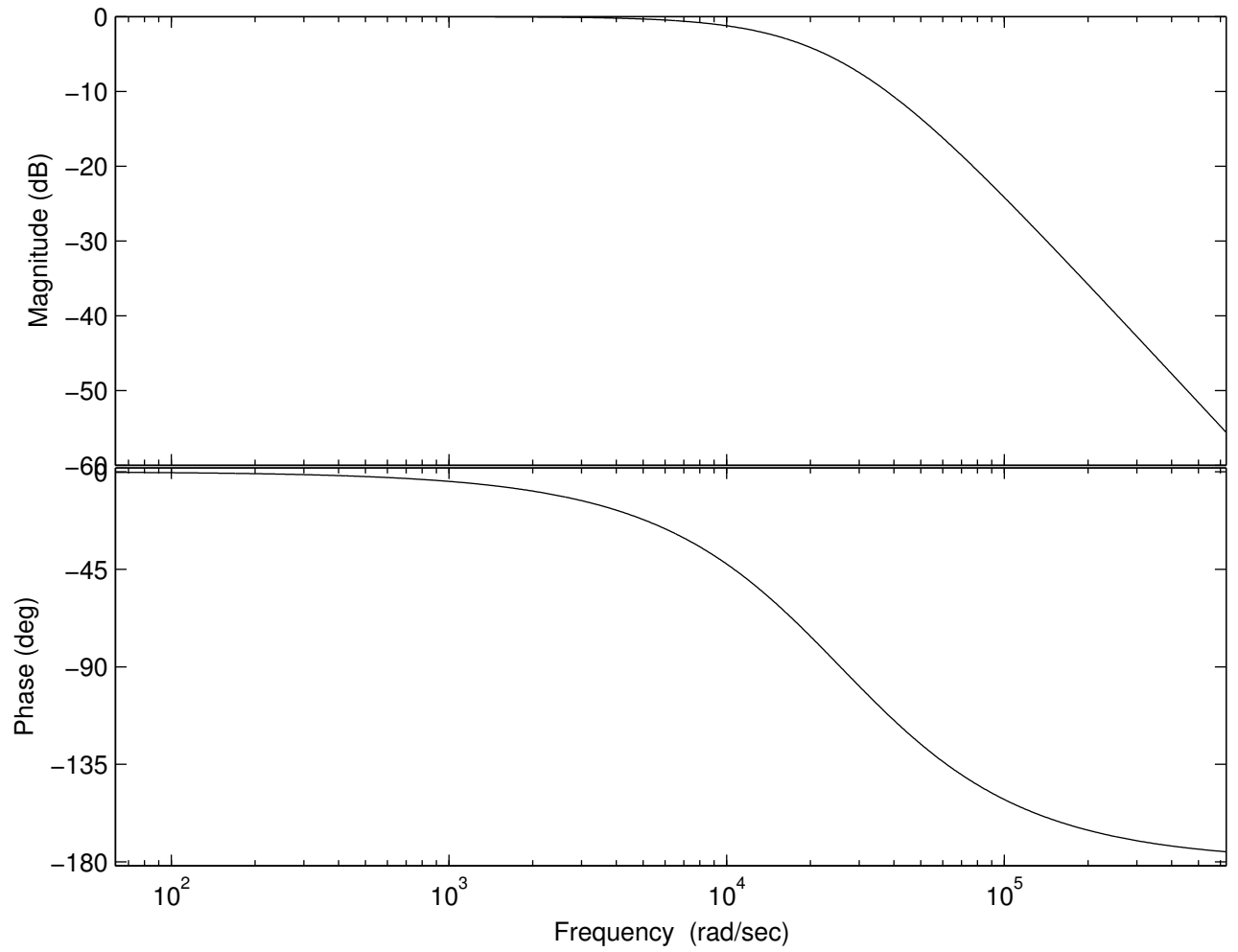
**Problem 11.4:    The Power Amplifier**

Figure 8 shows the output of the low-pass filter driving the power amplifier, which in turn drives the speaker, or alternatively headphones. The power amplifier is constructed from a high-power op-amp, and is necessary because an ordinary low-power op-amp can not supply the current, and hence the power, required to drive a typical 8 $\Omega$ speaker. Because there exists a coupling capacitor at its input, the power amplifier behaves like a highpass filter. In this way, the amplifier is designed to prevent a possibly damaging DC voltage from being applied to the speaker. Such a voltage component could be present in $v_{\mathrm{LPF}}$ if, for example, $v_{\mathrm{OFF}}$ in the analog-to-digital converter is not properly adjusted to balance the output of the converter.
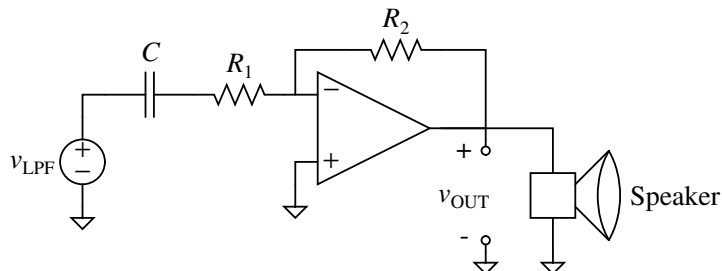


Figure 8: the power amplifier

(A) Assume that the power amplifier operates in sinusoidal steady state with $v_{\mathrm{LPF}} = \Re\{\tilde{v}_{\mathrm{LPF}}e^{j\omega t}\}$ and $v_{\mathrm{OUT}} = \Re\{\tilde{v}_{\mathrm{OUT}}e^{j\omega t}\}$ where $\tilde{v}_{\mathrm{LPF}}$ and $\tilde{v}_{\mathrm{OUT}}$ are complex amplitudes. Find the input-output transfer function $H_{\mathrm{AMP}}(\omega)$ of the power amplifier where $H_{\mathrm{AMP}}(\omega) \equiv \tilde{v}_{\mathrm{OUT}}/\tilde{v}_{\mathrm{LPF}}$.

**Answer:**    We can use the equation for an inverting op-amp to write down the answer directly.

$$H_{\mathrm{AMP}}(\omega) = \frac{\tilde{v}_{\mathrm{OUT}}}{\tilde{v}_{\mathrm{LPF}}} = \frac{-R_2}{R_1 + \frac{1}{j\omega C}} = \frac{-j\omega R_2 C}{1 + j\omega R_1 C}$$

Remember that this comes from assuming that $v_- = v_+ = 0$ and that the current into $v_- = 0$.

(B) Using the result of Part (A), find the magnitude and phase of $H_{\mathrm{AMP}}(\omega)$. **Answer:**

$$|H_{\mathrm{LPF}}(\omega)| = \frac{\omega R_2 C}{\sqrt{1 + \omega^2 R_1^2 C^2}}$$

$$\angle H_{\mathrm{LPF}}(\omega) = -\pi/2 - tan^{-1}(\omega R_1 C)$$

(C) Let $\omega_{\mathrm{AMP}}$ be the frequency at which the low-frequency and high-frequency asymptotes of $|H_{\mathrm{AMP}}(\omega)|$ intersect. Determine $\omega_{\mathrm{AMP}}$ in terms of $R_1$, $R_2$ and $C$.

**Answer:**    This problem can be approached just as in Problem 3.C:

For $\omega \ll R_1 C$ we drop the $\omega$ term because it is much less than 1. This result is simple:

$$H_{\mathrm{LPF}}(\omega \ll R_1 C) \approx \omega R_2 C$$

Which goes to zero as $\omega$ goes to zero. This matches out intuition that the capacitor becomes an open circuit at low frequencies.

For $\omega \gg R_1 C$ we drop the 1 because it is much less than $\omega$. The result is what we expect from noticing that the capacitor behaves like a short at high frequencies:

$$H_{\text{LPF}}(\omega \gg R_1 C) \approx \frac{R_2}{R_1}$$

Solving for the intercept fo these equations gives the expected $\omega = \frac{1}{R_1 C} = \omega_{\text{AMP}}$.

(D) Choose values for $R_1$, $R_2$ and $C$ so that $\omega_{\text{AMP}} \leq 2\pi \times 100$ Hz, and $|H_{\text{AMP}}(\omega)| = 1$ for $\omega \gg \omega_{\text{AMP}}$. Since these conditions alone under specify $R_1$, $R_2$ and $C$, there is no single correct choice. Therefore, choose values for $R_1$, $R_2$ and $C$ that are easily implemented with the components in the 6.002 lab kit.

**Answer:** $|H_{\text{AMP}}(\omega)| = 1$ requires that $R_1 = R_2 = R$. So now we only need to choose two values, $R$ and $C$. The key here is that $RC > 1/(2\pi \times 100) \approx 1.59 \times 10^{-3}$.

Using the same criteria as in the previous problem, one possible combination is:

$$R_1 = R_2 = 15\text{k}\Omega$$

$$C = 0.1\mu\text{F}$$

To check: $\omega = 1/(RC) = 666.7$ rad/s $= 2\pi \times 106$ Hz.

(E) If the original analog signal is recorded with a reduced amplitude, then the power amplifier must compensate by providing greater than unity gain. To provide this gain, $R_2$ is implemented with a fixed resistor in series with a potentiometer. Design such a modification that provides a variable gain of 1 to 5. Note that the 6.002 lab kit has a limited number of potentiometers.

**Answer:** When we choose values for the potentiometer and $R$, we still need to obey the restriction above that $RC > 1/(2\pi \times 100) \approx 1.59 \times 10^{-3}$.

Let's use a 100k$\Omega$ potentiometer, as it is the closest value we have to four times the 15k$\Omega$ above. The sum of the potentiometer and the series resistor $R_2$ must be five times the value of the input resistor $R_1$. This means that $R_1 = R_2 = 25$k$\Omega$. To satisfy the condition from Part (D), let $C = .072$ $\mu$F. We can implement this with a 0.022 $\mu$F capacitor in parallel with two 0.1 $\mu$F capacitors in series. When the potentiometer is at one extreme of its travel, its resistance is zero, and the circuit has a gain of one. At the other end, it has a resistance of 100k$\Omega$, and the gain of the circuit is five. Realize that we can still satisfy the condition of Part (D) with a single 0.1 $\mu$F capacitor and the 25k$\Omega$ resistor. It just means that $\omega_{\text{AMP}}$ will be significantly less than $2\pi \times 100$ Hz.

**Problem 11.5:     Connecting The Blocks**

In the complete audio playback system the output of the digital-to-analog converter is connected directly to the input of the low-pass filter, and the output of the low-pass filter is connected directly to the input of the power amplifier, as shown in Figure 1. Thus, the filter loads the converter, and the amplifier loads the filter. Explain why this loading could be ignored in Problems 2, 3 and 4. That is, explain why the converter, filter and amplifier may each be analyzed and designed in isolation.

**Answer:**     The key to this simplicity is the op-amp. Using the ideal model of the opamp (which turns out to be a relatively accurate model) we see that the output of each stage is independent of the amount of current supplied. That is to say, the op-amp in the digital-to-analog converter has the same output value no matter how much current the low-pass filter draws. Similarly, the op-amps in the low-pass filter and output stage maintain the same output voltage regardless of the current drawn.

Of course none of the op-amps are completely ideal. The speakers that you will use for the lab are piezo-electric devices that have high input-impedances, and so draw little current. The reason we have the final "power" stage is to remove any remaining DC-offset in the signal and to provide a volume control. If we were to use a traditional $8\Omega$ speaker, we would need to use a special high-power op-amp, or a power audio amplifier like the LM386, rather than the 741, which can only supply around 20mA at it's output. Within their designed region of operation, the op-amps will be highly insensitive to loading, and we can chain them together without worrying about how each block will affect the others.