Massachusetts Institute of Technology
Department of Electrical Engineering and Computer Science

6.002 – Circuits & Electronics
Spring 2004

Problem Set #3

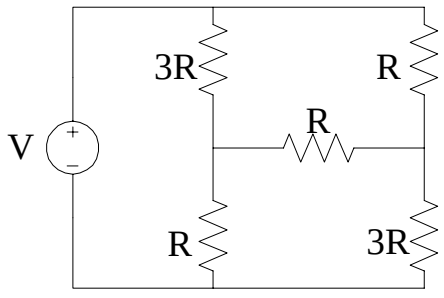
Issued 2/18/04 – Due 2/27/04

Exercise 3.1: A battery is measured to have an open-circuit voltage of 1.5 V. It can deliver 2.5 A to a 0.5-Ω resistor. How much current can it deliver to a short circuit? Hint: consider the Norton equivalent of the battery.

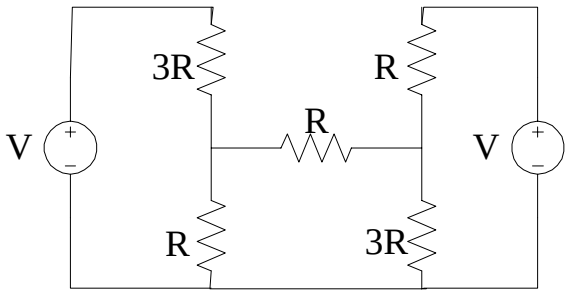
Exercise 3.2: This exercise applies two different analyses to determine the unknown node voltages in Network (A) shown below. It illustrates that the direct method of analysis is not always the simplest.

(A) Using nodal analysis, find the unknown node voltages in Network (A). Hint: see Problem 1.3.

(B) First, explain why Network (A) may be re-drawn as Network (B). Second, combine the left-hand source with the two left-most resistors to form their Thevenin equivalent, and redraw the resulting network. Third, combine the right-hand source with the two right-most resistors to form their Thevenin equivalent, and again redraw the resulting network. Finally, using superposition, determine the two unknown node voltages in the thrice re-drawn version of Network (A) thereby completing the analysis. Your answers to Parts (A) and (B) should be the same.

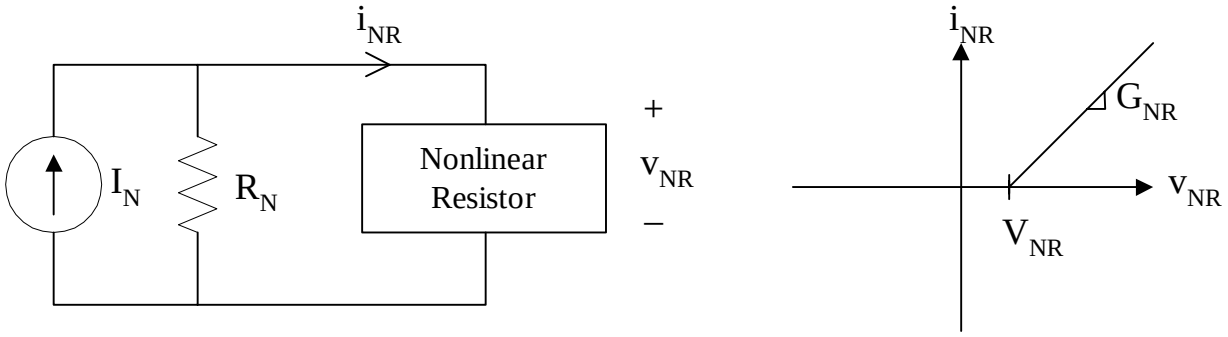


Network A



Network B

Exercise 3.3: A Norton equivalent network is used to excite a nonlinear resistor as shown below. The graphical i-v characteristic that defines the nonlinear resistor is also shown below. Determine the terminal current i_{NR} and the terminal voltage v_{NR} of the nonlinear resistor for all values of I_{N}. Hint: consider using a load-line analysis to gain insight.



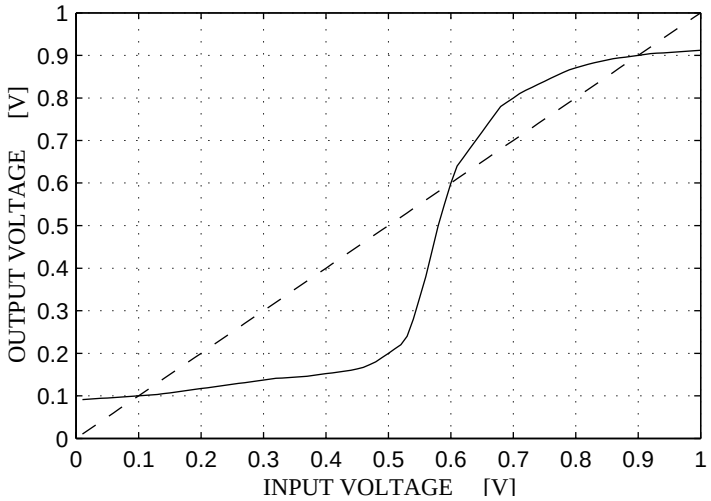
Problem 3.1: Consider the Boolean-logic buffer having the real input-output characteristic shown below. (The dashed diagonal is for referene.) The usual static discipline is to be defined for this buffer such that $V_{\mathrm{OL}} < V_{\mathrm{IL}} < V_{\mathrm{IH}} < V_{\mathrm{OH}}$. The high-level noise margin for this static discipline is $V_{\mathrm{OH}} - V_{\mathrm{IH}}$. The low-level noise margin for this static discipline is $V_{\mathrm{IL}} - V_{\mathrm{OL}}$.

(A) If zero noise margin were acceptable, over what voltage range could V_{IL} be chosen? What is the corresponding voltage range of V_{OL}?

(B) What combination of V_{IL} and V_{OL} maximizes the low-level noise margin?

(C) If zero noise margin were acceptable, over what voltage range could V_{IH} be chosen? What is the corresponding voltage range of V_{OH}?

(D) What combination of V_{IH} and V_{OH} maximizes the high-level noise margin?



Problem 3.2: This problem shows that there is often more than one way in which to implement a particular Boolean logic function, and that the most direct way is not always the simplest. Here, the two-input exclusive-or (XOR) gate serves as an example. The Boolean logic function that this gate implements is OUT = $(\text{IN1} \cdot \overline{\text{IN2}}) + (\overline{\text{IN1}} \cdot \text{IN2})$. Thus, its output is true if one or the other input is true, but not both.

(A) Using AND-gate, OR-gate and NOT-gate (inverter) Boolean logic symbols, implement a two-input XOR gate by directly implementing the Boolean logic function that defined it above.

(B) Design an NMOS inverter, an NMOS two-input AND gate and an NMOS two-input OR gate using a minimum of MOSFETs and pull-up resistors.

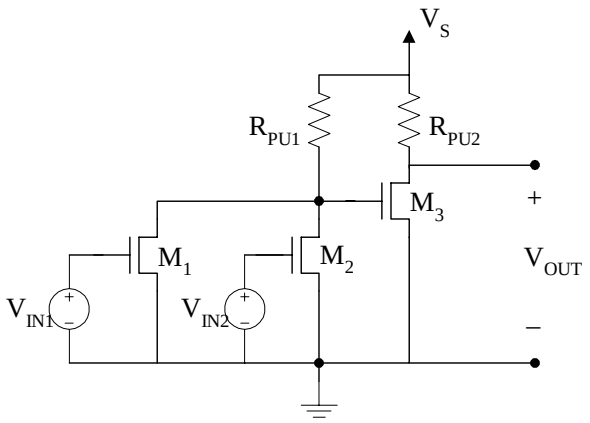
(C) Combine your results from Parts (A) and (B) to implement an NMOS two-input XOR gate. Your implementation should require eleven MOSFETs and eight pull-up resistors.

(D) Using truth tables, prove DeMorgan's law. DeMorgan's Law states that $\overline{\text{A} + \text{B}} = \overline{\text{A}} \cdot \overline{\text{B}}$, or equivalently that $\text{A} + \text{B} = \overline{\overline{\text{A}} \cdot \overline{\text{B}}}$, or equivalently that $\overline{\text{A} \cdot \text{B}} = \overline{\text{A}} + \overline{\text{B}}$, or equivalently, that $\text{A} \cdot \text{B} = \overline{\overline{\text{A}} + \overline{\text{B}}}$. (Note that the second version of DeMorgan's Law can be derived by inverting the first version, and that the third and fourth versions can be derived from the second and first versions, respectively, by substituting $\overline{\text{A}}$ for A and $\overline{\text{B}}$ for B.

(E) Using only inverters and two-input NOR gates, implement an alternative NMOS two-input XOR gate. This can be done with as few as nine MOSFETs and six pull-up resistors. Hint: use DeMorgan's Law to modify your result found in Part (A).

Problem 3.3: Consider the NMOS two-input OR gate shown below. This gate is to be implemented with MOSFETs having 1 V $\leq V_{\text{T}} \leq$ 4 V and $10^3\ \Omega \leq R_{\text{ON}} \leq 10^6\ \Omega$, and pull-up resistors having $10^3\ \Omega \leq R_{\text{PU}} \leq 10^6\ \Omega$. (The inequalities express a permissible design space as opposed to a range of manufacturing uncertainty.) The MOSFETs and pull-up resistors need not have identical parameters.

Complete the design of the OR gate by choosing values for each V_{T}, R_{ON} and R_{PU} so that: $V_{\text{OL}} = 1$ V; $V_{\text{IL}} = 2$ V; $V_{\text{IH}} = 3$ V; $V_{\text{OH}} = 4$ V; and the power dissipated by the gate is minimized. If any parameter does not have a unique design value, then give the permissible range for that parameter. Assume $V_{\text{S}} = 5$V.



Problem 3.4: The switch-resistor (SR) model of a MOSFET is a highly simplified model that is nonetheless very useful for describing the behavior of a MOSFET in a digital logic circuit. However, this model is so simplified that it can lead to inconsistent analyses in some cases, as illustrated by this problem.

Consider the analysis of the two-input NAND and two-input NOR gates shown below. Assume that all MOSFETS in these gates behave according to the SR model with a threshold voltage $V_T = 1$ V, and on-state resistance R_{ON}. Further, let $R_{PU} = R_{ON}$, and $V_S = 3$ V.

(A) Consider the two-input NAND gate. Let $V_{IN1} = V_{IN2} = 1.5$ V. Assume that M2 is on and determine v_{OUT} and v_{GS} for M2. (Is M1 on or off?) Is the value of v_{GS} consistent with the assumption that M2 is on?

(B) Again consider the two-input NAND gate, and again let $V_{IN1} = V_{IN2} = 1.5$ V. Now assume that M2 is off and determine v_{OUT} and v_{GS} for M2. Is the value of v_{GS} consistent with the assumption that M2 is off?

(C) From your answers to Parts (A) and (B) you should conclude that M2 can be neither on nor off. What characteristics of the SR model and the design of the two-input NAND gate allow this inconsistency to occur? How do you think the real circuit actually behaves?

(D) How high must V_{IH} be defined for the two-input NAND gate so that the inconsistent analysis found above is inconsequential to the proper operation of the gate?

(E) Consider now the two-input NOR gate. Can its analysis produce the same inconsistency for any combination of parameter values? Why or why not?