6.002 Spring 2004
Problem Set #3
Solutions

Ex 3.1

This problem can be done with either Norton or Thevenin equivalent circuits. Once we have these parameters we can solve for the behavior of the battery in any circuit, including the short-circuit condition.

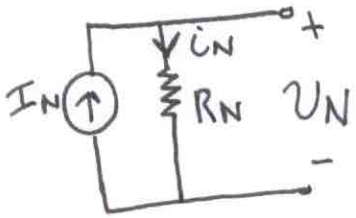
Norton:

Given:

$v_{oc} = 1.5\ V$

$2.5\ A$ to a $0.5\ \Omega$ Resistor

① Draw Norton equivalent:



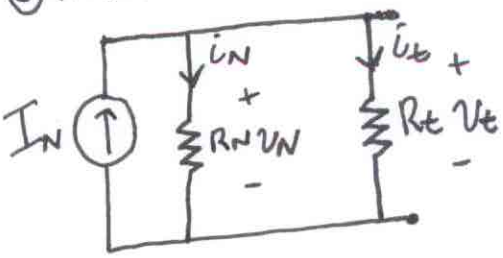
$v_N = v_{oc} = 1.5\ V$ (given)

$i_N = I_N$ (KCL)

② write device law and substitute

$v_N = i_N \cdot R_N = I_N \cdot R_N = 1.5\ V$

③ insert test resistor ($R_t = 0.5\ \Omega$)



$i_t = 2.5\ A$ (given)

$v_t = v_N$

$v_t = i_t R_t = 2.5A \cdot 0.5\Omega = 1.25\ V$

$v_N = 1.25\ V$

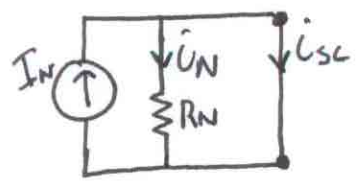
$i_N = I_N - i_t = I_N - 2.5A$

$v_N = i_N R_N = (I_N - 2.5A) \cdot R_N$

$I_N R_N = 1.5V \Rightarrow 1.25\ V = (I_N R_N - (2.5A) R_N)$

$R_N = 0.1\ \Omega$

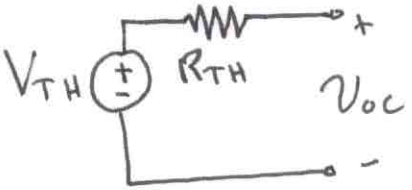
$I_N = 15\ A$



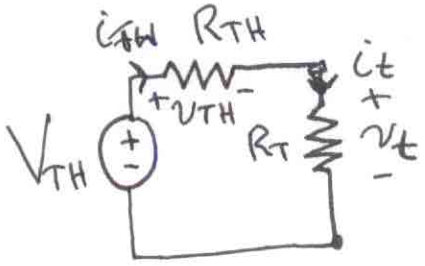
$\boxed{i_{sc} = I_N = 15A}$

Ex 3.1 (continued)

Thevenin (Brief solution for those interested)



$V_{TH} = v_{oc} = 1.5\,V$



$R_t = 0.5\,\Omega$ (given)

$i_t = 2.5\,A$

$v_t = R_t i_t = 1.25\,V$

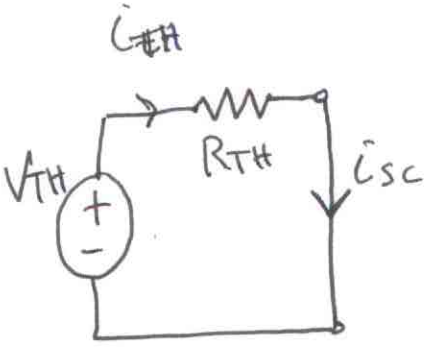
$i_{TH} = i_t$

$V_{TH} - v_t = v_{TH} = 0.25\,V$

$v_{TH} = i_{TH} R_{TH}$

$0.25\,V = 2.5\,A \cdot R_{TH}$

$0.1\,\Omega = R_{TH}$



$i_{sc} = i_{TH}$

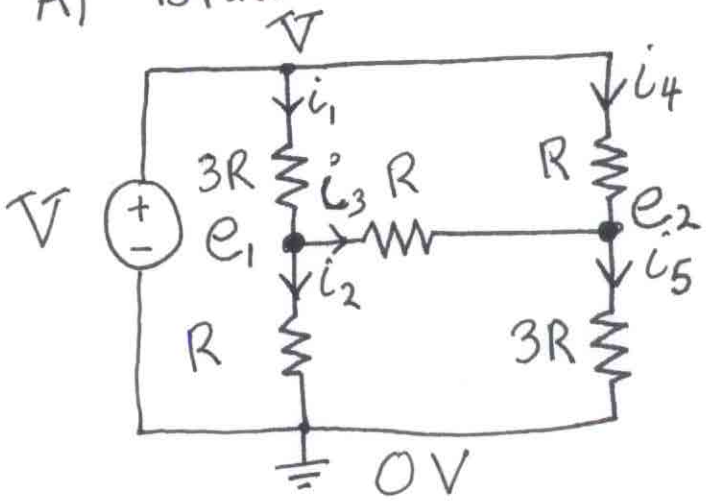
$i_{sc} = \dfrac{V_{TH}}{R_{TH}} = \dfrac{1.5\,V}{0.1\,\Omega} = 15\,A$

$\boxed{i_{sc} = 15\,A^{\star}}$

*matches result from Norton equivalent.

Ex. 3.2

A) Draw network and label nodes e_1, e_2



Write node equations.

e_1: $\left(\frac{e_1 - V}{3R}\right) + \left(\frac{e_1 - e_2}{R}\right) + \frac{e_1}{R} = 0$

$$(e_1 - V) + 3(e_1 - e_2) + 3e_1 = 0$$

e_2: $\frac{(e_2 - e_1)}{R} + \frac{(e_2 - V)}{R} + \frac{e_2}{3R} = 0$

$$3(e_2 - e_1) + 3(e_2 - V) + e_2 = 0$$

Solve 2 simultaneous equations:

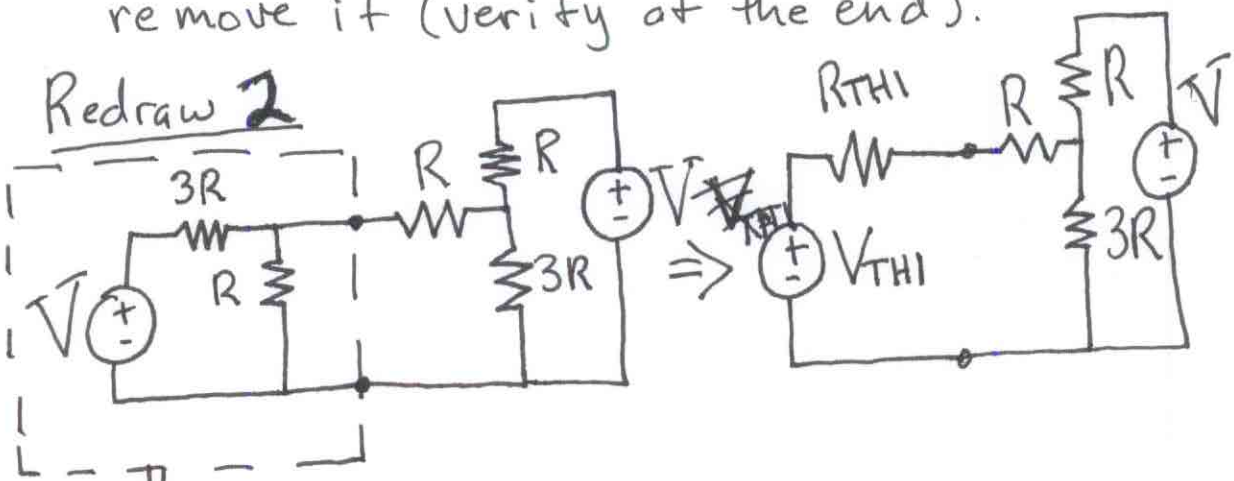
$$7e_1 - 3e_2 = V$$
$$-3e_1 + 7e_2 = 3V$$
$$\Rightarrow \begin{pmatrix} 7 & -3 \\ -3 & 7 \end{pmatrix} \begin{pmatrix} e_1 \\ e_2 \end{pmatrix} = \begin{pmatrix} V \\ 3V \end{pmatrix}$$

$$\boxed{e_1 = 0.4\,V}$$
$$\boxed{e_2 = 0.6\,V}$$

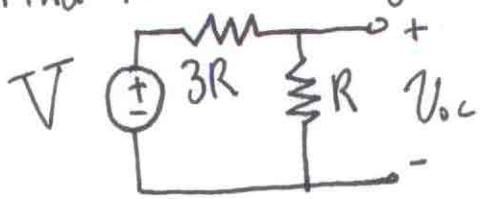
Ex 3.2

B) The role of the voltage source is to set the voltage at the "top" node to $\bar{V}$ (a constant). Therefore, as long as we set both nodes to $\bar{V}$ with a voltage source on each, we can split this top node into 2 nodes. Since no current will flow through the wire connecting these nodes, we can remove it (verify at the end).

Redraw 2



Find Thevenin equivalent

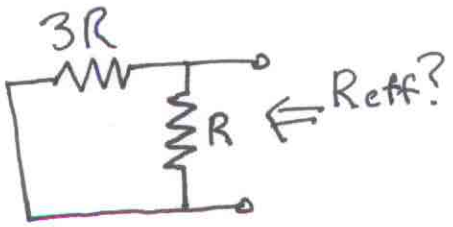


$V_{TH} = V_{oc}$

Voltage divider

$$V_{oc} = \left(\frac{R}{R+3R}\right)\cdot \bar{V}$$

$$\boxed{V_{TH} = \frac{1}{4}\bar{V}}$$



$R_{TH} = R_{eff}$

$$R_{TH} = (3R)\,//\,R = \frac{3R\cdot R}{3R+R}$$

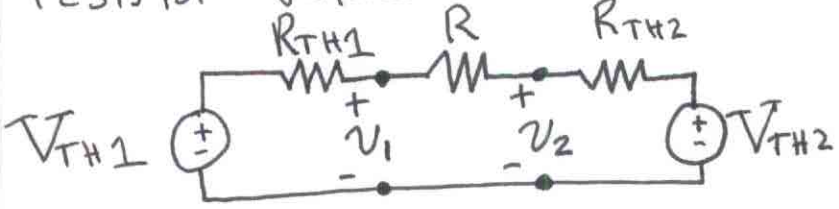
$$\boxed{R_{TH} = \frac{3}{4}R}$$

Ex 3.2

B)

Redraw **3**

Similar to other side, just switch resistor values.

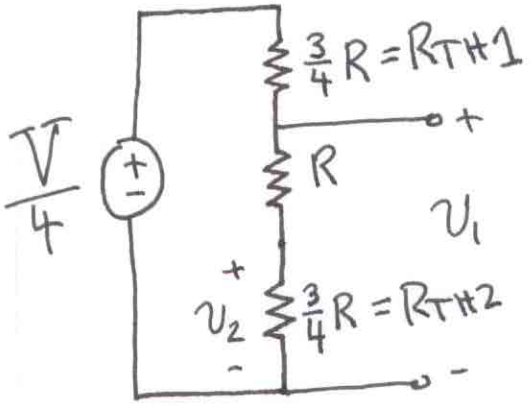


$$R_{TH2} = R \,//\, (3R) = \frac{3}{4}R$$

$$V_{TH2} = \frac{3R}{R+3R} = \frac{3}{4}V$$

Use superposition to solve for v_1, v_2

V_{TH1} = ON, V_{TH2} = OFF

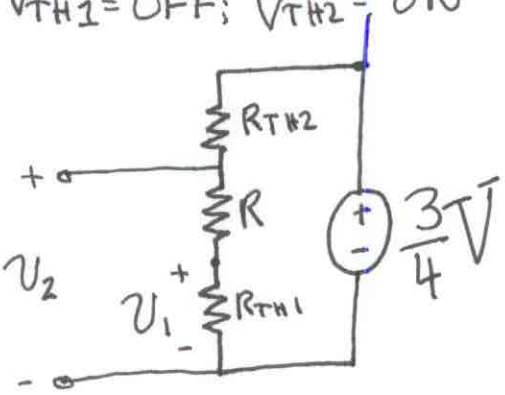


Voltage Divider:

$$v_1 = \frac{V}{4} \cdot \frac{(R + R_{TH2})}{(R_{TH1} + R + R_{TH2})}$$

$$v_2 = \frac{V}{4}\left(\frac{R_{TH2}}{R_{TH1} + R + R_{TH2}}\right)$$

V_{TH1} = OFF; V_{TH2} = ON



Voltage Divider:

$$v_1 = \frac{3}{4}V\left(\frac{R_{TH1}}{R_{TH1} + R + R_{TH2}}\right)$$

$$v_2 = \frac{3}{4}V\frac{(R + R_{TH1})}{(R_{TH2} + R + R_{TH1})}$$

$v_1 = 0.225V$

$v_2 = 0.525V$

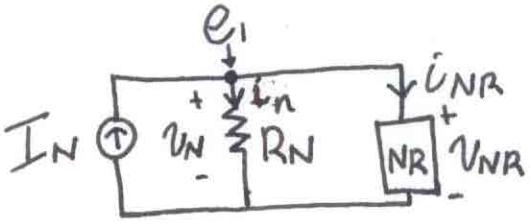
$v_1 = 0.175\ V$; $v_2 = 0.075V$

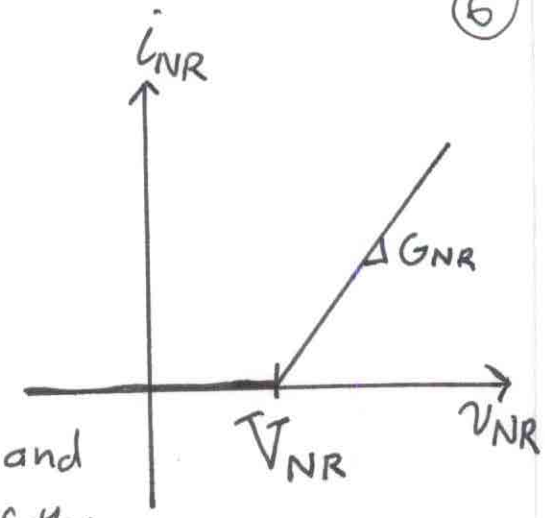
Total $v_1 = (0.175 + 0.225)V = 0.4V$

Total $v_2 = (0.075 + 0.525)V = 0.6V$

✓ same as Part A)

Ex. 3.3





Plot curve for i_{NR}-v_{NR} and "load-line" for the rest of the circuit to find operating point.

by KCL @ node e_1:

$$I_N = i_N + i_{NR} \Rightarrow i_{NR} = -i_N + I_N$$

by KVL:

$$v_N = v_{NR}$$

Define: $G_N \equiv \frac{1}{R_N}$

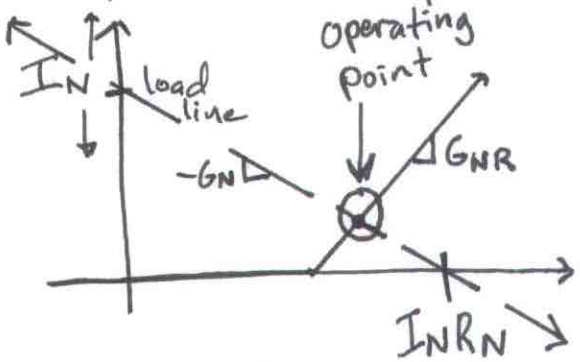
$$v_{NR} = i_N R_N \quad \text{(Device Law)}$$

$$v_{NR} \cdot G_N = i_N$$

$$\therefore\ i_{NR} = -G_N v_{NR} + I_N \quad \text{(load line)}$$

Note: this is a general equation for all values of I_N.

Example load-line plot for some $I_N > 0$

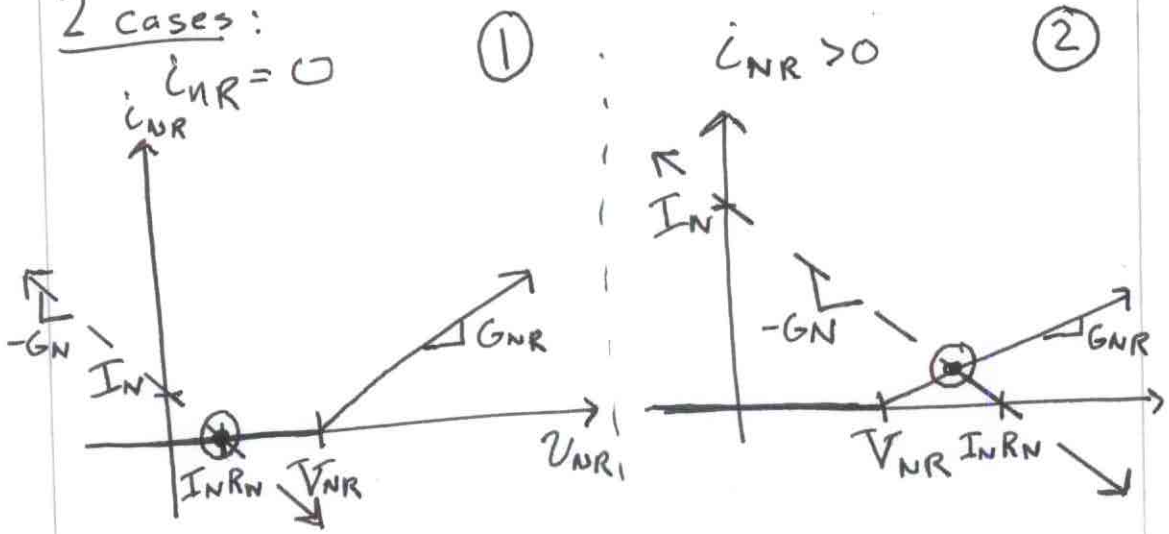


Adjusting I_N up or down will shift load line up or down, but will not change slope.

Ex 3.3

Now that we have the general load-line plot, we must solve for all cases of I_N.

2 cases:



Find I_N where two cases intersect.

x-intercept = V_{NR} (load line)

$I_N R_N = V_{NR}$ so $I_N = \frac{V_{NR}}{R_N}$

Case 1: $I_N \leq \frac{V_{NR}}{R_N}$

$i_{NR} = 0$, $v_{NR} = I_N R_N$

Case 2:

for $i_{NR} > 0$, the characteristic curve for the device looks like a line with slope = G_{NR} and x-intercept = V_{NR}.

$$i_{NR} = G_{NR} v_{NR} - G_{NR} V_{NR}$$

Set this equal to load line:

$$-G_N v_{NR} + I_N = G_{NR} v_{NR} - G_{NR} V_{NR}$$

$$\therefore v_{NR} = \frac{I_N + G_{NR} V_{NR}}{G_{NR} + G_N} \qquad i_{NR} = \frac{G_{NR}(I_N - G_N V_{NR})}{G_{NR} + G_N}$$

Ex 3.3

$$(V_{NR}, i_{NR}) = \begin{cases} (I_N R_N, 0) & I_N \le \frac{V_{NR}}{R_N} \\ \left(\frac{I_N + G_{NR} V_{NR}}{G_{NR} + G_N}, \frac{G_{NR}(I_N - G_N V_{NR})}{G_{NR} + G_N} \right) & I_N > \frac{V_{NR}}{R_N} \end{cases}$$

P. 3.1

- Valid V_{IL} is value such that all inputs $\leq V_{IL}$ result in outputs $\leq V_{OL}$
- Valid V_{IH} is value such that all inputs $\geq V_{IH}$ result in outputs $\geq V_{OH}$

A) Find where curve crosses $V_{out} = V_{IN}$ line. $\Rightarrow V_{IN} = V_{OUT} = 0.6\ V$

$\Rightarrow V_{IN} = V_{out} = 0.1\ V$

These are the upper and lower limits of V_{IL}. The curve must be below the $V_{IN} = V_{out}$ line.

$$\text{Range}: \begin{cases} 0.1\ V < V_{IL} < 0.6\ V \\ 0.1\ V < V_{OL} < V_{IL} \end{cases}$$

B) From 0.6V (max V_{IL}) follow curve to left until slope = 1. Up until this point, V_{out} is decreasing faster than V_{IN}, so noise margin is growing. After this point, the noise margin begins to decrease again. At this point, the value of $V_{IN} \Rightarrow V_{IL}$ and the value of $V_{out} \Rightarrow V_{OL}$

$V_{IL} = 0.5\ V$
$V_{OL} = 0.2\ V$

Noise margin = 0.3 V

P3.1 (10)

C) same as A)

find points where $V_{IN} = V_{out}$. The space between where $V_{out} > V_{IN}$ is the acceptable range.

$$0.6\,V < V_{IH} < 0.9V$$
$$V_{IH} < V_{OH} < 0.9\,V$$

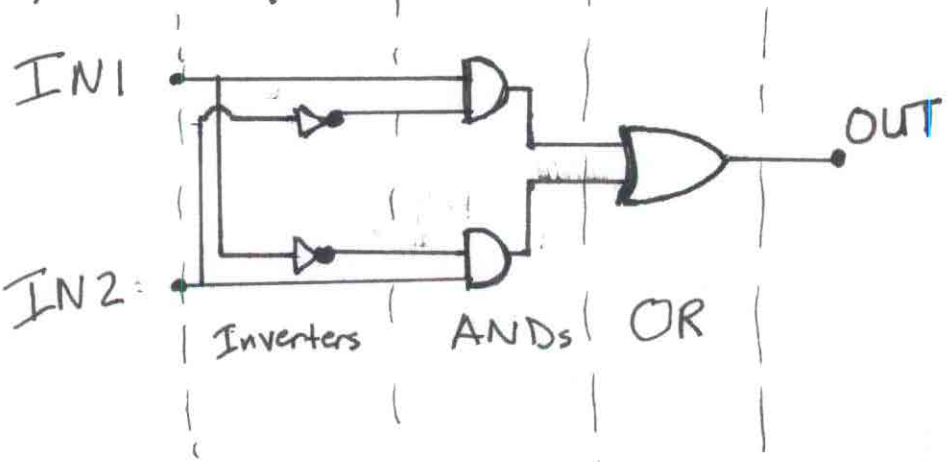
D) Choose point where slope = 1

$$V_{IH} = 0.7V$$
$$V_{OH} = 0.8V$$

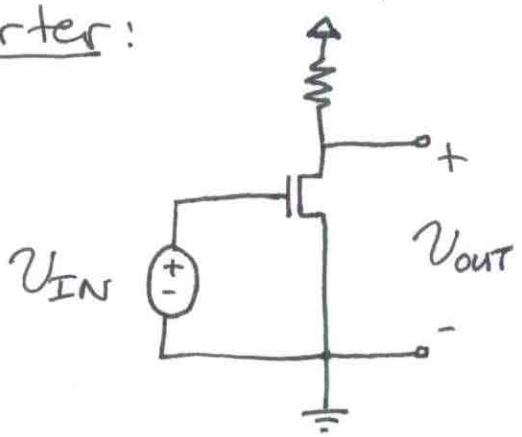
Noise Margin = 0.1 V

P.3.2

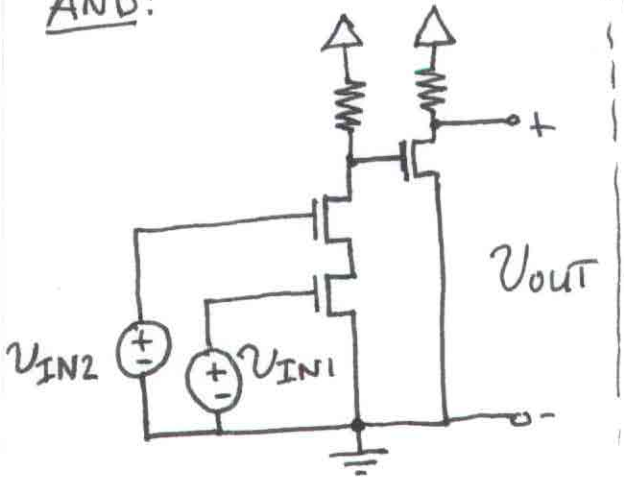
A) $OUT = (IN1 \cdot \overline{IN2}) + (\overline{IN1} \cdot IN2)$



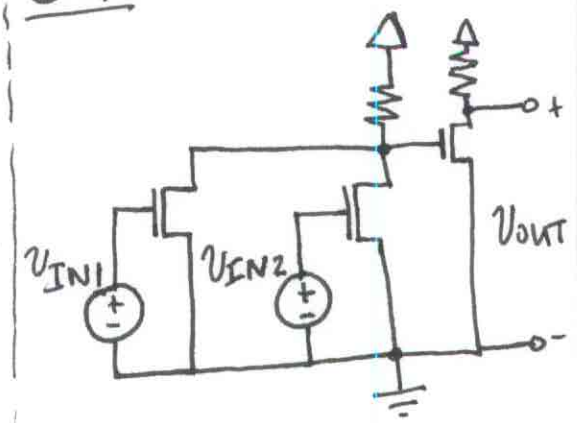
B) Inverter:



AND:

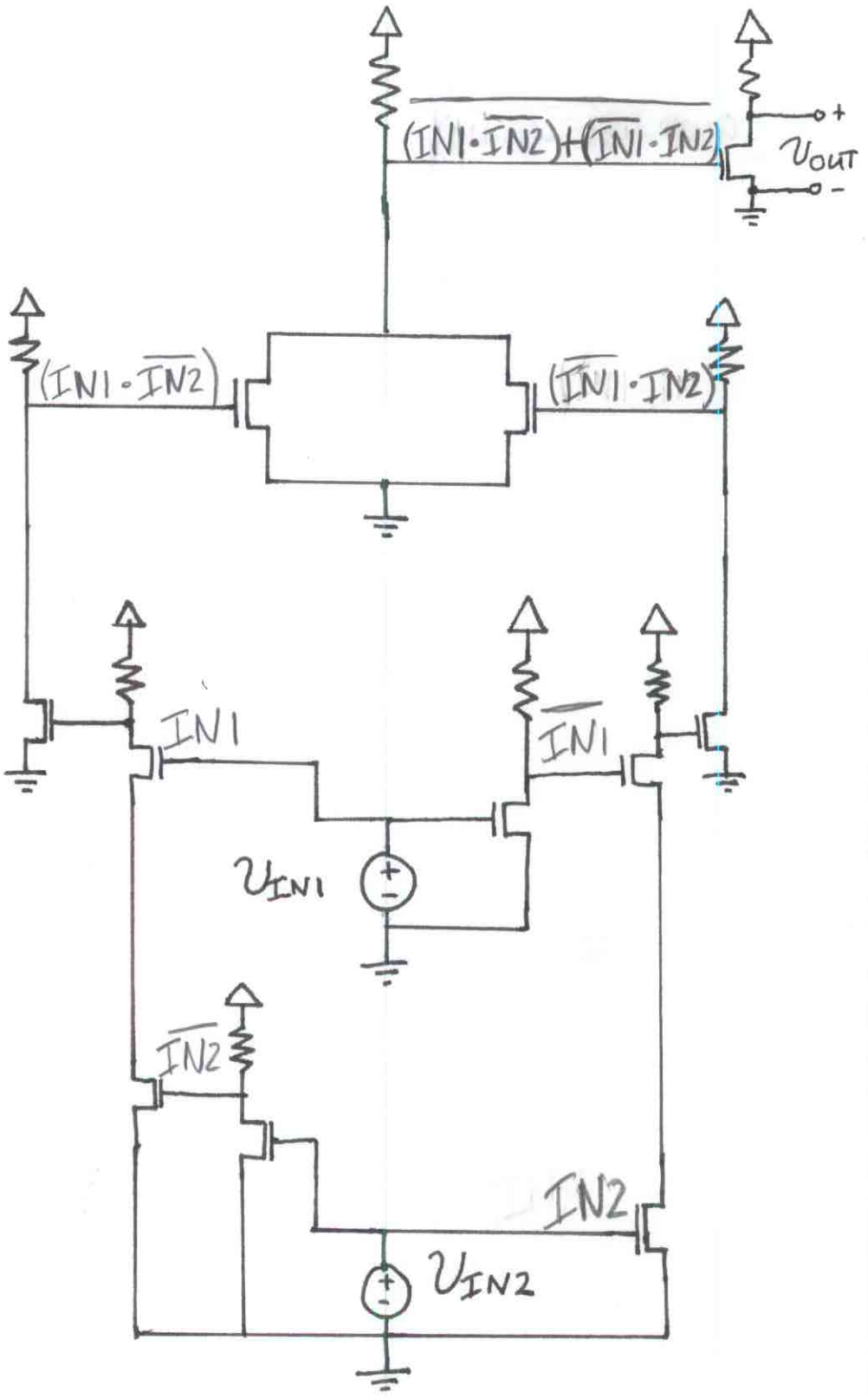


OR:



P3.2

c) XOR:


(IN1·$\overline{IN2}$)+($\overline{IN1}$·IN2)
V_{OUT}
+
-
(IN1·$\overline{IN2}$)
($\overline{IN1}$·IN2)
IN1
$\overline{IN1}$
V_{IN1}
$\overline{IN2}$
IN2
V_{IN2}

P 3.2

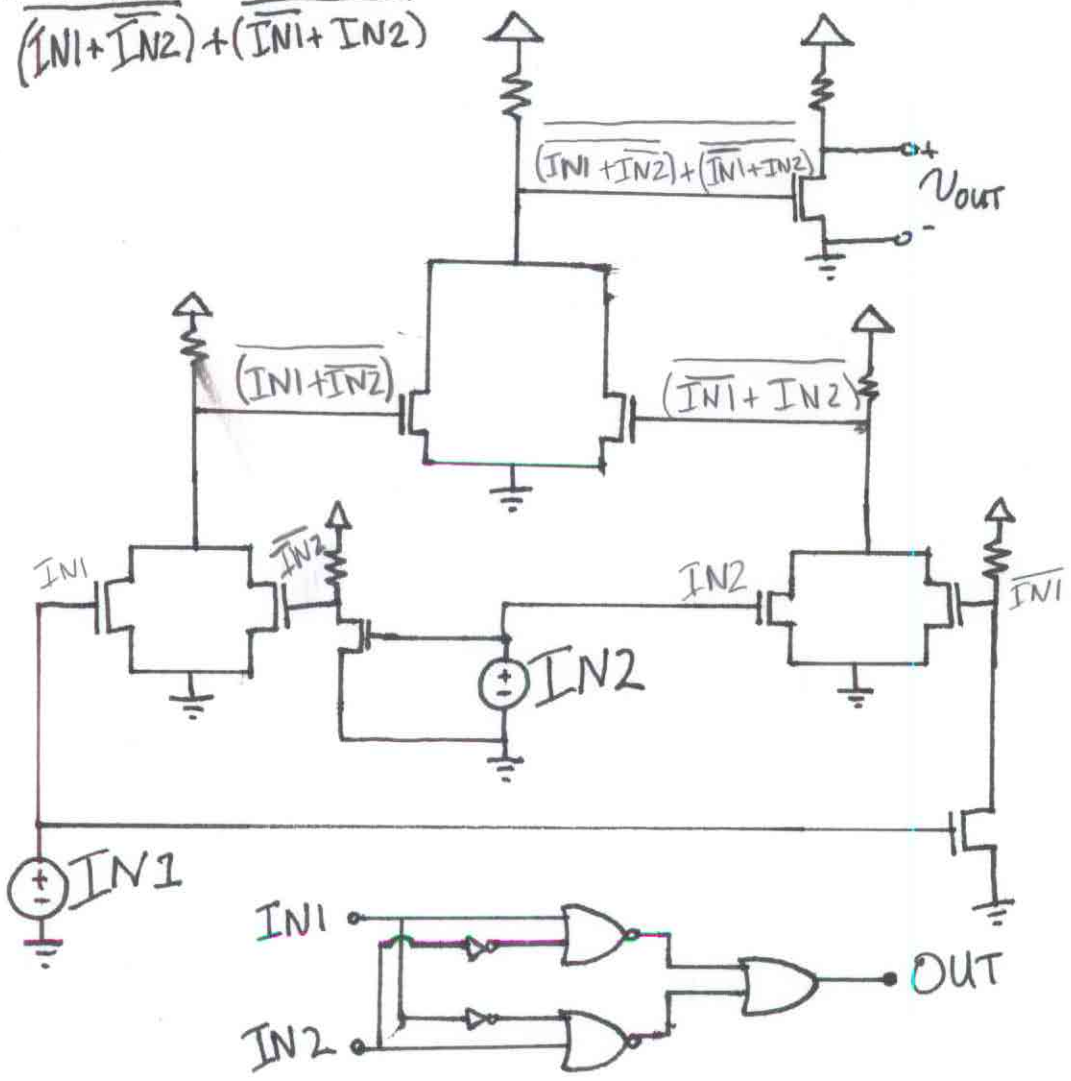
D)

A	B	$\bar{A}$	$\bar{B}$	A+B	$\bar{A}\cdot\bar{B}$	$\overline{\bar{A}\cdot\bar{B}}$
0	0	1	1	0	1	0
0	1	1	0	1	0	1
1	0	0	1	1	0	1
1	1	0	0	1	0	1

The same

For all combinations of A, B $\Rightarrow$ $A+B = \overline{\bar{A}\cdot\bar{B}}$

E) XOR = $\overline{(IN1+\overline{IN2})}+\overline{(\overline{IN1}+IN2)}$



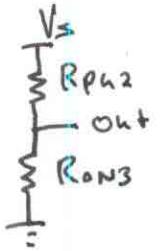
P 3.3

R_{pu1}, R_{pu2}:

Power is dissipated when MOSFETs are ON. $P_{diss} = \frac{V^2}{R}$ in resistors. For the output and input stages, $V = V_s$ and $R = R_{pu} + R_{ON}$.

To minimize power, maximize R.

$\therefore R_{pu1} = R_{pu2} = 10^6 \Omega$



R_{ON3}: $V_{OL} = 1\ V$

When MOSFET is on, output voltage is a voltage divider between R_{pu2} and R_{ON3}

$$V_{OL} = V_s \cdot \frac{R_{ON3}}{R_{ON3} + R_{pu2}}$$

$$1V = 5V \cdot \frac{R_{ON3}}{R_{ON3} + 10^6 \Omega}$$

$$\therefore R_{ON3} = 2.5 \times 10^5 \Omega$$

R_{ON1}, R_{ON2}:

To minimize power dissipation, maximize R_{on1}, R_{on2}. Since it is internal to the gate, it does not have to follow the static discipline.

$R_{ON1} = R_{ON2} = 10^6 \Omega$

V_{T3}:

highest input voltage to M3 is when one of M1, M2 is on. $V_{in3} = V_s \cdot \frac{R_{ON1}}{R_{ON1} + R_{pu1}} = 5V \cdot \frac{10^6 \Omega}{10^6 \Omega + 10^6 \Omega}$

$$V_{in3} = 2.5V$$

$$2.5V < V_{T3} < 5V$$

P 3.3

V_{T1}, V_{T2}:

Must be between V_{IL} and V_{IH}

$2K < V_{T1} < 3V$

$2V < V_{T2} < 3V$

$R_{PU1} = 10^6 \Omega$

$R_{PU2} = 10^6 \Omega$

$R_{ON1} = 10^6 \Omega$

$R_{ON2} = 10^6 \Omega$

$R_{ON3} = 2.5 \times 10^5 \Omega$

$2V < V_{T1} < 3V$

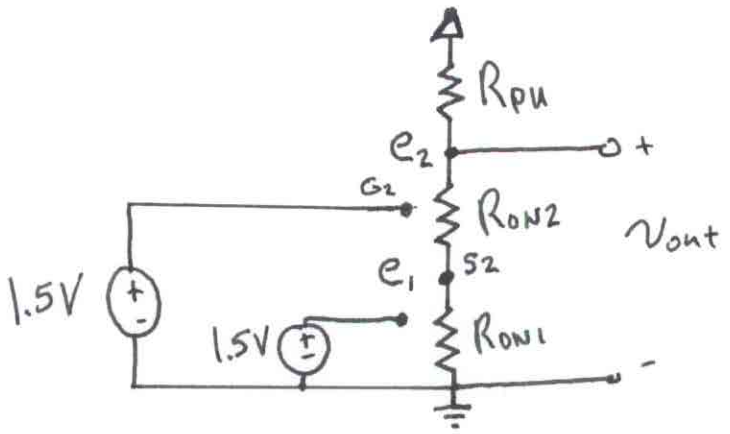
$2V < V_{T2} < 3V$

$2.5V < V_{T3} < 5V$

P3.4

A) $V_{IN1} = V_{IN2} = 1.5V$ $\quad V_T = 1V$

Assume: M1 ON, M2 ON



$R_{PU} = R_{ON2} = R_{ON1}$

Voltage divider

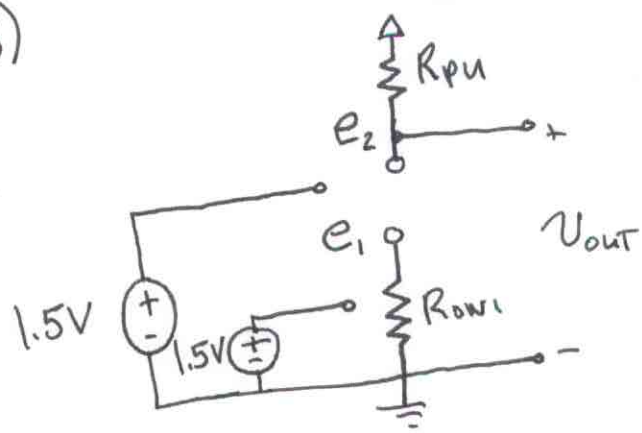
$e_2 = 2V$

$e_1 = 1V$

$V_{gs2} = 1.5V - e_1 = 1.5V - 1V = \boxed{0.5V}$

$V_{gs2} < V_T$ $\boxed{\text{Inconsistent}}$

B)



Open circuit. $e_1 = 0V$, $e_2 = 5V$

$v_{gs2} = 1.5V - e_1 = \boxed{1.5V}$

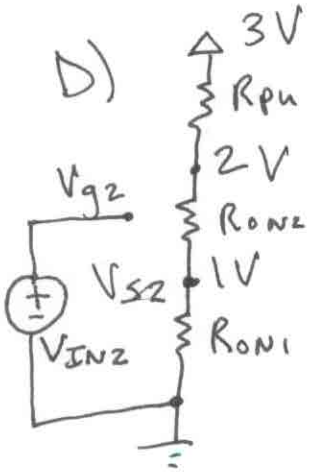
$v_{gs2} > V_T$ $\boxed{\text{inconsistent}}$

P3.4

C) The SR model is only reliable when $V_{DS} \ll V_{GS} - V_T$.

For V_{GS} very close to V_T, the on-state resistance (R_{ON}) of the MOSFET is much lower. The SR model, with two extreme states, is not an accurate physical model of the device for all inputs. This inconsistency is apparent in the NAND gate because the control voltage of M2, V_{gs2}, depends on the state of the MOSFET. The source of M2 is floating, so here the inconsistency affects circuit behavior.

D)



V_{IN2} must be set so that $V_{gs2} > V_T$. $V_{S2} = 1V$

$V_{gs2} = V_{g2} - V_{S2} > V_T$

$V_{IN2} - 1V > 1V$

$V_{IN2} > 2V$

$$\boxed{V_{IH} = 2V}$$

E) No, the SR model will not cause an inconsistency in the NOR gate. All MOSFET source terminals are tied to ground, so all control signals are referenced to ground.