Massachusetts Institute of Technology
Department of Electrical Engineering and Computer Science

# 6.002 – Electronic Circuits
Spring 2000

## Conflict Final Exam

Solutions

- Please put your name in the space provided below, and circle the name of your recitation instructor and the time of your recitation.
- Do all of your work on the pages contained within this exam. In particular, do your work for each question within the boundaries of the question, or on the back side of the page preceding the question. When finished, put your answer to each question in the corresponding answer box at the bottom of the page on which the question in written.
- You may use one double-sided page of notes while taking this exam.
- Final grades in 6.002 will not be given out by phone or by e-mail. Rather, they should be available through WEBSIS by May 22. You may review and take back your final exam on or after May 22.
- Good luck!

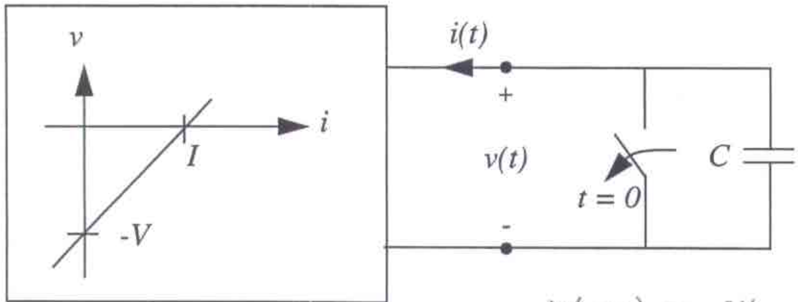
Name: ______________________________

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **Instructor:** | Freidberg | | Chandrakasan | | Cooke | | Weiss | |
| **Time:** | 9 | 10 | 10 | 11 | 11 | 12 | 1 | 2 |

## Problem 1 – 20%

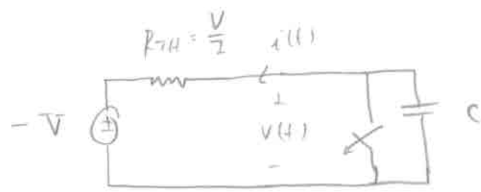
This problem involves determining the transient responses of the three circuits shown below. For each circuit, determine the response analytically, and then graph the response on the axis provided. Clearly label each graph.

(1A) The terminal characteristics of part of this circuit are described graphically. At $t = 0$, the switch *opens*. Determine $v(t)$ for $t \geq 0$.



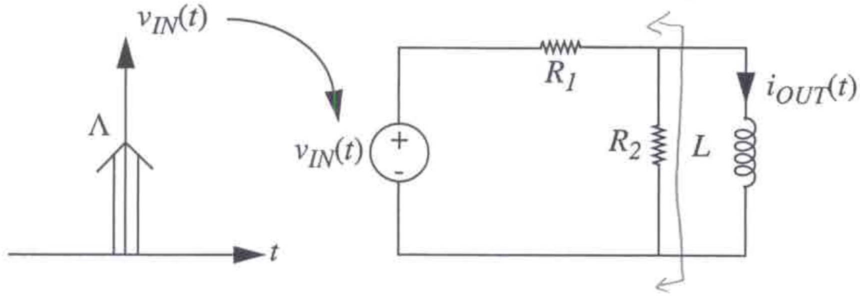

$v(0^-) = 0V.$

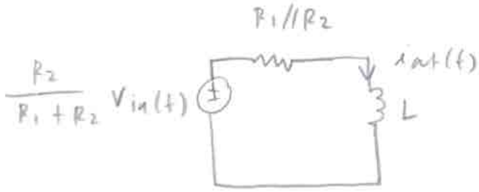
$v(t) = -V(1 - e^{-t/R_{TH}C})$




$v(t) =$ $-V\left(1 - e^{\frac{-t}{\frac{VC}{I}}}\right) u(t)$

(1B) This circuit is initially at rest. At $t = 0$, the voltage source provides an impulse of area $\Lambda$. Determine $i_{\mathrm{OUT}}(t)$ for $t \geq 0^+$.

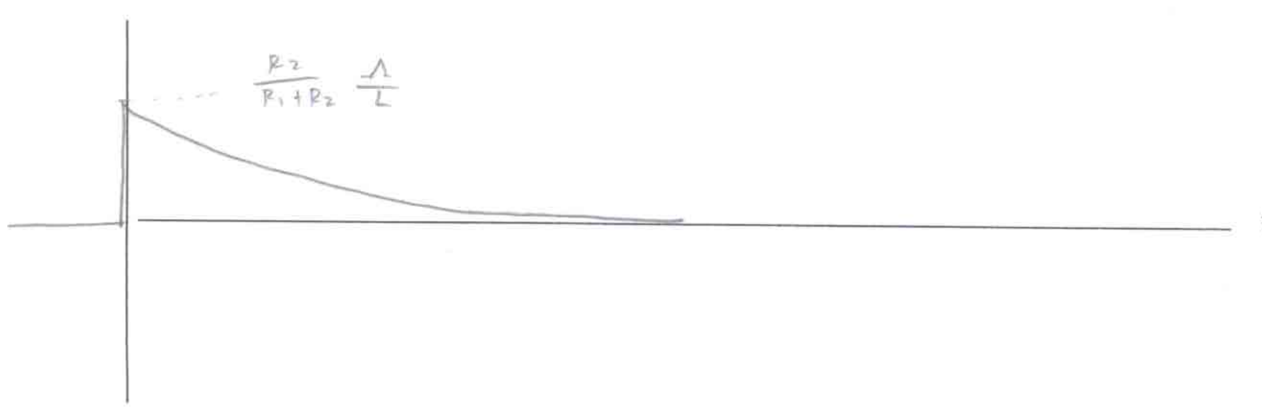


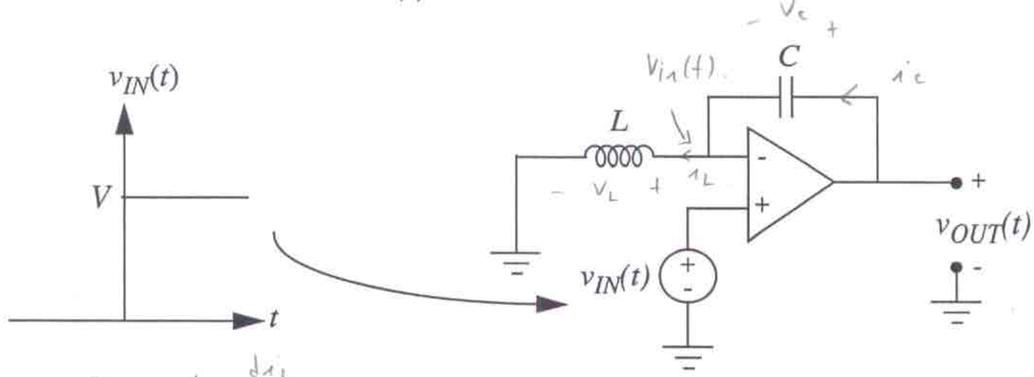

$$i_{at}(0^+) = \frac{R_2}{R_1+R_2} \frac{\Lambda}{L}$$

$i_{at}(t)$ will decay down to 0 with $\tau = \frac{L}{R_{eq}} = \frac{L}{R_1 // R_2}$ after $t > 0$.

$$i_{\mathrm{OUT}}(t) = \frac{R_2}{R_1+R_2} \frac{\Lambda}{L} e^{-\frac{t}{L/(R_1//R_2)}} u(t)$$



(1C) This circuit is initially at rest. At $t = 0$, the voltage source takes a step. Assume that the op-amp is ideal. Determine $v_{\mathrm{OUT}}(t)$ for $t \geq 0$.



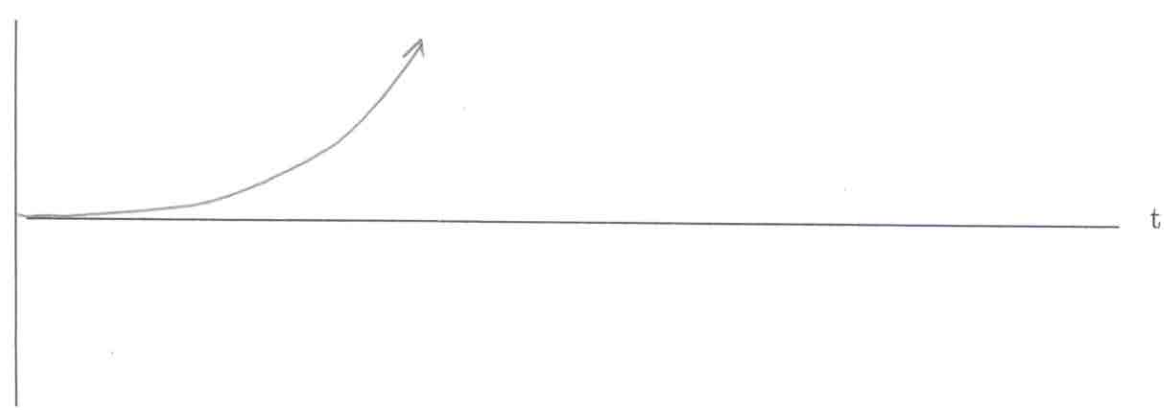

$$V_L = L \frac{di_L}{dt} \Rightarrow i_L = \frac{V}{L} t$$

Know $i_c = i_L$ because $i^- = i^+ = 0\,A$ for ideal op-amp.

$$\Rightarrow \frac{V}{L} t = C \frac{dV_c}{dt} = C \frac{d}{dt} ( V_{at} - V ) = C \frac{dV_{at}}{dt}$$

$$\Rightarrow V_{at} = \frac{V}{LC} \int t \, dt = \frac{Vt^2}{2LC}$$

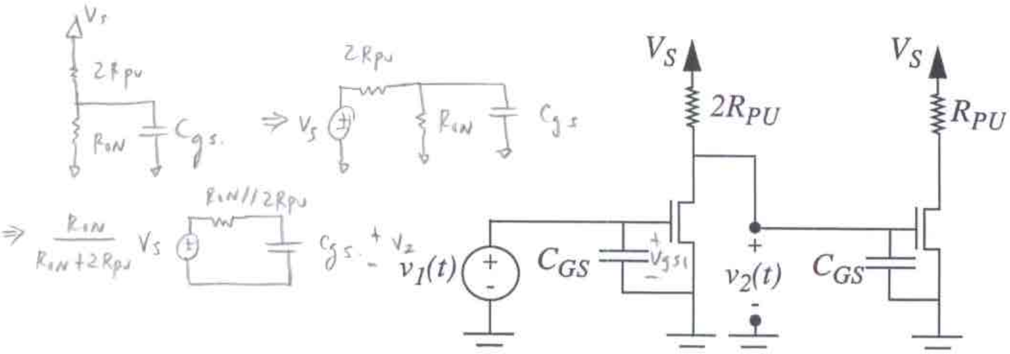
$v_{\mathrm{OUT}}(t) = \dfrac{Vt^2}{2LC}$



## Problem 2 – 20 %

This problem focuses on NMOS digital logic circuits built with MOSFETs and pull-up resistors. Model each MOSFET with a switch-resistor model having a threshold voltage $V_T$ and on-state resistance $R_{ON}$. Also include the gate-to-source capacitance $C_{GS}$ in the model. Finally, let $V_T \equiv V_S/2$ and assume that $R_{ON} \ll R_{PU}$.

(2A) Consider the cascaded inverters shown below. Determine the fall time $T_F$ and the rise time $T_R$ of the first inverter in terms of the MOSFET model and circuit parameters. The fall time is defined here as the delay from the time that $v_1(t)$ rises past $V_T$ to the time $v_2(t)$ falls past $V_T$; the rise time is the delay from the time that $v_1(t)$ falls past $V_T$ to the time $v_2(t)$ rises past $V_T$. Assume that the circuit is at rest before $v_1(t)$ passes $V_T$ in both cases, and make reasonable approximations based on the inequality $R_{ON} \ll R_{PU}$.




$R_{ON} << R_{pu} \Rightarrow$

$R_{ON} // R_{pu} \approx R_{ON}$

$V_T = \frac{V_S}{2}$

(1) when $v_1(t)$ hits $V_T$, M1 turns on, $v_2(0) = V_s$

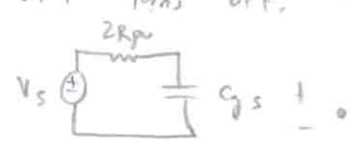
$\Rightarrow$ approximate circuit as

$\Rightarrow V_2(t_f) = V_s e^{-\frac{t_f}{R_{ON} C_{gs}}} = \frac{V_s}{2}$

$\Rightarrow -R_{ON} C_{gs} \ln \frac{1}{2} \approx t_f$

(2) when $V_1(t)$ hits $V_T$, M1 turns off. $V_2(0) = 0$.

$\Rightarrow$ approximate circuit as

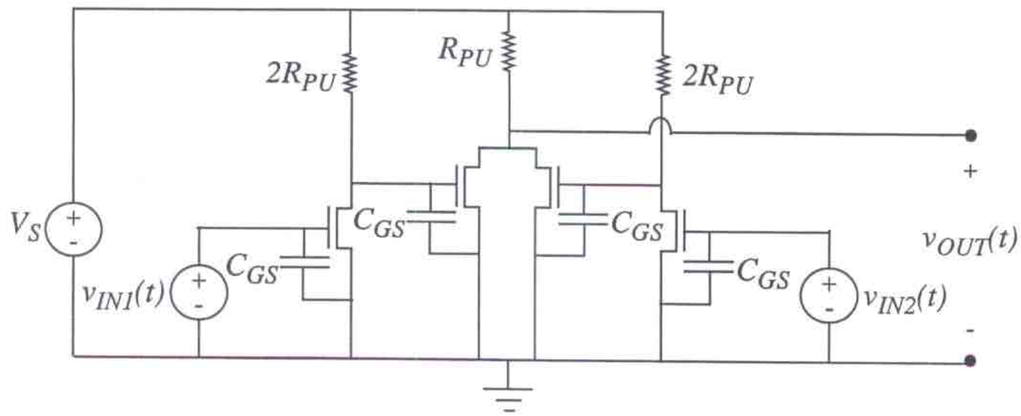


$\Rightarrow V_2(t_r) = V_s (1 - e^{-\frac{t_r}{2R_{pu} C_{gs}}}) = \frac{V_s}{2}$

$\Rightarrow -2R_{pu} C_{gs} \ln \frac{1}{2} = t_r$

| | |
|---|---|
| $T_F = R_{ON} C_{gs} \ln 2$ | $T_R = 2 R_{pu} C_{gs} \ln 2$ |

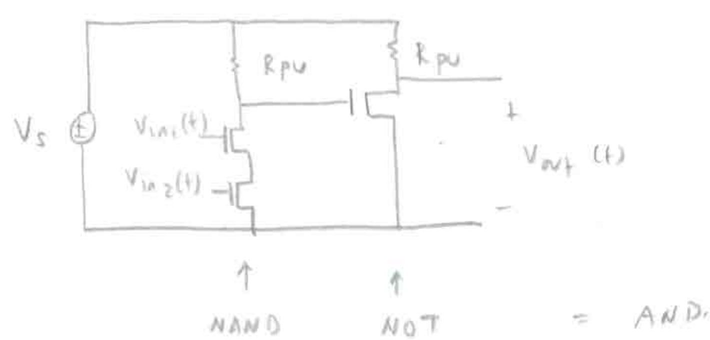
(2B) Assuming that the logic level 0 is represented by a voltage below $V_T$, and that a logic level 1 is represented by a voltage above $V_T$, determine the truth table for the circuit shown below that describes its operation at rest. Also, design an alternative NMOS circuit implementation that uses fewer MOSFETs and fewer resistors.




| Truth Table | | |
|---|---|---|
| IN1 | IN2 | OUT |
| 0 | 0 | 0 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 1 |

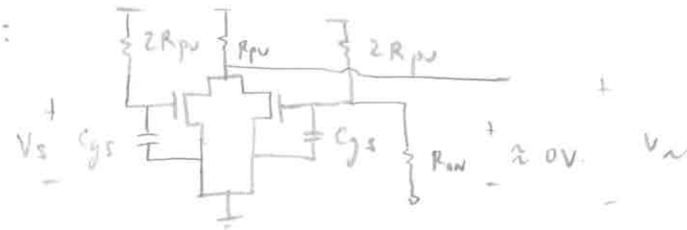
AND function

Implementation:



(2C) Consider the original circuit from Part (B) at rest with $v_{IN1} < V_T$ and $v_{IN2} > V_T$ prior to $t = 0$. At $t = 0$, $v_{IN1}$ rises above $V_T$ while $v_{IN2}$ simultaneously falls below $V_T$. For these inputs, sketch and clearly label the time dependence of $v_{OUT}(t)$ on the axis provided below from slightly before $t = 0$ until slightly after $v_{OUT}(t)$ reaches its steady state. Again, make reasonable approximations based on the inequality $R_{ON} \ll R_{PU}$.

prior to $t=0$ :




$V_{out}(0-) = 0\,V$ per truth table

LHS

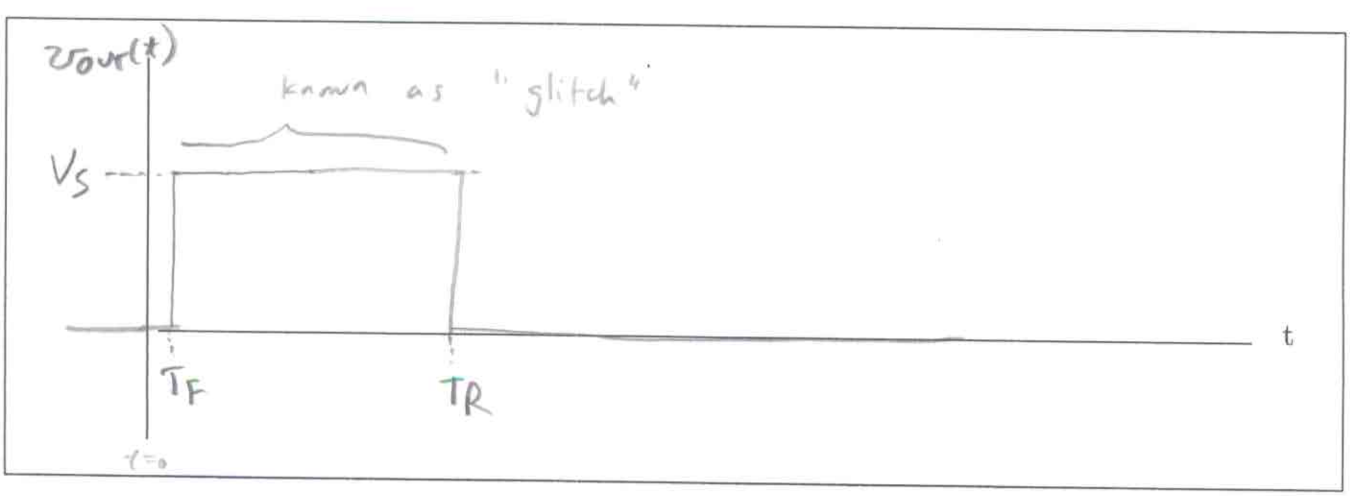
RHS


dis charge, $\tau_L = R_{ON} C_{gs}$ charging, $\tau_R = 2R_{pu} C_{gs}$.

$V_{out} = 0\,V$ as long as either capacitor voltage $> \frac{V_S}{2}$

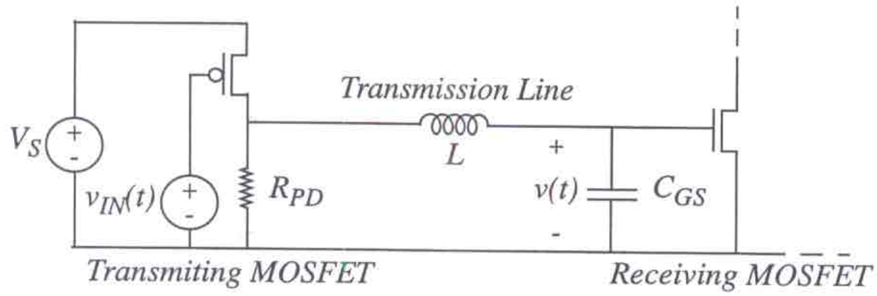
$= V_s$ if both cap voltage $< \frac{V_S}{2}$

$\tau_L \ll \tau_R$ since $R_{ON} \ll R_{pu}$ $\Rightarrow$ LHS $V_c$ drop below $\frac{V_S}{2}$ first ; then RHS $V_C$ rise above $\frac{V_S}{2}$.



## Problem 3 – 20%

In this problem a MOSFET and pull-down resistor having resistance $R_{PD}$ are used to transmit digital data down a transmission line having inductance $L$ as shown below. At the end of the transmission line is a receiving MOSFET having gate-to-source capacitance $C_{GS}$. Model the transmitting MOSFET with a switch-resistor model having on-state resistance $R_{ON}$.

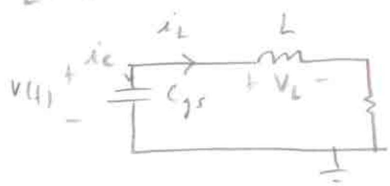



(3A) Assume that $v_{IN}$ turns the transmitting MOSFET off at $t = 0$ after it was on for a very long time. In this case, derive *but do not solve* the differential equation that describes the evolution of $v(t)$, the gate-to-source voltage of the receiving MOSFET. Also provide the corresponding initial conditions in terms of $v(t)$ and its derivatives at $t = 0$.

Trans MOSFET on for long time $\Rightarrow$ $V_R = v(0^-) = \dfrac{R_{PD}}{R_{PD}+R_{ON}}$

Since $V_L = 0$.

@ $t = 0^+$




$i_L(0^-) = i_L(0^+) = 0A$.

$\Rightarrow i_c(0^+) = 0 = C\dfrac{dv_c}{dt} \Rightarrow \left.\dfrac{dv_c}{dt}\right|_{0^+} = 0.$

$$v(t) - V_L - V_R = 0$$

$$\Rightarrow v(t) + L\frac{di_c}{dt} + i_c R = 0. \qquad i_c = C\frac{dv(t)}{dt}$$

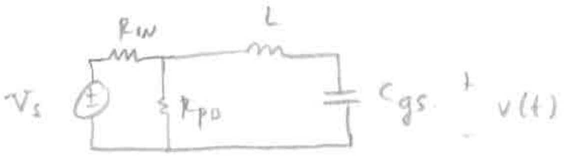
$$\Rightarrow v(t) + LC\frac{d^2v(t)}{dt^2} + RC\frac{dv}{dt} = 0$$

| | |
|---|---|
| Eqn: | $\dfrac{d^2v(t)}{dt^2} + \dfrac{R_{PD}}{L}\dfrac{dv(t)}{dt} + \dfrac{1}{LC}v(t) = 0$ (series RLC) |
| IC: | $v(0^+) = \dfrac{R_{PD}}{R_{PD}+R_{ON}}$, $\left.\dfrac{dv}{dt}\right|_{t=0^+} = 0$ |

(3B) Assume that $v_{\rm IN}$ turns the transmitting MOSFET on at $t = 0$ after it was off for a very long time. In this case, derive *but do not solve* the differential equation that describes the evolution of $v(t)$, the gate-to-source voltage of the receiving MOSFET. Also provide the corresponding initial conditions in terms of $v(t)$ and its derivatives at $t = 0$.

Trans MOSFET off for long time $\Rightarrow$ $v(0^-) = 0\,V$, $i_L(0^-) = 0\,A$.

@ $t = 0^+$




$\Rightarrow$


$\Rightarrow$ Same circuit as in (3A) except with excitation source

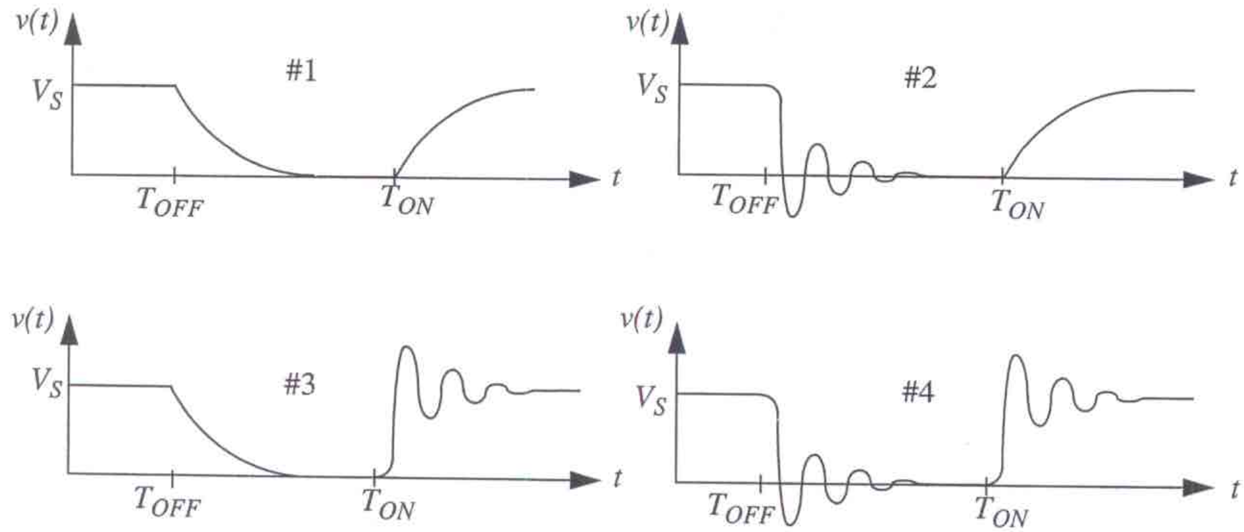
$$\Rightarrow \frac{R_{PD}}{R_{IN} + R_{PD}} V_s - i_c R_{eq} - L \frac{d i_c}{dt} - v(t) = 0 \quad , \quad i_c = C \frac{dv}{dt}.$$

$$\Rightarrow \frac{R_{PD}}{R_{ON} + R_{PD}} V_s = R_{eq} C \frac{dv}{dt} + LC \frac{d^2 V}{dt^2} + V$$

Eqn: $$\frac{d^2 v(t)}{dt^2} + \frac{R_{ON} // R_{PD}}{L} \frac{d v(t)}{dt} + \frac{1}{LC} v(t) = \frac{1}{LC} \frac{R_{PD}}{R_{ON} + R_{PD}} V_s.$$

IC: $v(0^+) = 0\,V$, $\left.\frac{dv}{dt}\right|_{t=0^+} = 0$

(3C) Assume that $R_{\mathrm{ON}} \ll \sqrt{L/C_{\mathrm{GS}}} \ll R_{\mathrm{PD}}$. In this case, which of the following sketches best describes the evolution of $v(t)$ given that the transmitting MOSFET turns on at $T_{\mathrm{ON}}$ and off at $T_{\mathrm{OFF}}$? Why?




To see behavior @ $T_{off}$, must look at

$\sqrt{\alpha^2 - \omega_0^2} = \sqrt{\left(\frac{R_{PD}}{2L}\right)^2 - \frac{1}{LC}}$ $\quad R_{PD} \gg \sqrt{\frac{L}{C_{gs}}} \Rightarrow R_{PD}^2 \gg \frac{L}{C_{gs}}$

$\Rightarrow \frac{R_{PD}^2}{4L^2} \gg \frac{1}{LC_{gs}}$

$\Rightarrow$ turn off transient is over damped

@ $T_{ON}$ must look at

$\sqrt{\alpha^2 - \omega_0^2} \approx \sqrt{\left(\frac{R_{ON}}{2L}\right)^2 - \frac{1}{LC}}$ $\quad R_{ON} \ll \sqrt{\frac{L}{C_{gs}}} \Rightarrow R_{ON}^2 \ll \frac{L}{C_{gs}}$

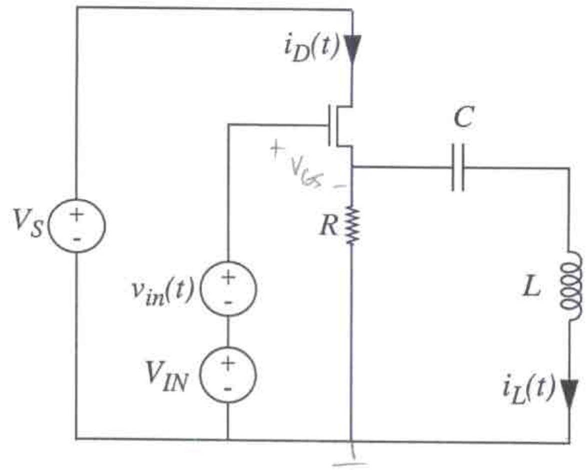
$\Rightarrow \frac{R_{ON}^2}{4L^2} \ll \frac{1}{LC_{gs}}$

$\Rightarrow$ turn on transient is under damped

Sketch: #3 Why? $T_{off}$ over damped $\Rightarrow$ exp response
$T_{on}$ under damped $\Rightarrow$ oscillatory response.

**Problem 4 – 20%**

A MOSFET amplifier is coupled to an inductive load through a capacitor as shown below. The MOSFET is biased into saturated operation by the large signal $V_{\mathrm{IN}}$ so that $i_{\mathrm{D}}(t) = \frac{K}{2}(v_{\mathrm{GS}}(t) - V_{\mathrm{T}})^2$. In addition, the MOSFET is excited by the small signal $v_{\mathrm{in}}(t)$.




(4A) Let $v_{\mathrm{in}}(t) = 0$, and determine $I_{\mathrm{D}}$ and $I_{\mathrm{L}}$, the large-signal bias components of $i_{\mathrm{D}}(t)$ and $i_{\mathrm{L}}(t)$, respectively, in terms of $V_{\mathrm{IN}}$ and the MOSFET and circuit parameters.

$V_{IN}$ is DC signal $\Rightarrow$ cap looks like open so $I_L = 0A$.

$$\frac{V_{IN} - V_{GS}}{R} = I_D = \frac{K}{2}(V_{GS} - V_T)^2$$

$$\Rightarrow \frac{KR}{2}(V_{GS} - V_T)^2 + (V_{GS} - V_T) - (V_{IN} - V_T) = 0$$

$$\Rightarrow V_{GS} - V_T = \frac{-1 + \sqrt{1 + 2KR(V_{IN} - V_T)}}{KR}$$ +ve turns sat m

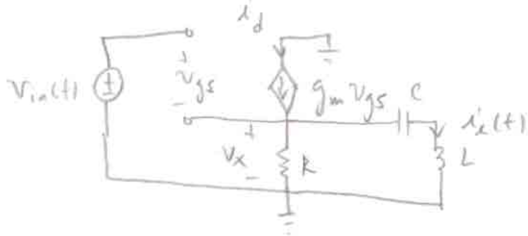
$$\Rightarrow V_{GS} = V_T + \frac{-1 + \sqrt{1 + 2KR(V_{IN} - V_T)}}{KR}.$$

$$I_D = \frac{V_{IN} - V_{GS}}{R} = \frac{V_{IN} - V_T - \frac{-1 + \sqrt{1 + 2KR(V_{IN} - V_T)}}{KR}}{R}.$$

$I_{\mathrm{D}} = \frac{1}{R}\left[V_{IN} - V_T - \frac{\sqrt{1 + 2KR(V_{IN} - V_T)} - 1}{KR}\right].$

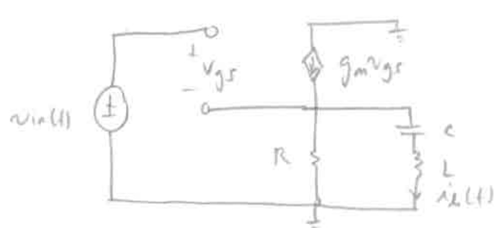
$I_{\mathrm{L}} =$ 0A

(4B) Draw a small-signal circuit model that relates $i_l(t)$, the small-signal component of $i_L(t)$, to $v_{in}(t)$. Clearly label all parameters in the small-signal circuit model.




$$g_m = \frac{\partial i_D}{\partial v_{GS}}\Big|_Q = \boxed{K(V_{GS} - V_T)}$$

Circuit:




$$g_m = K(V_{GS} - V_T)$$

(4C) Assume that $v_{\text{in}}(t) = \Re\{V_{\text{in}}e^{j\omega t}\}$ such that $i_l(t) = \Re\{I_l e^{j\omega t}\}$ where $V_{\text{in}}$, and $I_l$ are complex constants. Determine $I_l$ in terms of $V_{\text{in}}$ and the small-signal circuit model parameters.

$$V_{IN} = V_{gs} + V_x = V_{gs} + g_m V_{gs} Z_{eff}$$

$$= V_{gs}(1 + g_m Z_{eff})$$

$$Z_{eff} = R \,//\, \left[\frac{1}{j\omega C} + j\omega L\right]$$

$$= R \,//\, \left[\frac{1-\omega^2 LC}{j\omega C}\right] = \frac{R\left(\frac{1-\omega^2 LC}{j\omega C}\right)}{R + \frac{1-\omega^2 LC}{j\omega C}}$$

$$= \frac{R(1-\omega^2 LC)}{(1-\omega^2 LC) + j\omega CR}$$

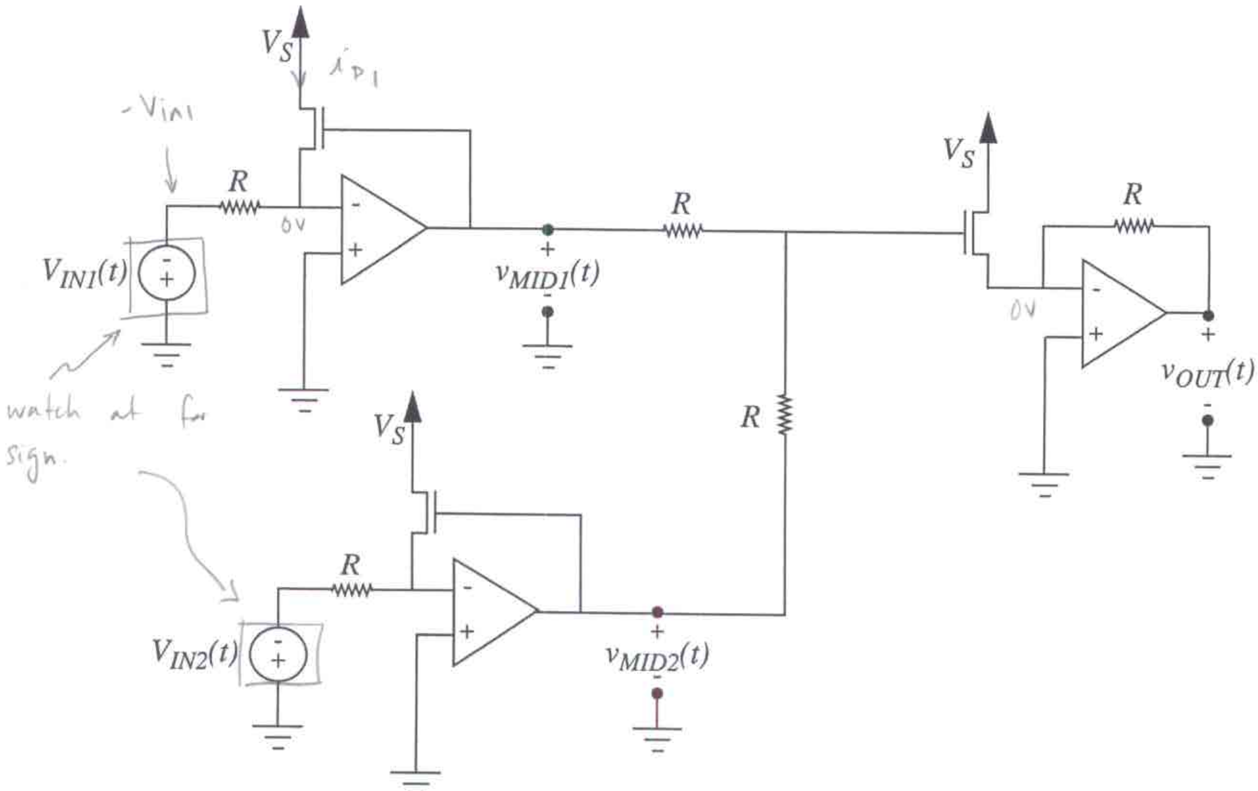
$$\Rightarrow \quad V_{gs} = \frac{V_{IN}}{1 + g_m Z_{eff}}$$

$$\Rightarrow \quad i_l = \frac{R}{R + \frac{1}{j\omega C} + j\omega L}\, g_m \frac{V_{in}}{1 + g_m Z_{eff}}$$

$$I_l = \frac{g_m}{1 + g_m Z_{eff}} \cdot \frac{R}{R + \frac{1}{j\omega C} + j\omega L} V_{in} \qquad Z_{eff} = \frac{R(1-\omega^2 LC)}{(1-\omega^2 LC) + j\omega RC}$$

## Problem 5 – 20%

The circuit shown below has two non-negative input voltages, $v_{IN1}(t)$ and $v_{IN2}(t)$, and one output voltage $v_{OUT}(t)$; two intermediate voltages, $v_{MID1}(t)$ and $v_{MID2}(t)$, are also defined. In analyzing this circuit, assume that each op-amp is ideal and that each MOSFET operates in its saturation region so that $i_D(t) = \frac{K}{2}(v_{GS}(t) - V_T)^2$.



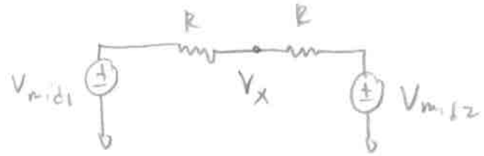

(5A) Determine $v_{MID1}(t)$ as a function of $v_{IN1}(t)$.

$$i_{D1} = \frac{K}{2}(V_{mid1} - V_T)^2 = \frac{V_{in1}}{R}$$

$$V_{mid1} = V_T + \sqrt{\frac{2V_{in1}}{KR}}$$

$v_{MID1}(t) =$ $V_T + \sqrt{\frac{2V_{in1}}{KR}}$

(5B) Determine $v_{\mathrm{OUT}}(t)$ as a function of $v_{\mathrm{MID1}}(t)$ and $v_{\mathrm{MID2}}(t)$.




$$V_x = \frac{V_{mid1} + V_{mid2}}{2}.$$

Think of a "weighting" circuit like DAC.

$$I_{D0} = \frac{k}{2}(V_x - V_T)^2 = -\frac{V_{out}}{R}.$$

$$\Rightarrow \quad V_{out} = -\frac{kR}{2}(V_x - V_T)^2$$

$$v_{\mathrm{OUT}}(t) = -\frac{kR}{2}\left[\left(\frac{V_{mid1} + V_{mid2}}{2}\right) - V_T\right]^2$$

(5C) Determine $v_{OUT}(t)$ as a function of $v_{IN1}(t)$ and $v_{IN2}(t)$.

$$V_{mid1} = V_T + \sqrt{\frac{2V_{in1}}{KR}}$$

By symmetry, $V_{mid2} = V_T + \sqrt{\frac{2V_{in2}}{KR}}$.

$$\Rightarrow V_X = \frac{2V_T + \sqrt{\frac{2V_{in1}}{KR}} + \sqrt{\frac{2V_{in2}}{KR}}}{2}$$

$$= V_T + \frac{1}{2}\left[\sqrt{\frac{2V_{in1}}{KR}} + \sqrt{\frac{2V_{in2}}{KR}}\right].$$

$v_{OUT}(t) =$ $-\frac{KR}{8}\left[\sqrt{\frac{2V_{in1}}{KR}} - \sqrt{\frac{2V_{in2}}{KR}}\right]^2$