TENTATIVE LECTURE SCHEDULE

Date	Lecture	Reading Assignment
SEMICONDUCTOR FUNDAMENTALS		
September 7	6.012 overview; key conclusions of 6.012	1.1-1.4
September 12	Intro to semiconductors: electrons and holes, donors and acceptors	2.1-2.3
September 14	Carrier transport: drift and diffusion	2.4 -2.6
MOSFET		
September 19	Semiconductor electrostatics; the "60 mVrule"	3.1-3.2
September 21	p-n junction electrostatics in thermal equilibrium	3.3-3.6
September 26	MOS electrostatics in thermal equilibrium	3.7-3.8
September 28	MOS under bias, MOS capacitance	3.8-3.9
October 3	MOS: IV characteristics	4.1-4.3
October 5	MOSFET: saturation, backgate effect	4.4
October 10	**Columbus Day**	
October 12	MOSFET: Equivalent circuit models	4.5-4.6
DIGITAL CIRCUITS		
October 17	Logic concepts, Inverter characteristics, NMOS inverter	5.1-5.3.2
October 19	CMOS inverter: transfer characteristics	5.3-5.4
October 24	CMOS inverter: delay; CMOS scaling, VLSI	5.4-5.5
BIPOLAR TRANSISTORS		
October 26	p-n junction diode: IV characteristics	6.1-6.3
October 31	p-n junction diode: equivalent circuit models	6.4-6.5, 6.9
November 2	BJT: electrostatics & forward active region	7.1-7.2
November 7	BJT: saturation, reverse active region & cut-off, equivalent cct. models	7.3-7.5
ANALOG CIRCUITS		
November 9	Single-stage Amplifiers: fundamentals, Common source amplifier	8.1-8.5
November 14	Common emitter amplifier	8.6
November 16	Common drain amplifier & common gate amplifier	8.7-8.9
November 21	Frequency response of common source amplifier	10.1-10.4
November 23	**Thanksgiving Day**	
November 28	Open-circuit time constant technique	10.4-10.5
November 30	Frequency response of other amplifier stages	10.5-10.6
December 5	Multi-stage amplifiers	9.1-9.3
December 7	DC voltage and current sources	9.4
December 12	Differential Amplifier: DC analysis, incremental analysis	11.1-11.6

Tentative Schedule of Quizzes and Major Assignments

Problem Sets

There will be a total of eight graded problems sets. They are assigned approximately once a week and are due a week later. No problem set is due on the week of quizzes.

Problem Set	Assigned	Due
PS#1	9/8	9/15
PS#2	9/15	9/22
PS#3	9/22	9/29
PS#4	9/29	10/06
PS#5	10/13	10/20
PS#6	10/27	11/03
PS#7	11/03	11/09
PS#8	11/14	11/22
PS#9	12/05	Not graded

Design Projects

Design Project #1	Assigned: October 18	Due: November 1
Design Project #2	Assigned: November 21	Due: December 1

Quizzes

Quiz #1	October 11	7:30 – 9:30 PM	Walker Memorial
Quiz #2	November 15	7:30 – 9:30 PM	Walker Memorial

Final Examination

Three-hour Examination	Scheduled by the Registrar's Office	December 18-22