Lecture 26

Differential Amplifiers (I)

DIFFERENTIAL AMPLIFIERS

Outline

1. Introduction
2. Incremental analysis of differential amplifier
3. Common-source differential amplifier

Reading Assignment:
Howe and Sodini, Chapter 11, Sections 11-1-11.3, 11.6

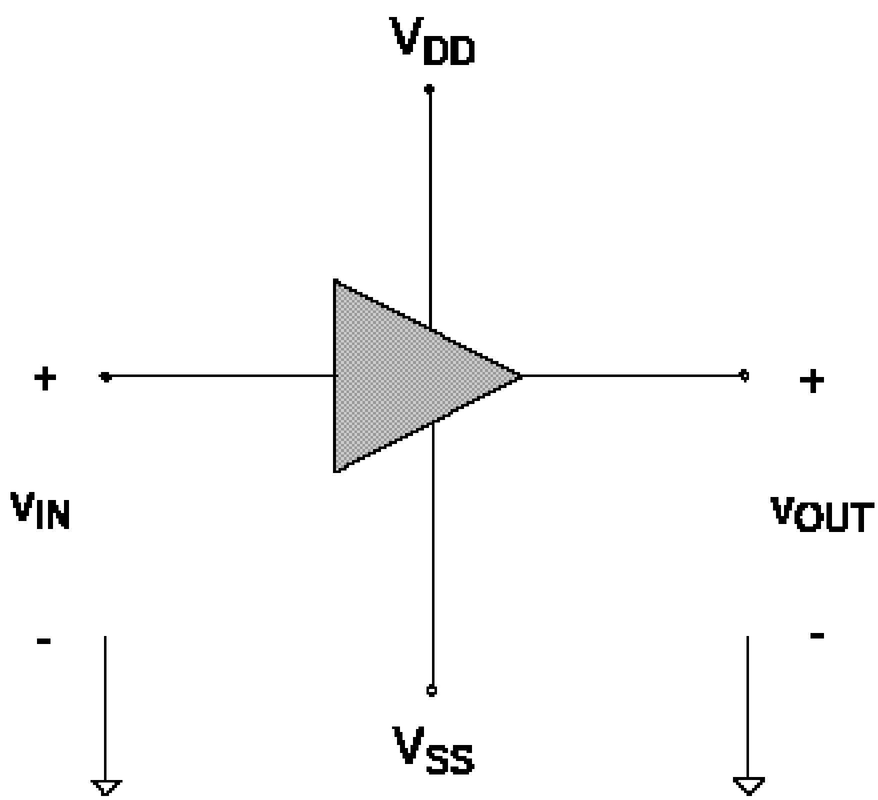
Summary of Key Concepts

- In differential amplifiers, signals are represented by ***difference*** between two voltages
- Differential amplifier amplifies the difference between two voltages but rejects "***common mode***" signals
  - $\Rightarrow$ Improved noise immunity
- Using "***half-circuit***" technique, small-signal operation of differential amplifiers is analyzed by breaking the problem into two simpler ones
  - ***Differential mode*** problem
  - ***Common mode*** problem
- ***Common-mode rejection ratio*** (CMRR) is an important figure of merit for differential amplifiers
- Differential amplifiers require good device matching

1. Introduction

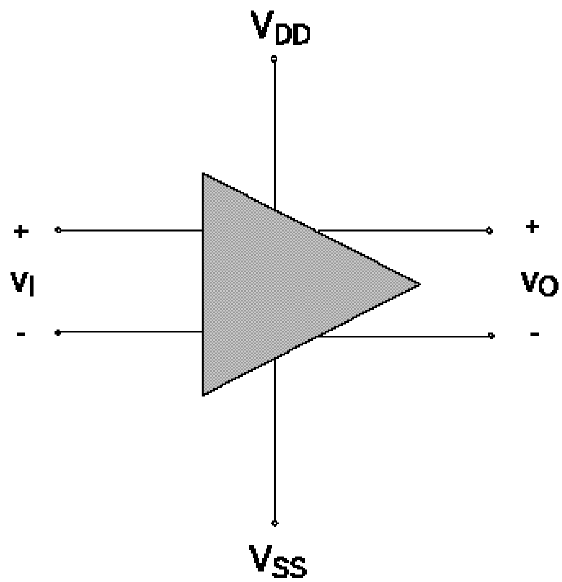
Two problems found in single-transistor amplifier stages are:

- Bias and gain sensitivity to device parameters (μC_{ox}, V_T)
  - Sensitivity can be mitigated but often at a price in terms of performance or cost (gain, power, device area, etc.)
- Vulnerability to ground and power supply noise
  - In dense IC's there is cross-talk, 60 Hz coupling, substrate noise, etc.



Introduction (contd.)

Solution : represent relevant signal by the difference between two voltages

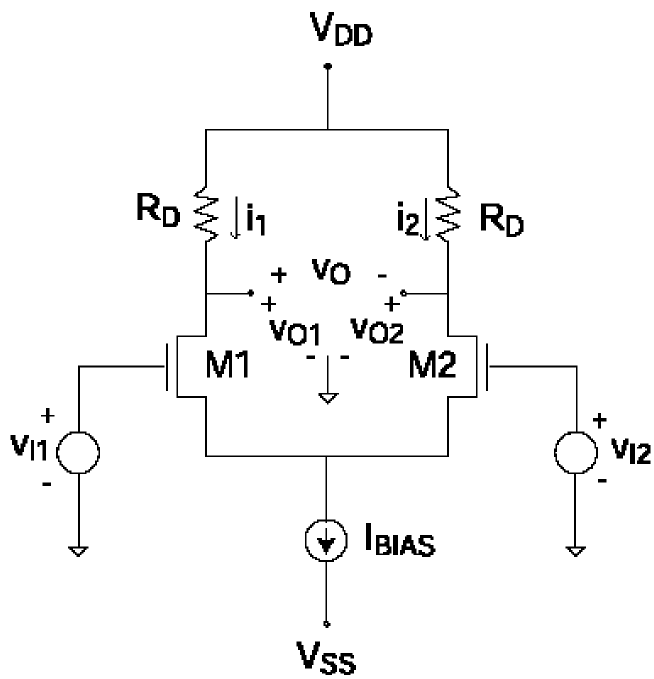


Differential Amplifier:

- Amplifies **difference** between two voltages
- Rejects components **common** to both voltages

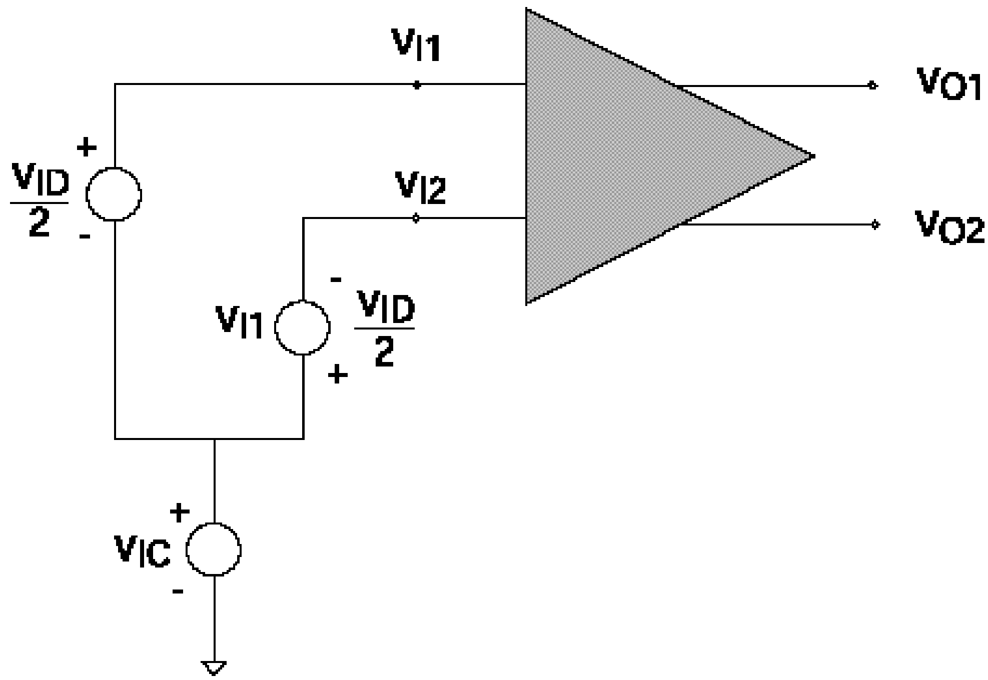
MOSFET Differential Amplifier

Basic Configuration



- v_O responds to difference between v_I's
  - If $v_{I1} = v_{I2} \Rightarrow$ symmetry $\Rightarrow v_{O1} = v_{O2} \Rightarrow v_O = 0$
  - If $v_{I1} > v_{I2} \Rightarrow$ M1 conducts more than M2 $\Rightarrow i_1 > i_2 \Rightarrow v_{O1} < v_{O2} \Rightarrow v_O < 0$
- v_O insensitive to common mode signals:
  - If both v_{O1} and v_{O2} move in sync, symmetry is preserved $\Rightarrow v_O$ unchanged
  - If ground V_{DD} or V_{SS} have noise, symmetry preserved $\Rightarrow v_O$ unchanged
  - If V_T or μC_{ox} change, symmetry preserved $\Rightarrow v_O$ unchanged.
- Need precise device matching

Differential-mode and Common-mode signals



Distinguish between common-mode and differential-mode:

$$\mathbf{v}_{I1} = \mathbf{v}_{IC} + \frac{\mathbf{v}_{ID}}{2}, \qquad \mathbf{v}_{I2} = \mathbf{v}_{IC} - \frac{\mathbf{v}_{ID}}{2}$$

Then:

$$\mathbf{v}_{ID} = \mathbf{v}_{I1} - \mathbf{v}_{I2}, \qquad \mathbf{v}_{IC} = \frac{\mathbf{v}_{I1} + \mathbf{v}_{I2}}{2}$$

Similarly at the output:

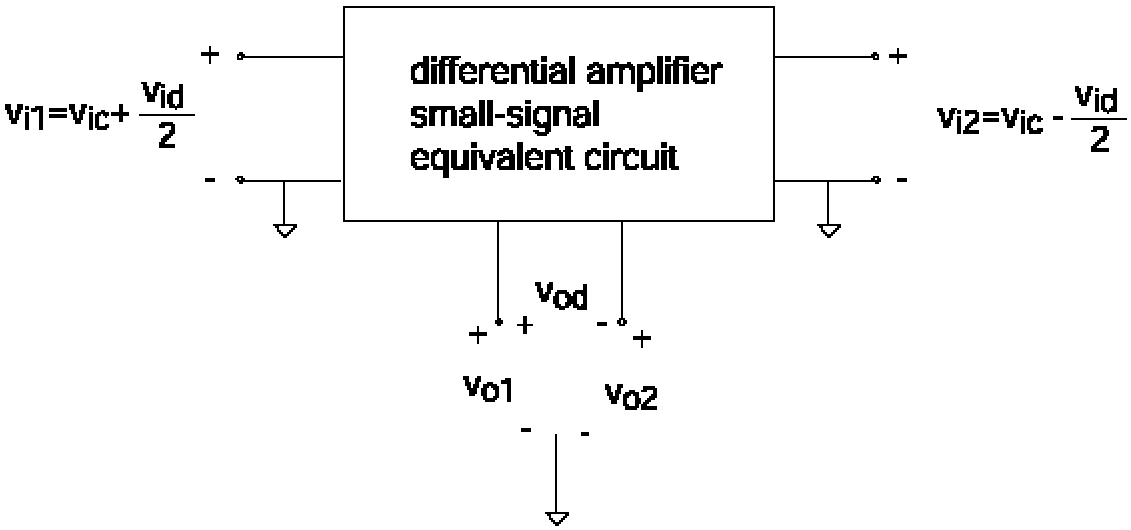
$$\mathbf{v}_{O1} = \mathbf{v}_{OC} + \frac{\mathbf{v}_{OD}}{2}, \qquad \mathbf{v}_{O2} = \mathbf{v}_{OC} - \frac{\mathbf{v}_{OD}}{2}$$

Then:

$$\mathbf{v}_{OD} = \mathbf{v}_{O1} - \mathbf{v}_{O2}, \qquad \mathbf{v}_{OC} = \frac{\mathbf{v}_{O1} + \mathbf{v}_{O2}}{2}$$

2. Incremental analysis of differential amplifier

Consider generic differential amplifier:



Figures of Merit:

Differential-mode voltage gain (**want it high**):

$$\mathbf{a_{dm}} = \frac{\mathbf{v_{od}}}{\mathbf{v_{id}}}$$

Common-mode voltage gain (**want it small**):

$$\mathbf{a_{cm}} = \frac{\mathbf{v_{oc}}}{\mathbf{v_{ic}}}$$

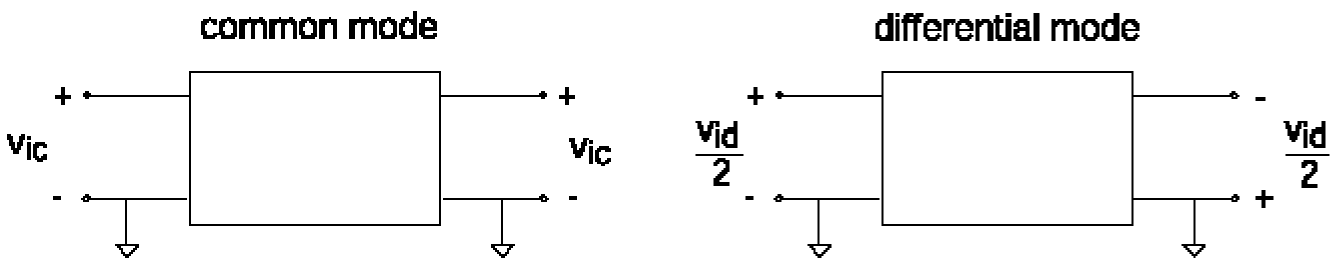
Common-mode rejection ratio (**want it very high**):

$$\mathbf{CMRR} = \frac{\mathbf{a_{dm}}}{\mathbf{a_{cm}}}$$

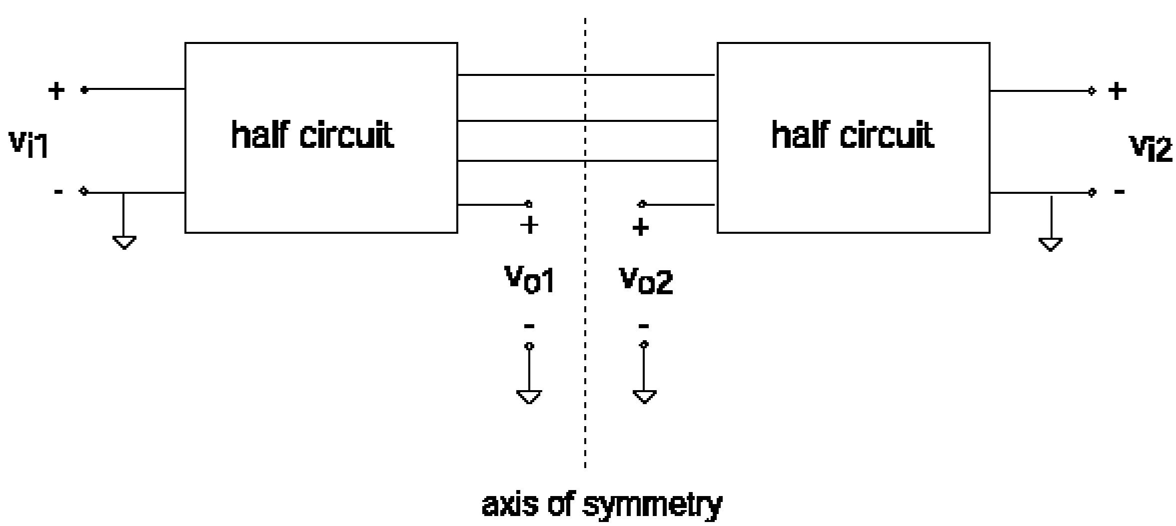
Incremental analysis of differential amplifier (contd.)

Two steps to simplify the problem:

1. Use superposition and break the problem into two:



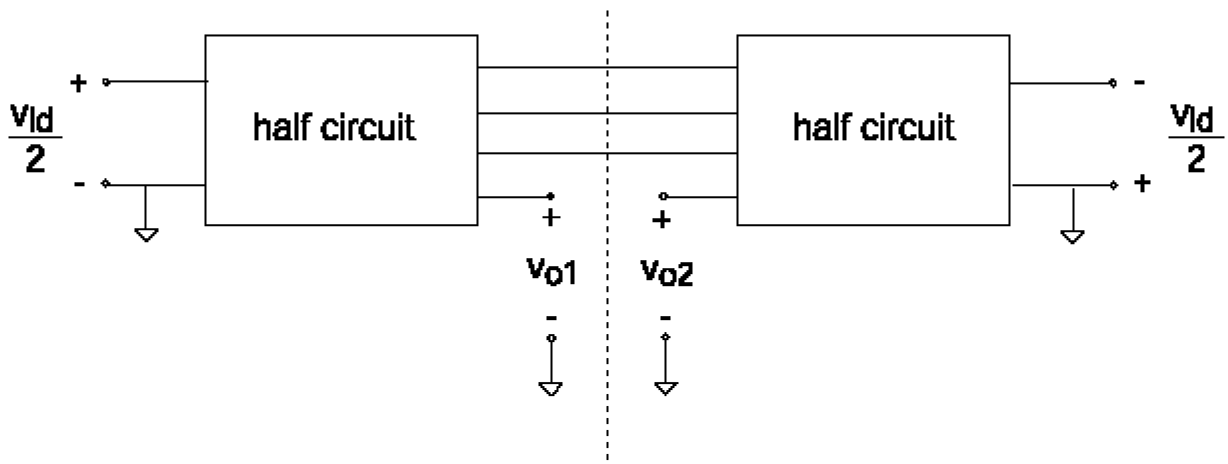
2. Exploit symmetry:



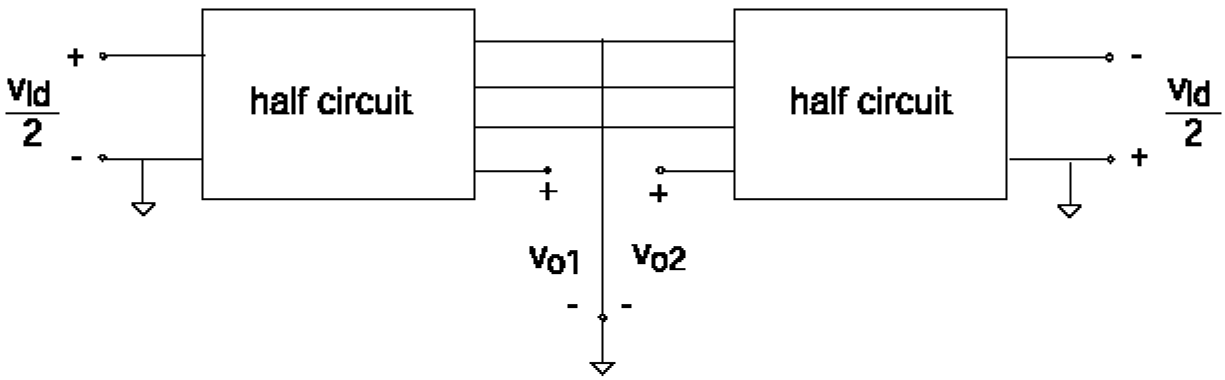
Circuit broken into two "half circuits".

Incremental analysis of differential amplifier

Differential-mode Analysis



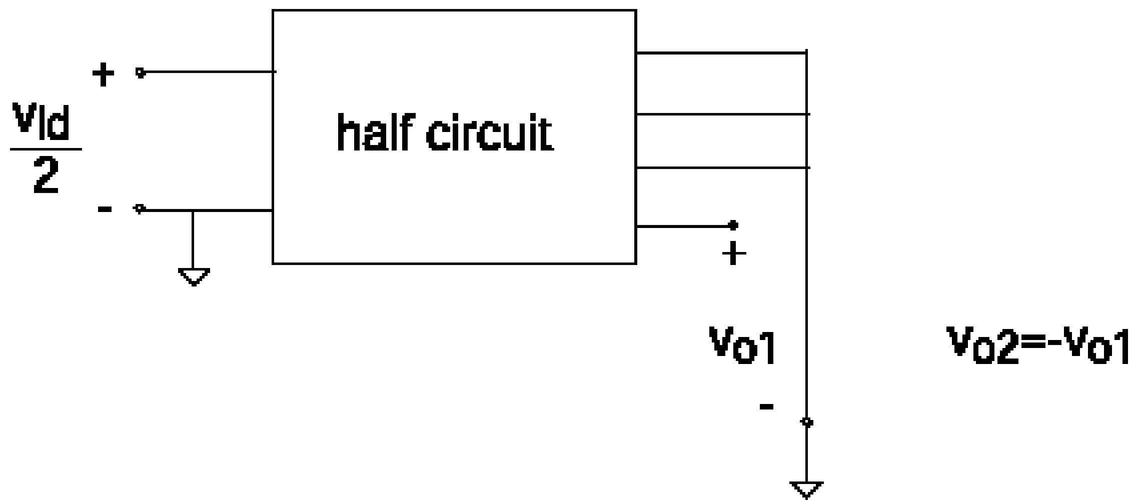
No voltage relative to ground along axis of symmetry ⇒ circuit identical to:



Incremental analysis of differential amplifier

Differential-mode Analysis (contd.)

Need to solve:



Differential-mode voltage gain:

$$a_{dm} = \frac{v_{od}}{v_{id}} = \frac{v_{o2} - v_{o1}}{v_{i2} - v_{i1}}$$

In differential –mode:

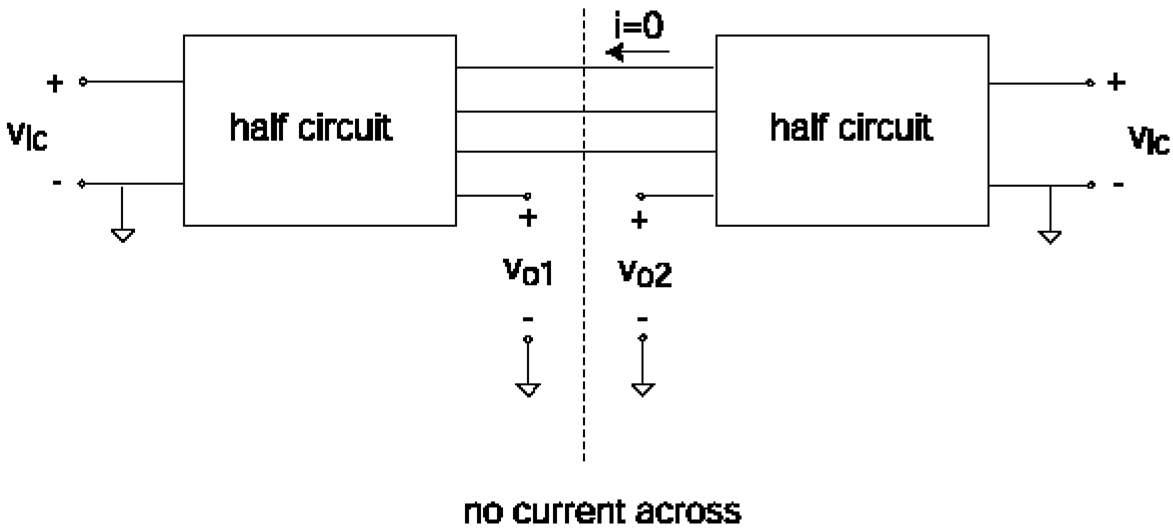
$$v_{i1} = -v_{i2} = \frac{v_{id}}{2} \quad \text{and} \quad v_{o1} = -v_{o2}$$

Then:

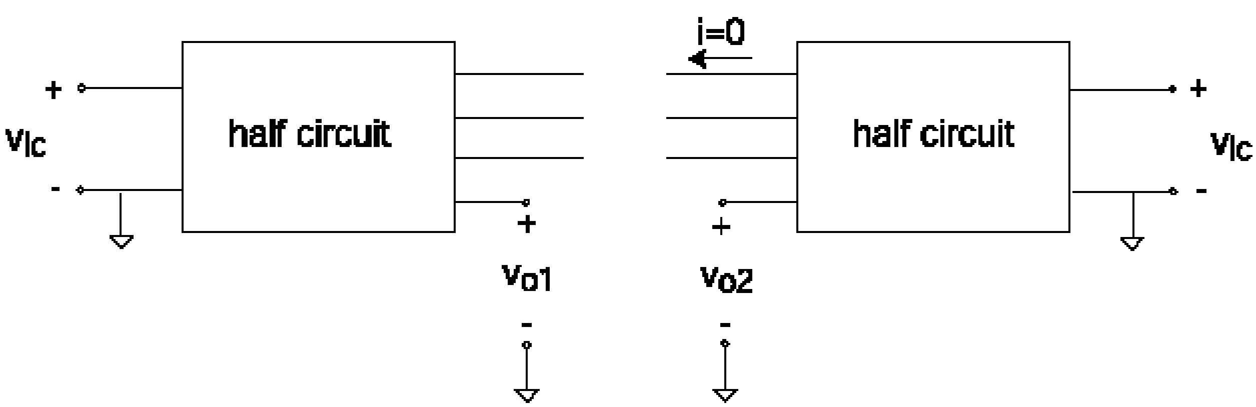
$$a_{dm} = \frac{2v_{o1}}{v_{id}} = \frac{v_{o1}}{\frac{v_{id}}{2}}$$

Incremental analysis of differential amplifier

Common-mode Analysis

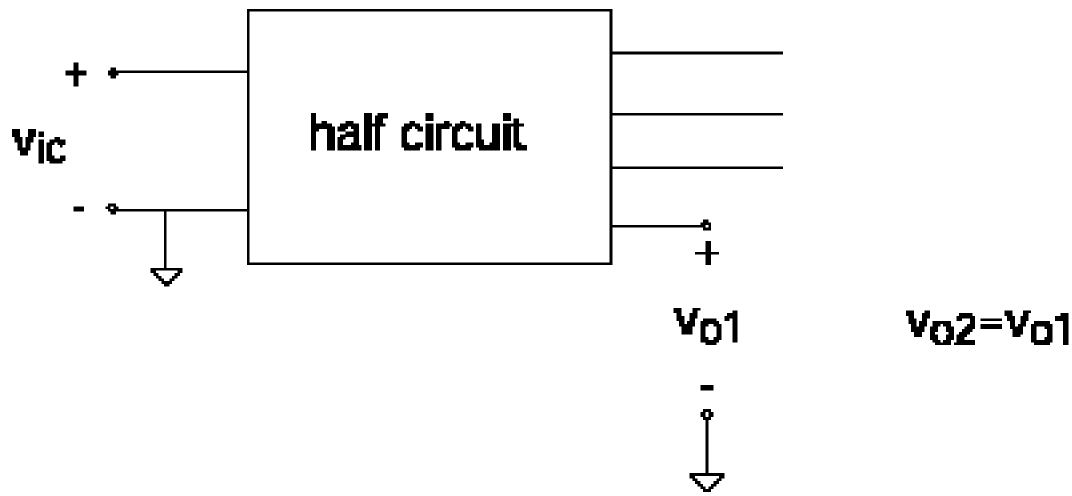


No current across wires connecting the two half-circuits
⇒ circuit is identical to:



Incremental analysis of differential amplifier

Common-mode Analysis (contd.)



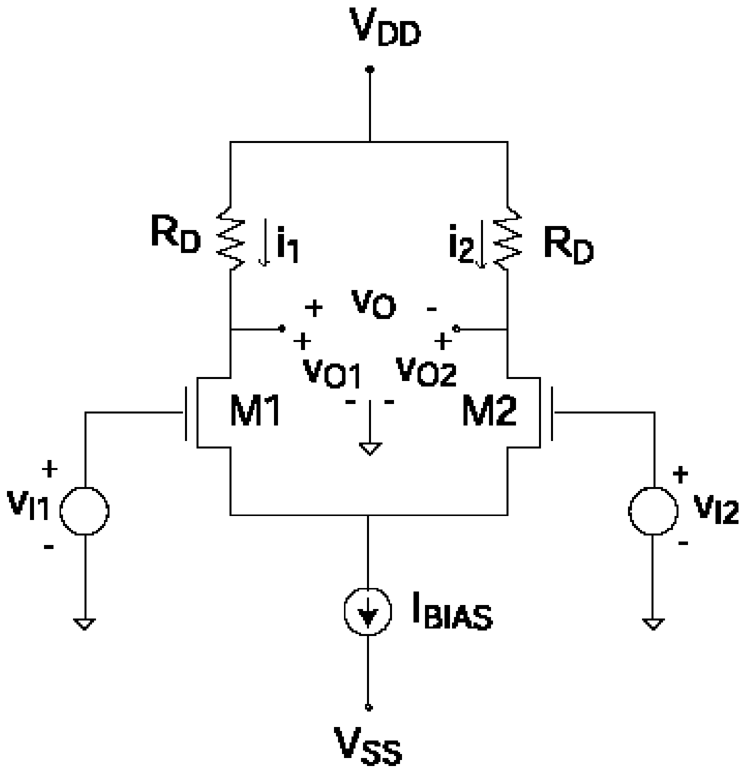
Common-mode voltage gain:

$$\mathbf{a_{cm}} = \frac{\mathbf{v_{oc}}}{\mathbf{v_{ic}}} = \frac{\frac{\mathbf{v_{o2}} + \mathbf{v_{o1}}}{2}}{\mathbf{v_{ic}}}$$

In common–mode, $v_{o1} = v_{o2}$, then:

$$\mathbf{a_{cm}} = \frac{\mathbf{v_{o1}}}{\mathbf{v_{ic}}}$$

3. Common-source differential amplifier (source-coupled pair)



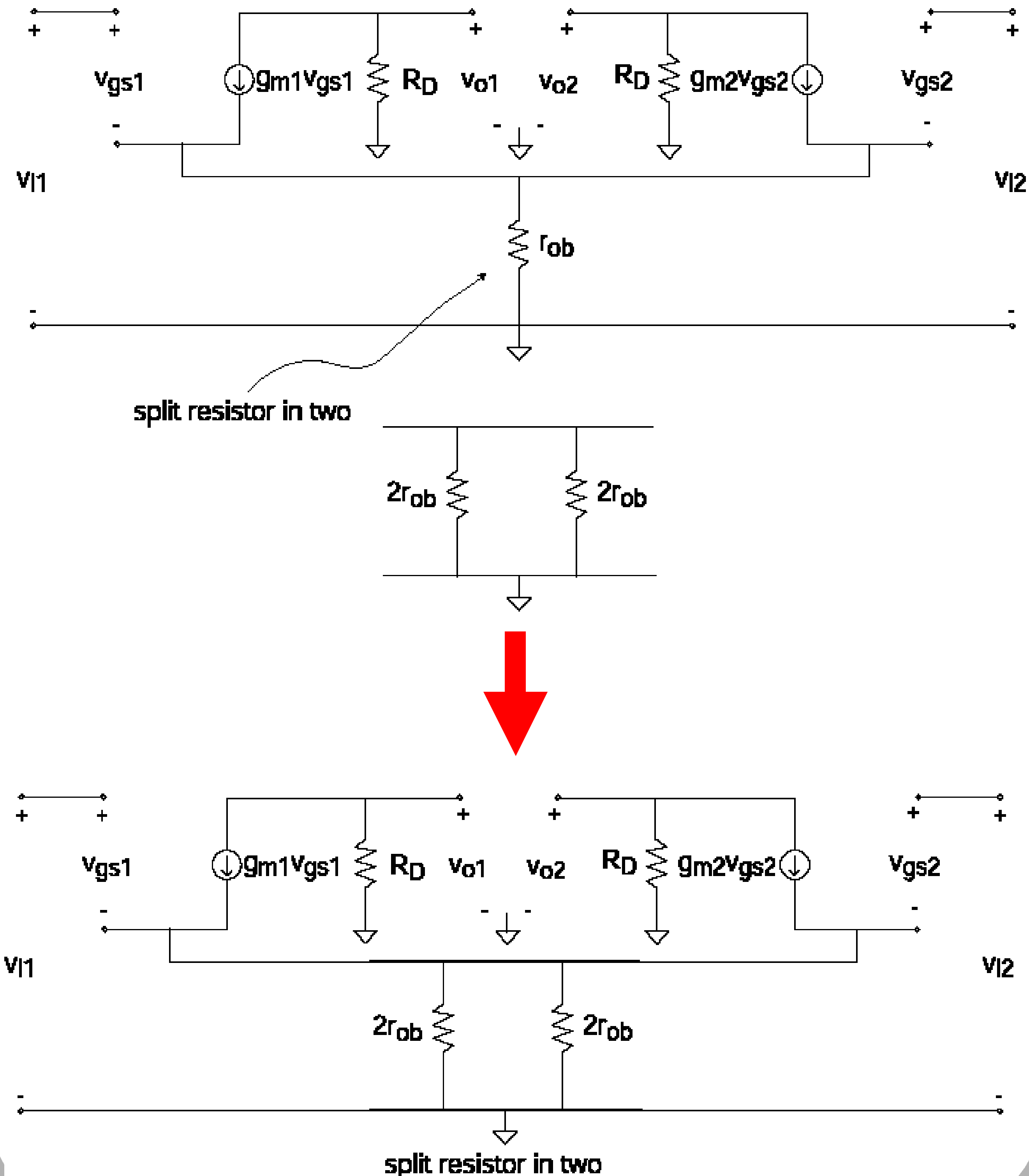
Biasing Issues: must keep MOSFET's in saturation

- Upper limit to V_{I1} and V_{I2}: MI and M2 driven into linear regime:

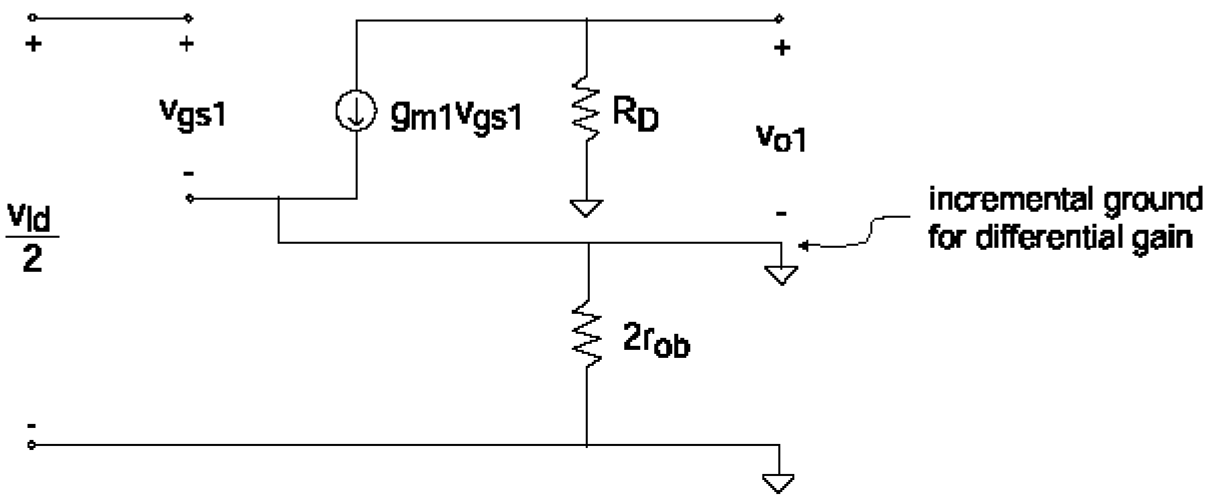
$$\mathbf{V}_{\mathbf{IC},\max} = \mathbf{V}_{\mathbf{O}1} + \mathbf{V}_{\mathbf{T}} = \mathbf{V}_{\mathbf{T}} + \mathbf{V}_{\mathbf{DD}} - \mathbf{R}_{\mathbf{D}} \frac{\mathbf{I}_{\mathbf{BIAS}}}{2}$$

- Lower limit to V_{I1} and V_{I2}: set by circuit that implements I_{BIAS}.

Common-source differential amplifier
(small-signal equivalent circuit model)



Common-source differential amplifier
Differential-mode half circuit



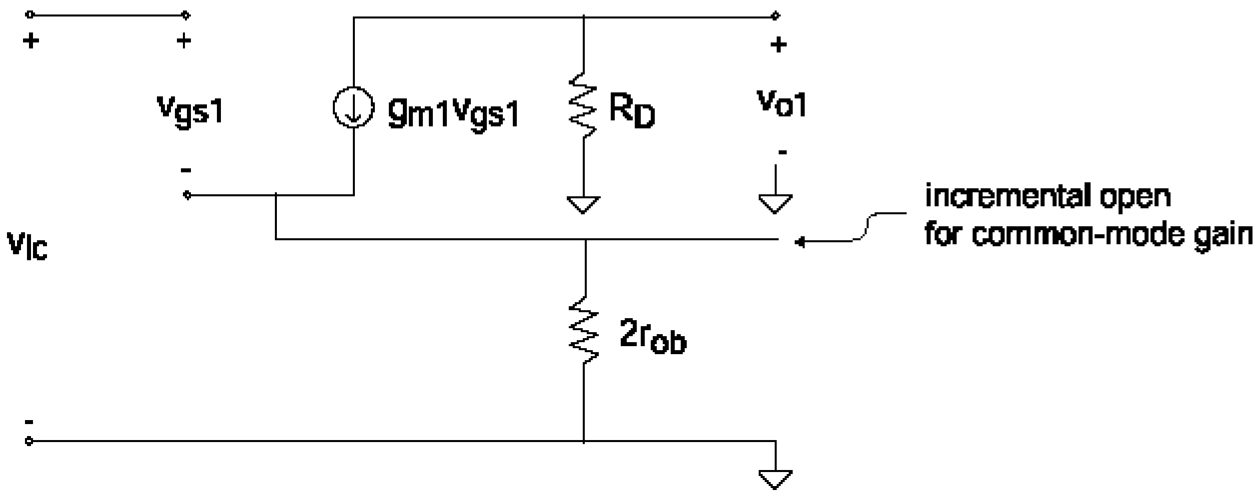
$$v_{o1} = -g_{m1} R_D \frac{v_{id}}{2}$$

Then the differential mode gain is

$$a_{dm} = \frac{v_{o1}}{\frac{v_{id}}{2}} = -g_{m1} R_D$$

Common-source differential amplifier

Common-mode half circuit



$$v_{o1} = -\frac{g_{m1} R_D}{1 + 2 g_{m1} r_{ob}} \bullet v_{ic}$$

Then the common-mode gain is

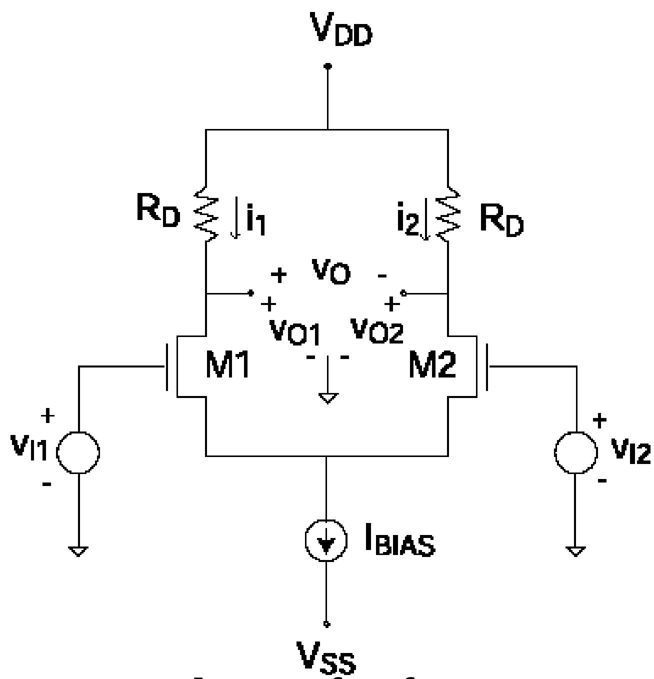
$$a_{cm} = \frac{v_{o1}}{v_{ic}} = -\frac{g_{m1} R_D}{1 + 2 g_{m1} r_{ob}}$$

Common-mode Rejection Ratio (CMRR):

$$\mathrm{CMRR} = \frac{a_{dm}}{a_{cm}} = \frac{-g_{m1} R_D}{-\dfrac{g_{m1} R_D}{1 + 2 g_{m1} r_{ob}}} = 1 + 2 g_{m1} r_{ob}$$

To get good CMRR, need good current source.

Large-signal response of differential amplifier



Examine large-signal transfer function:

- If $v_{I1} = v_{I2} \Rightarrow v_{O1} = v_{O2} \Rightarrow v_O = 0$
- If $v_{I1} > v_{I2} \Rightarrow$ M1 conducts more than M2 $\Rightarrow i_1 > i_2$
  $\Rightarrow v_{O1} < v_{O2} \Rightarrow \; v_O < 0$
- If $v_{I1} >> v_{I2} \Rightarrow$ M1 conducts strongly, M2 turns off
  $\Rightarrow i_1 \approx I_{BIAS}, \; i_2 \approx 0 \Rightarrow$

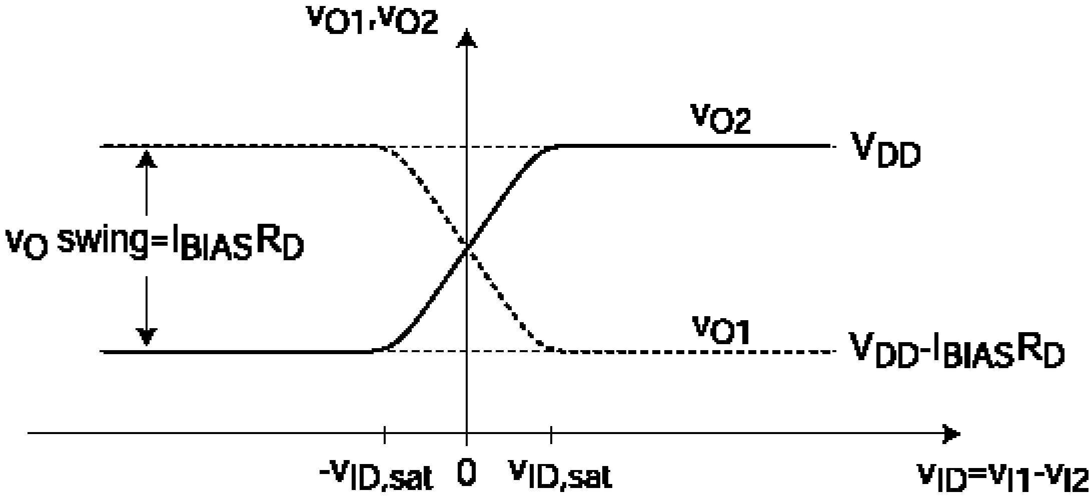
  $$\mathbf{v_{O1}} = \mathbf{v_{O1,min}} = \mathbf{V_{DD}} - \mathbf{I_{BAIS}R_D}, \qquad \mathbf{v_{O2}} = \mathbf{v_{O1,max}} = \mathbf{V_{DD}}$$

  $$\mathbf{v_{OD,min}} = -\mathbf{I_{BAIS}R_D}$$

- Symmetric behavior for $v_{I1} < v_{I2}$ and $v_{I1} << v_{I2}$

Large-signal response of differential amplifier (contd.)

Saturating behavior for large differential input signals:



v_{ID} that leads to amplifier saturation ($v_{I1} >> v_{I2}$):

$$\mathbf{v_{ID,sat}} = \mathbf{v_{GS1}} - \mathbf{v_{GS2}}$$

With:

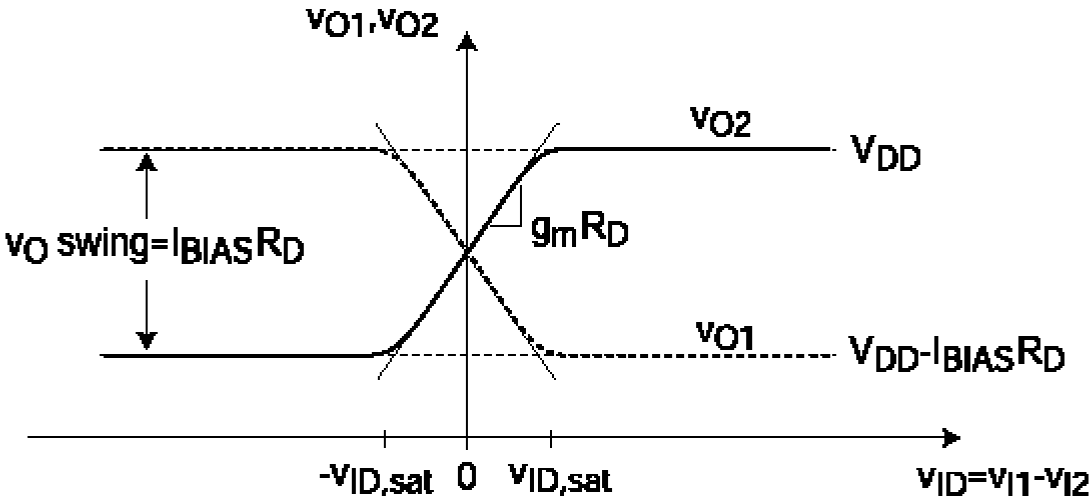
$$\mathbf{v_{GS1}} = \mathbf{V_T} + \sqrt{\frac{\mathbf{I_{BAIS}}}{\frac{\mathbf{W}}{2\mathbf{L}}\mu\mathbf{C_{ox}}}}$$

$$\mathbf{v_{GS2}} = \mathbf{V_T}$$

Then:

$$\mathbf{v_{ID,sat}} = \sqrt{\frac{\mathbf{I_{BAIS}}}{\frac{\mathbf{W}}{2\mathbf{L}}\mu\mathbf{C_{ox}}}}$$

Large-signal response of differential amplifier (contd.)



- For small v_{ID}, v_O is ***linear*** in $v_I \Rightarrow$ differential amplifier
- For large v_{ID}, v_O ***saturates***: once v_{ID} is large enough, v_O independent of $v_{ID} \Rightarrow$ logic inverter

Can do logic with this:

- Logic 0 = $-V_{ID,sat}$, logic 1 = $V_{ID,sat}$
- Regenerative if V_O (swing) $> V_{ID,sat}$

- Used in some MOSFET logic styles
- Used with Si BJTs: ***Emitter-Coupled Logic (ECL)***
- And GaAs FETs: ***Source-Coupled FET Logic (SCFL)***

What did we learn today?

Summary of Key Concepts

- In differential amplifiers, signals are represented by ***difference*** between two voltages
- Differential amplifier amplifies the difference between two voltages but rejects “***common mode***” signals
  - ⇒ Improved noise immunity
- Using “***half-circuit***” technique, small-signal operation of differential amplifiers is analyzed by breaking the problem into two simpler ones
  - ***Differential mode*** problem
  - ***Common mode*** problem
- ***Common-mode rejection ratio*** (CMRR) is an important figure of merit for differential amplifiers
- Differential amplifiers require good device matching

Wrap-up of 6.012

6.012: Introductory subject to *microelectronic* devices and circuits

- MICROELECTRONIC DEVICES
  - Semiconductor physics: **electrons / holes and drift / diffusion**
  - Metal-oxide-semiconductor field-effect transistors (MOSFETs): **drift of carriers in inversion layer**
  - Bipolar junction transistors (BJTs): **minority carrier diffusion**
- MICROELECTRONIC CIRCUITS
  - Digital circuits (mainly CMOS): **no static power dissipation; power ↓, delay ↓ & density ↑ as W & L ↓**
  - Analog circuits (BJT and CMOS): **f_τ ↑ and g_m ↑ as L ↓: however, A_{vomax} ↓ as L ↓**

Follow-on Courses

- **6.152J** — Microelectronics Processing Technology
- **6.720J** — Integrated Microelectronic Devices
- **6.301** — Solid State Circuits
- **6.371** — Introduction to VLSI Systems
- **6.374** — Analysis and Design of Digital ICs
- **6.775** — Design of Analog MOS LSI