6.012 Electronic Devices and Circuits
Fall 1999

October 13, 1999
Quiz #1

-OPEN BOOK-

NAME SOLUTIONS

RECITATION TIME____________

Problem	#points
1	
2	
3	
Total	

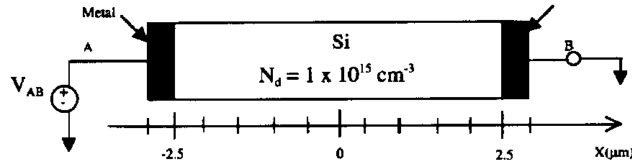
General guidelines (please read carefully before starting):

- Make sure to write your name on the space provided above.
- All answers should be given in the space provided. Please do not turn in any extra material. If you need more space, use the back page.
- You have 120 minutes to complete the quiz.
- Where required, make reasonable approximations and *state them.*
- Partial credit will be given for setting up problems without calculations. NO credit will be given for answers without reasons.
- Use the symbols utilized in class for the various physical parameters, i.e. N_d, n_o, etc.
- Every numerical answer must have the proper units next to it. Points will be subtracted for answers without units or with wrong units.
- Use the following fundamental constants and physical parameters for silicon at room temperature.

$n_i = 1.0 \times 10^{10} cm^{-3}$
$kT/q = 0.026V$
$q = 1.60 \times 10^{-19} C$
$\varepsilon_S = 1.04 \times 10^{-12} F/cm$
$\varepsilon_{OX} = 3.45 \times 10^{-13} F/cm$

Problem 1 – 35 Points

The n-type silicon sample illustrated below is 5 microns (μm) long and has metal ohmic contacts, A and B, on either end. The net donor concentration ~~is 1~~ 1 x 10^{15} cm^{-3}; the electron mobility, μ_n, is 1400 cm^2/V-s; and the hole mobility, μ_p, is 500 cm^2/V-s. The electrostatic potential of the metal relative to intrinsic silicon is 0.2V.



a) What are the thermal equilibrium hole and electron concentrations in this silicon? In thermal equilibrium V_{AB} is 0 V. Show your work and/or explain your answer.

$$n_o = N_D = 10^{15}$$

$$p_o = \frac{n_i^2}{n_o} = 10^5$$

n_o = 10^{15} cm^{-3}

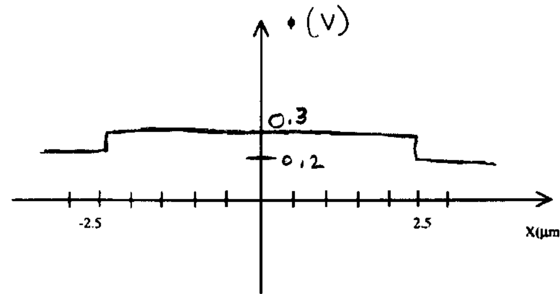
p_o = 10^5 cm^{-3}

b) What is the thermal equilibrium electrostatic potential, ϕ_n, of the silicon in this sample? Assume ϕ is zero in intrinsic silicon (our unusual convention). Show your work and/or explain your answer.

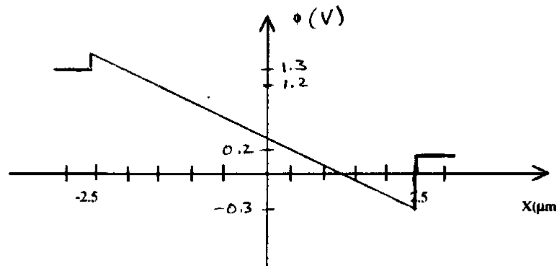
$$\phi_n = (60\ mV) \log_{10}\left(\frac{n_o}{n_i}\right) = 0.3 \text{ Volts}$$

ϕ_n = 0.3 Volts

c) On the axes provided below, sketch the electrostatic potential, $\phi(x)$, going from the metal on the left, through the silicon, and into the metal on the right, with $V_{AB} = 0$ V. Dimension your sketch and label any significant features.



d) On the axes provided below, sketch the electrostatic potential, $\phi(x)$, going from the metal on the left, through the silicon, and into the metal on the right, with $V_{AB} = 1$ V. Dimension your sketch and label any significant features, including $\phi(o)$.



e) When $V_{AB} = 1$ V, what are the electron and hole **drift** current densities, J_n^{dr} and J_p^{dr}, respectively, at x = 0 μm.

Constant E-field $\quad E = \frac{V}{L} = \frac{1}{5\times10^{-4}} = 2000\ V/cm$

$J_n^{dr} = q\mu_n n_o E = (1.6\times10^{-19})(1400)(10^{15})(2000)$

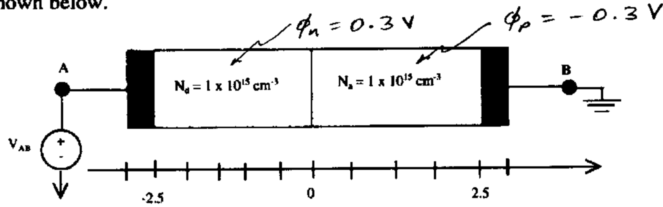
$J_p^{dr} = q\mu_p p_o E = (1.6\times10^{-19})(500)(10^{5})(2000)$

J_n^{dr} (0μm) = 448 A/cm²

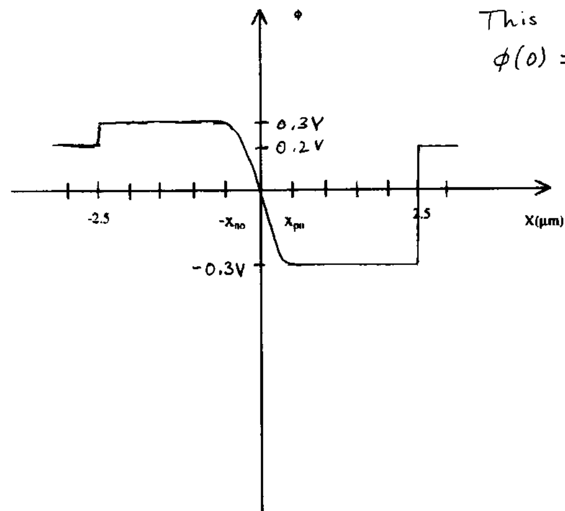
J_p^{dr} (0μm) = 1.6×10^{-8} A/cm²

Makes Sense! → Majority carrier drift current >> Minority carrier drift current.

Next, consider a sample similar to our original sample, except that it is doped p-type with a net acceptor concentration of 1×10^{15} cm^{-3} in the region from x = 0 μm to x = 2.5 μm as shown below.

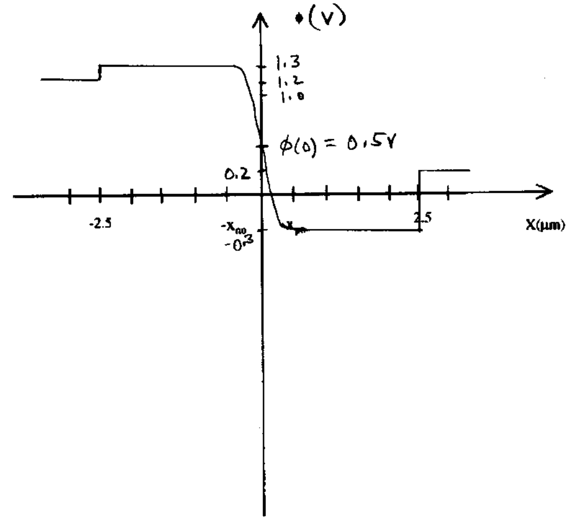


f) On the axes provided below, sketch the electrostatic potential, $\phi(x)$, going from the metal on the left, through the silicon, and into the metal on the right, with $V_{AB} = 0$ V. Dimension your sketch and label any significant features, including the shape of $\phi(x)$ in the depletion region and the value of $\phi(0)$. Use the $-x_{no}$ and x_{po} indicated on the horizontal axis. Do not calculate it.



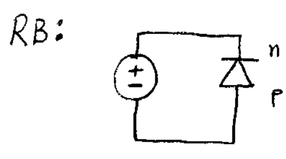
This is symetric
$\phi(0) = 0$ since $x_p = x_n$

g) On the axes provided below, sketch the electrostatic potential, $\phi(x)$, going from the metal on the left, through the silicon, and into the metal on the right, with $V_{AB} = 1$ V. Dimension your sketch and label any significant features, including the shape of $\phi(x)$ in the depletion region and the value of $\phi(o)$. Use the $-x_{no}$ and x_{po} indicated on the horizontal axis. You do not need to calculate the new depletion region edges. Just make the sketch relative to the equilibrium values shown.

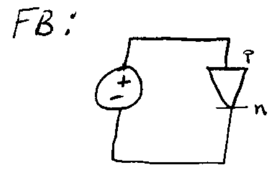


We are applying a reverse bias
⇒ Depletion region expands

RB:

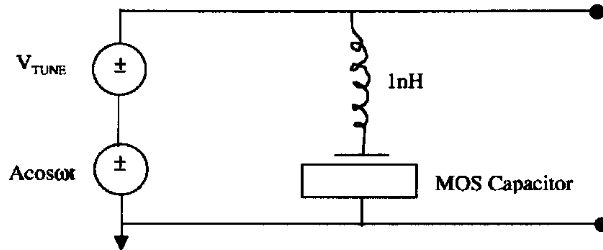


FB:



Problem 2 – 35 Points

You are given an LC tank circuit that uses an MOS capacitor. The MOS capacitor has $T_{ox} = 200$ Å, $N_a = 10^{16}$ cm^{-3}, has its N^+ polysilicon gate tied to the inductor and its substrate grounded. The DC voltage V_{TUNE} is applied to the gate of MOS capacitor through the inductor. This DC voltage can vary the capacitance value and corresponding resonant frequency. The small signal voltage source will be shunted to ground at the resonant frequency $\omega_c = 1/\sqrt{LC}$. The amplitude of the small signal source, A, is much less than V_{TUNE}.



a) Specify the range(s) of voltages, V_{TUNE}, at which the MOS capacitance is a maximum.

Max when in accumulation or inversion.

$V_{FB} = -(\phi_{n+} - \phi_p) = -(550 + 360)\,mV = -0.91\,V$

$V_{Tn} = V_{FB} - 2\phi_p + \frac{1}{C_{ox}}\sqrt{2q\epsilon_{si}N_a(-2\phi_p)} = -0.91 + 0.72 + 0.284$

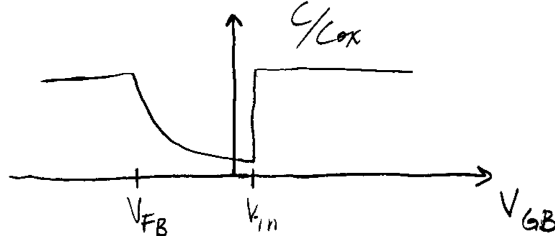
$V_{Tn} = 0.094\,V$

Cap is max @ $V_{Tune} > -0.0506V$ & $V_{Tune} < -0.91V$

b) Specify the voltage, V_{TUNE} at which the MOS capacitance is a minimum.

MOS Capacitance is minimum at

$V_{Tune} = V_{Tn} = -0.0506\,V$



c) Calculate the area of the MOS capacitor such that the minimum resonant frequency is 1Grad/s. ω_r is minimum when C is maximum

$$\omega_r = \frac{1}{\sqrt{LC_{max}}} = 1\times10^{9} \Rightarrow C_{max} = 1\,nF \qquad C_{ox} = \frac{\epsilon_{ox}}{t_{ox}} = 1.73\times10^{-7}\,F/cm^2$$

$$C_{max} = A \cdot C_{ox}$$

$$A = 5.79\times10^{-3}\,cm^2$$

d) Using the area calculated in (c), what is the maximum resonant frequency?

$$C(V_{GB} = V_{Tn}) = \frac{C_{ox}}{\sqrt{1 + \frac{2C_{ox}^2(V_{Tn} - V_{FB})}{q\epsilon_{Si} N_a}}} = 2.85\times10^{-8}\,F/cm^2$$

$$C_{min} = A \cdot C(V_{GB} = V_{Tn}) = 1.65\times10^{-10}\,F$$

$$\omega_{max} = \frac{1}{\sqrt{L\,C_{min}}} = 2.46\ Grad$$

e) In many applications, we need to have a large range of resonant frequencies. Circle how would you change the following parameters to maximize C_{MAX}/C_{MIN}.

$$\frac{C_{max}}{C_{min}} = \frac{C_{ox}}{\dfrac{C_{ox}}{\sqrt{1 + \frac{2C_{ox}^2(V_{Tn} - V_{FB})}{q\epsilon_{Si} N_a}}}} = \sqrt{1 + \frac{2C_{ox}^2(V_{Tn} - V_{FB})}{q\epsilon_{Si} N_a}}$$

T_{OX}:	Increase	**(Decrease)**	No Effect
N_a:	Increase	**(Decrease)**	No Effect
Area:	Increase	Decrease	**(No Effect)**

Problem 3 (30 Points)

Consider an n-channel MOSFET with $V_{BS}=0$. The oxide thickness is $t_{ox}=20$ nm and the substrate is doped at $N_A=10^{17}$ cm^{-3}. $\mu_n=400$ cm^2/Vs and W/L=10μm/2μm=5. The flatband voltage is given as $V_{FB}=60$ mV.

(a) Determine the doping type and the dopant concentration for the polysilicon gate.

$$V_{FB} = (\phi_{gate} - \phi_p) = -420\text{ mV} - \phi_{gate} = 60\text{mV}$$

$$\phi_{gate} = -480\text{ mV}$$

$$\text{p-type gate w/ } N_a = n_i e^{\frac{q\phi_{gate}}{kT}} = 10^{18}\text{ cm}^{-3}$$

Determine the oxide capacitance (C_{ox}),

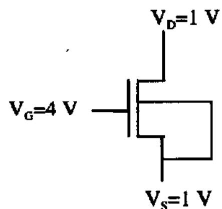
$$C_{ox} = \frac{\epsilon_{ox}}{t_{ox}} = 1.73 \times 10^{-7}\text{ F/cm}^2$$

and the threshold voltage (V_{Tn}).

$$V_{Tn} = V_{FB} - 2\phi_p + \frac{1}{C_{ox}}\sqrt{2q\epsilon_{si}N_a(-2\phi_p)} = 0.06 + 0.84 + 0.971$$

$$V_{Tn} = 1.87\text{ V}$$

(b) If the device is biased as shown below:



(i) what is the regime of operation for the gate capacitor (depletion, accumulation or inversion) ?

$$V_{GS} = 3V > V_{Tn} \longrightarrow \text{inversion}$$

(ii) Determine the mobile charge density under the gate.

$$Q_N = -C_{ox}\left(V_{GB} - V_{Tn}\right) = -(1.73\times10^{-7})(3 - 1.87)$$

$$Q_N = -1.954 \times 10^{-7}\ C/cm^2$$

(iii) Calculate I_D.

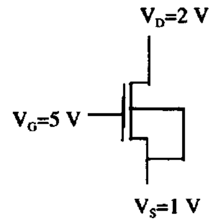
triode/linear operation region

For n-channel MOSFET

$$I_D = \begin{cases} \left(\frac{W}{L}\right)\mu_n C_{ox}\left[V_{GS} - V_{Tn} - \frac{V_{DS}}{2}\right]V_{DS} & \text{for } V_{GS} > V_{Tn},\ V_{DS} \leq V_{GS} - V_{Tn} \\ \frac{1}{2}\left(\frac{W}{L}\right)\mu_n C_{ox}\left[V_{GS} - V_{Tn}\right]^2 & \text{for } V_{GS} > V_{Tn},\ V_{DS} \end{cases}$$

$$V_{DS} = 0 \Rightarrow I_D = 0$$

(c) If the device is biased as shown below:



(i) what is the regime of operation for the MOSFET (cut-off, triode or saturation) ?

$V_{GS} = 4V > V_{Tn}$

$V_{DS} = 1V < V_{GS} - V_{Tn} = 2.13\ V$

$\Rightarrow$ triode region of operation

(ii) Calculate I_D.

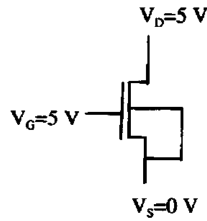
units: $[\ ]\left[\frac{cm^2}{V \cdot s}\right]\left[\frac{C}{V \cdot cm^2}\right][V][V] = [C/s] = [Amp]$

$$I_D = \left(\frac{W}{L}\right) \mu_n C_{ox} \left[V_{GS} - V_{Tn} - \frac{V_{DS}}{2}\right] V_{DS}$$

$$I_D = 5(400)(1.73 \times 10^{-7})\left[4 - 1.87 - \tfrac{1}{2}\right] 1$$

$$I_D = 0.564\ mA$$

(d) If the device is biased as shown below:



(i) what is the regime of operation for the MOSFET
(cut-off, triode or saturation) ?

$V_{GS} = 5V > V_{Tn}$

$V_{DS} = 5V > V_{GS} - V_{Tn} \Rightarrow$ Saturation

(ii) Calculate I_D.

$$I_D = \frac{1}{2}\left(\frac{W}{L}\right)\mu_n C_{ox}(V_{GS} - V_{Tn})^2 = 1.69\ mA.$$