May 20, 1999 - Final Exam

Name: ______________________________

Recitation: ______________________________

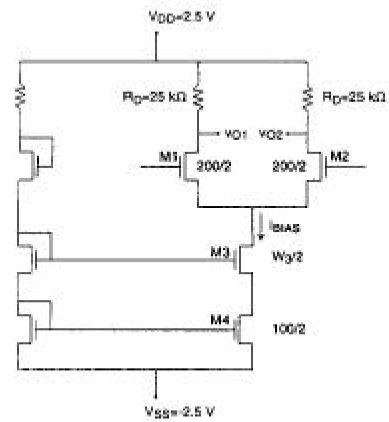
problem	grade
1	/25
2	/25
3	/20
4	/20
5	/10
total	/100

General guidelines (please read carefully before starting):

- Make sure to write your name on the space designated above.
- **Open book**: you can use any material you wish.
- All answers should be given in the space provided. Please do not turn in any extra material. If you need more space, use the back page.
- You have **180 minutes** to complete your quiz.
- Make reasonable approximations and *state them*, i.e. quasi-neutrality, depletion approximation, etc.
- Partial credit will be given for setting up problems without calculations. NO credit will be given for answers without reasons.
- Use the symbols utilized in class for the various physical parameters, i.e. μ_n, I_D, β_F, etc.
- Every numerical answer must have the proper units next to it. Points will be subtracted for answers without units or with wrong units.
- Use the following fundamental constants and physical parameters for silicon and silicon dioxide at room temperature:

$$n_i = 1 \times 10^{10}\ cm^{-3}$$
$$kT/q = 0.026\ V$$
$$q = 1.60 \times 10^{-19}\ C$$
$$\epsilon_s = 1.05 \times 10^{-12}\ F/cm$$
$$\epsilon_{ox} = 3.45 \times 10^{-13}\ F/cm$$

1. *(85 points)* Below is a differential amplifier with transistors with the following parameters: $V_T = 1.0\ V$, $\mu_n C_{ox} = 50\ \mu A/V^2$, and $\lambda_n = 0.05\ V^{-1}$ @ $L = 2\ \mu m$. All transistors are biased in the saturation regime of operation.



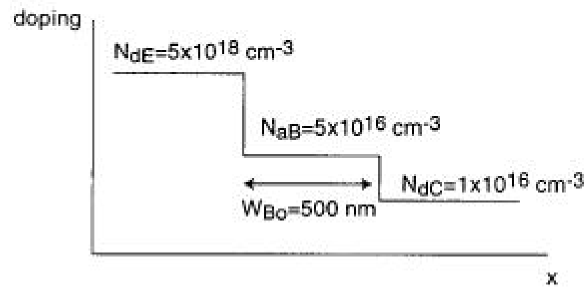
1a) *(5 points)* Choose I_{BIAS} such that $V_{O1} = V_{O2} = 0\ V$.

1b) *(5 points)* Calculate the small-signal differential mode gain, a_{dm}, of this amplifier.

1c) *(10 points)* Select the width of transistor **M3** so that the output resistance of the current source of the differential amplifier is $10^7\ \Omega$.

1d) *(5 points)* Calculate the common-mode rejection ratio.

2. *(25 points)* You find an npn bipolar transistor with the following doping profile:



The width of the metallurgical base (the entire extent of the p base) is $W_{Bo} = 500\ nm$. The emitter cross-sectional area is $A_E = 10\ \mu m^2$. This transistor is biased such that the collector current $I_C = 10\ mA$ and the base-collector voltage $V_{CB} = 5\ V$. The electron diffusion coefficient in the base is $D_n = 10\ cm^2/s$. Assume that the depletion width of the emitter-base junction is negligible.

2a) *(5 points)* Sketch the charge density and the electric field profile for the base-collector depletion region at this bias condition. Use the depletion approximation. What is the width of the quasi-neutral portion of the base $W_B = W_{Bo} - x_p$? Round off result to 0.1 nm.

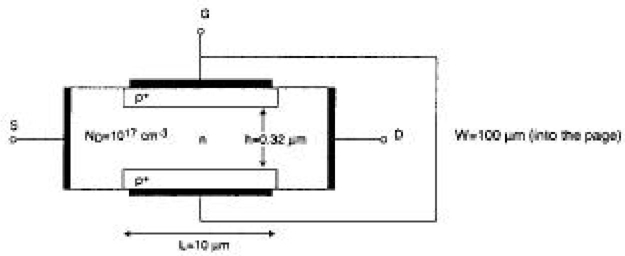
2b) *(5 points)* What is V_{BE} at this bias point?

2c) *(5 points)* What does $W_B = W_{Bo} - x_p$ become if V_{CB} increases to 5.5 V but V_{BE} is hold constant? What is the new value of I_C? Round off result to 10 μA.

2d) *(5 points)* From the result obtained in part c), estimate the output resistance r_o of this transistor at this bias point.

2e) *(5 points)* What is the small-signal voltage gain if the above transistor is used as a common-emitter amplifier driving a 100 Ω load? (Neglect the output resistance of the biasing current supply and assume that the resistance of the small-signal source is very small).

3. *(20 points)* The figure below sketches a Junction Field-Effect Transistor (JFET). This is a three-terminal device that consists of a n region (*channel*) surrounded by two p^+ regions (*gates*). The lateral resistance of the n region can be modulated by the voltage applied to the p^+ regions.

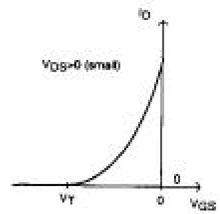


The electron mobility in the n-type channel is $750\ cm^2/V\cdot s$. For this problem, you will ignore the resistance associated with the n regions that are not surrounded by the p^+ regions.

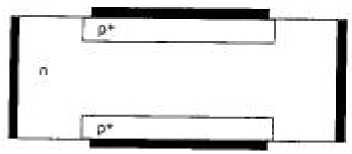
3a) *(3 points)* For $V_{GS} = V_{DS} = 0$, calculate the extent of each of the p^+-n junction depletion regions into the n-type channel.

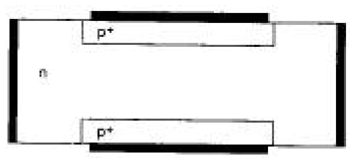
3b) *(3 points)* For $V_{GS} = V_{DS} = 0$, calculate the *channel resistance*, that is, the resistance of the 10 μm long n-type region in between the p^+ regions.

3c) *(4 points)* With $V_{DS} = 10\ mV$, we now apply $V_{GS} < 0$. We obtain the following I-V characteristics.



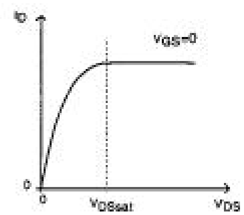
Explain this behavior. Qualitatively sketch the evolution of the depletion regions in the channel as a function of V_{GS} on the cross-sections provided below.



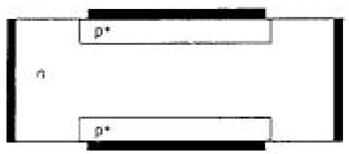


3d) *(3 points)* Calculate the value of $V_{GS} = V_T$ that results in $I_D = 0$. Numerical value expected.

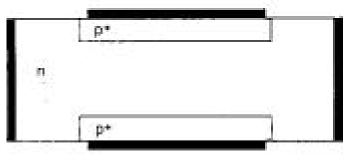
3e) *(4 points)* Keeping $V_{GS} = 0$, we now apply $V_{DS} > 0$. We obtain the following I-V characteristics.



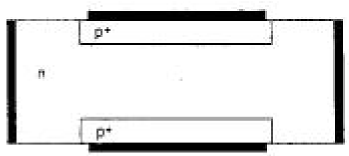
Explain this behavior. Sketch the evolution of the depletion region in the channel as a function of V_{DS} on the cross-sections provided below.



$V_{DS}=0$



$0<V_{DS}<V_{DS,sat}$



$V_{DS}=V_{DS,sat}$

3f) *(3 points)* Calculate the value of $V_{DS} = V_{DS,sat}$ that results in the saturation of I_D. Numerical value expected.

4. *(20 points)* You are given two bipolar transistors and two MOS transistors with their body tied up to the source. The collector and drain currents are set such that the devices have the following parameters:

BJT	MOSFET
$g_m = 5\ mS$	$g_m = 1\ mS$
$\beta_F = 100$	-
$r_o = 100\ k\Omega$	$r_o = 50\ k\Omega$

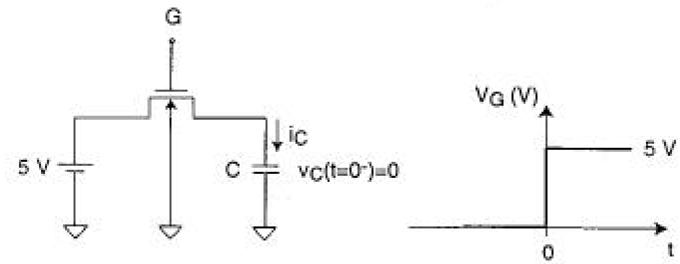
This problem is about designing a two-stage voltage amplifier with $R_S = 20\ k\Omega$ and $R_L = 1\ k\Omega$ using these transistors. Assume that $r_{oc} \to \infty$ for all required current sources.

4a) *(5 points)* In a first-pass design you use only MOSFETs. Choose the first and second stage type (CS, CG, or CD) to maximize the overall voltage gain for the amplifier (include R_S and R_L). Explain your answer.

4b) *(5 points)* In an improved design, you consider using BJT's too. Choose the first and second stage type (CS, CG, CD, CE, CB, or CC) to maximize the overall voltage gain for the amplifier (include R_S and R_L). Explain your answer.

4c) *(10 points)* Calculate the overall voltage gain for the amplifier designed in part b). Numerical value expected.

5. *(10 points)* Consider an NMOS pass transistor configuration as sketched below.



At $t = 0^-$, $V_G = 0\ V$, and the voltage across the capacitor $v_C(t = 0^-) = 0$. At $t = 0$, the gate voltage rises abruptly to $V_G = 5\ V$ and remains there. The transistor parameters are as follows: $L_g = 1\ \mu m$, $W_g = 2\ \mu m$, $\mu_n C_{ox} = 50\ \mu A/V^2$, $V_{To} = 1\ V$, $\gamma = 0.6\ V^{1/2}$, $\phi_p = -0.4\ V$.

5a) *(5 points)* Compute the current flowing into the capacitor at $t = 0^+$. Numerical answer expected.

5b) *(5 points)* Compute $v_C(t \to \infty)$. Numerical answer expected.