April 14, 1999 - Quiz #2

Name: _____

Recitation: _____

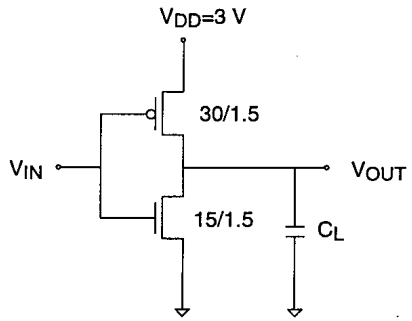
problem	grade
1	
2	
3	
total	

General guidelines (please read carefully before starting):

- Make sure to write your name on the space designated above.
- **Open book**: you can use any material you wish.
- All answers should be given in the space provided. Please do not turn in any extra material. If you need more space, use the back page.
- You have **120 minutes** to complete your quiz.
- Make reasonable approximations and *state them*, i.e. quasi-neutrality, depletion approximation, etc.
- Partial credit will be given for setting up problems without calculations. **NO** credit will be given for answers without reasons.
- Use the symbols utilized in class for the various physical parameters, i.e. μ_n, I_D, β_F, etc.
- Every numerical answer must have the proper units next to it. Points will be subtracted for answers without units or with wrong units.
- Use the following fundamental constants and physical parameters for silicon and silicon dioxide at room temperature:

$n_i = 1 \times 10^{10}\ cm^{-3}$
$kT/q = 0.026\ V$
$q = 1.60 \times 10^{-19}\ C$
$\epsilon_s = 1.05 \times 10^{-12}\ F/cm$
$\epsilon_{ox} = 3.45 \times 10^{-13}\ F/cm$

1. *(25 points)* Below is a CMOS inverter with the following device data: $t_{ox} = 15\ nm$, $\mu_n = 300\ cm^2/V \cdot s$, $\mu_p = 100\ cm^2/V \cdot s$, $V_{Tp} = -1\ V$, $\lambda_n = \lambda_p = 0\ V^{-1}$. The device dimensions are $W_p = 30\ \mu m$, $L_p = 1.5\ \mu m$, $W_n = 15\ \mu m$, $L_n = 1.5\ \mu m$.



1a) *(5 points)* Calculate V_{Tn} so that $V_M = 1.5\ V$.

Assume $V_{Tn} = 1\ V$ for parts 1b-1e.

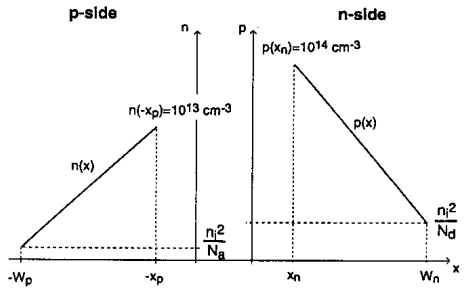
1b) *(5 points)* What is the maximum value for C_L and still have both t_{PLH} and t_{PHL} less than 1 ns? (Neglect C_{dB} for this calculation.)

1c) *(5 points)* A square wave signal from 0 to V_{DD} is applied to the input of this CMOS inverter with a frequency of 10 MHz. Calculate the power dissipated in the inverter. For this part, assume $C_L = 1\ pF$ and neglect any other parasitic capacitance.

1d) *(5 points)* What is the value of V_{DD} required to reduce the power dissipation in the inverter by a factor of 4?

1e) *(5 points)* If V_{DD} is reduced to 1.5 V, sketch the voltage transfer characteristics, V_{OUT} vs. V_{IN}, of the inverter.

2. *(40 points)* Below is a sketch *not to scale* of the minority carrier distribution across the quasi-neutral regions of a forward-biased p-n diode. For this diode, $W_p - x_p = 4\ \mu m$, $W_n - x_n = 3\ \mu m$, $D_n = 25\ cm^2/V \cdot s$, and $D_p = 10\ cm^2/V \cdot s$. The area of the junction is 10 μm^2.



2a) *(5 points)* Calculate the hole current injected into the n-side of the diode.

2b) *(5 points)* Calculate the electron current injected into the p-side of the diode.

2c) *(5 points)* Calculate the diffusion capacitance associated with carrier storage on the n-side of the diode.

2d) *(5 points)* Calculate the diffusion capacitance associated with carrier storage on the p-side of the diode.

2e) *(5 points)* How much should the voltage across the junction increase if we wish to double the total current through the diode?

2f) *(5 points)* If we increase the voltage in the manner suggested in the previous question, what happens to the total diffusion capacitance of the diode?

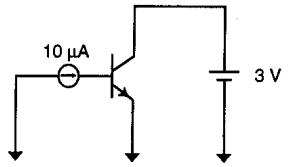
2g) *(5 points)* What is the ratio of the doping levels across the junction: N_a/N_d?

2h) *(5 points)* In what direction should N_a/N_d change if we wish to redesign the diode so as to get less diffusion capacitance at the same current level? (Assume that in redesigning the diode D_n, D_p, $W_n - x_n$, and $W_p - x_p$ do not change).

Choose one: N_a/N_d *must increase.* N_a/N_d *must decrease.* Explain (*no explanation, no points*).

3. *(35 points)* Consider a bipolar transistor with the following large-signal equivalent circuit model parameters $I_S = 10^{-16}$ A, $\beta_F = 100$, and $\beta_R = 1$. To answer some of the following questions, use the non-linear hybrid-π model of the transistor presented in class.

- Answer the following questions when the device is biased as sketched in the diagram below:

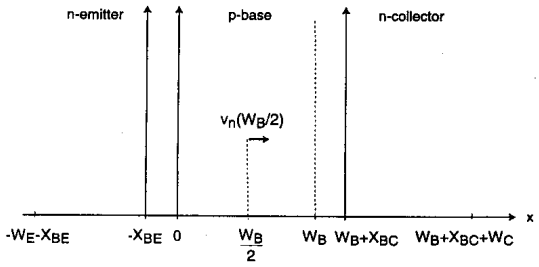


3a) *(5 points)* In what regime is the device operating? Explain.

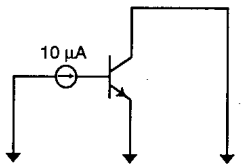
3b) *(5 points)* Calculate the collector current, I_C.

3c) *(5 points)* Calculate the base-emitter voltage V_{BE}.

3d) *(5 points)* If the doping level in the base is $N_{aB} = 10^{17}\ cm^{-3}$ and the area of the base-emitter junction is $A_E = 40\ \mu m^2$, calculate the electron velocity in the middle of the quasi-neutral base (see sketch below).



□ Answer the following questions when the device is biased as sketched in the diagram below:



3e) *(5 points)* In what regime is the device operating? Explain.

3f) *(5 points)* Calculate the base-emitter voltage V_{BE}.

3g) *(5 points)* Calculate the collector current, I_C.