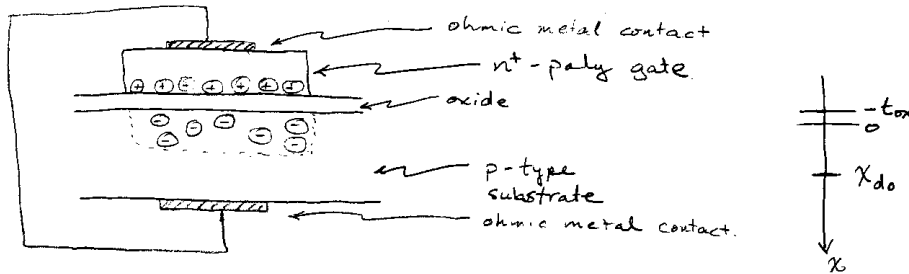


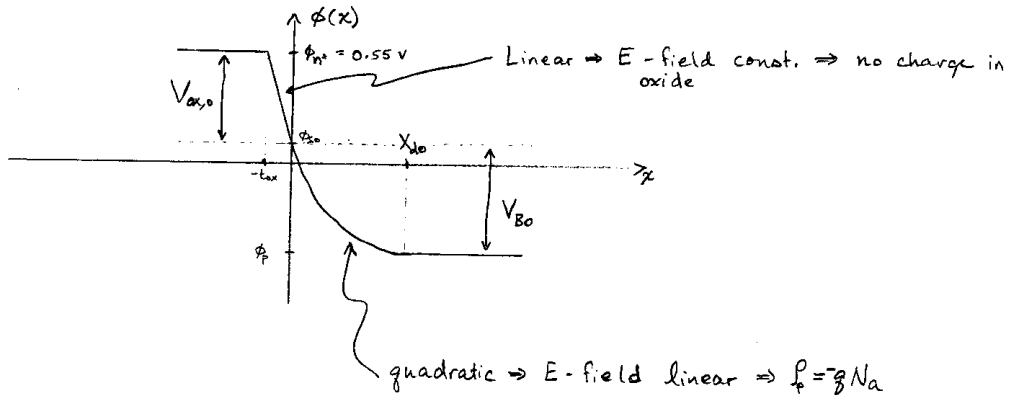
Tutorial #3 10/2/2000 & 10/3/2000

MOS Capacitor in thermal equilibrium:



What is happening in thermal equilibrium?

- $\phi_{n^+}$  poly is 0.55 volts.
- $\phi_p$  substrate has some potential that can be solved w/ GOMV rule.
- since  $\phi_{n^+} \neq \phi_p$ , there is a potential difference going from the poly to the substrate.
- This potential difference gives rise to E-field in the oxide and the depletion region of the p-substrate.
- Since there is an E-field, there must be non-zero charge densities.
- In the p-substrate, there is a portion depleted of mobile carriers (holes) near the Si-SiO<sub>2</sub> interface. There are  $N_a^-$  in this depletion region, giving rise to the negative charge there.
- The negative charge in the depletion region is matched by positive charged in the poly right at the poly-SiO<sub>2</sub> interface.
- The size of the depletion region in TE depends on the doping ( $N_a$ ) and the thickness of SiO<sub>2</sub>.



$$Q_{B0} = -Q_{G0} = -qNaX_{do}$$

$$V_{ox,0} + V_{B0} = \phi_{n+} - \phi_p$$

Boundary condition at oxide-Si interface:  $\epsilon_{ox} E_o(x=0^-) = \epsilon_{si} E_o(x=0^+)$

$$E_o(0^+) = \frac{-Q_{B0}}{\epsilon_{si}} = \frac{qNaX_{do}}{\epsilon_{si}} \quad E_{ox} = E_o(0^-) = \frac{qNaX_{do}}{\epsilon_{ox}}$$

$$E_o(x) = \frac{qNa(X_{do}-x)}{\epsilon_{si}} \quad \text{for } 0 \leq x \leq X_{do} \quad \leftarrow \text{valid for } -t_{ox} \leq x \leq 0$$

$$\phi_o(x) = \phi_{n+} - \frac{qNaX_{do}}{\epsilon_{ox}}(x+t_{ox}) \quad \text{for } -t_{ox} \leq x \leq 0$$

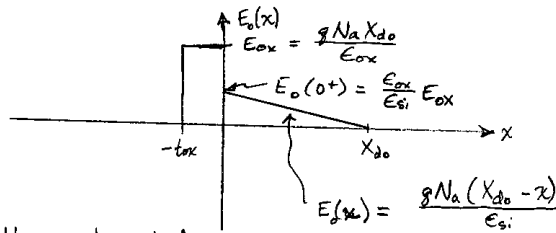
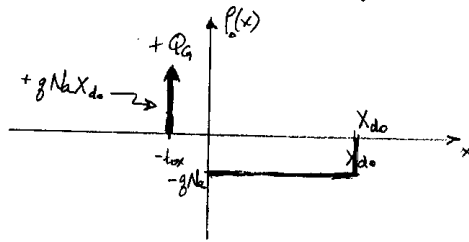
$$\phi_o(0) = \phi_{s0} = \phi_{n+} - qNaX_{do} \frac{t_{ox}}{\epsilon_{ox}} = \phi_{n+} - \frac{qNaX_{do}}{C_{ox}} \quad \text{where } C_{ox} = \frac{\epsilon_{ox}}{t_{ox}}$$

$$V_{ox,0} = \phi_{n+} - \phi_{s0} = \frac{qNaX_{do}}{C_{ox}} = \frac{Q_{G0}}{C_{ox}}$$

$$\phi_o(x) = \phi_{s0} - \frac{qNa}{\epsilon_{si}} \left( X_{do}x - \frac{x^2}{2} \right) \quad \text{for } 0 \leq x \leq X_{do}$$

$$\phi_o(X_{do}) = \phi_{s0} - \frac{qNaX_{do}^2}{2\epsilon_{si}} = \phi_p \Rightarrow \phi_{n+} - \phi_p = \frac{qNaX_{do}}{C_{ox}} + \frac{qNaX_{do}^2}{2\epsilon_{si}}$$

$$X_{do} = t_{ox} \left( \frac{\epsilon_{si}}{\epsilon_{ox}} \right) \left( \sqrt{1 + \frac{2C_{ox}^2(\phi_{n+} - \phi_p)}{q\epsilon_{si}Na}} - 1 \right)$$



Now apply voltage to gate:

Regions of MOS-C operation: (For p-type substrate)

- accumulation ( $V_{GB} < V_{FB}$ )
- depletion ( $V_{FB} < V_{GB} < V_T$ )
- inversion ( $V_T < V_{GB}$ )

Other conditions

- Flatband ( $V_{GB} = V_{FB}$ )
- Onset of Inversion ( $V_{GB} = V_T$ )

Flatband Condition when there is no E-field or charge through device.

$$V_{GB} = V_{FB} = -(\phi_{n+} - \phi_p)$$

When  $V_{GB} < V_{FB}$ : (Accumulation Region)

- gate is negatively charged.

- holes accumulate at SiO<sub>2</sub>-Si boundary.

$$\phi_s \approx \phi_p$$

When  $V_{FB} < V_{GB} < V_{Tn}$ : (Depletion Region)

- gate has positive charge.

- matched by immobile charge (Na<sup>-</sup>) in depletion region.

$$X_d(V_{GB}) = t_{ox} \left( \frac{\epsilon_{si}}{\epsilon_{ox}} \right) \left( \sqrt{1 + \frac{2C_{ox}^2 (V_{GB} - V_{FB})}{q\epsilon_{si}N_a}} - 1 \right)$$

$$\phi_s(V_{GB}) = (V_{GB} + \phi_{n+}) - \frac{qN_a X_d(V_{GB})}{C_{ox}}$$

Onset of inversion when  $X_d$  no longer grows with  $V_{GB}$  increase.

The positive charge on gate due to  $V_{GB}$  increase no longer matched by acceptor atoms in depletion region, but by electrons at the surface. This happens when  $\phi_s = -\phi_p$  ( $n_s = p_0$ ).

$$X_{d,max} = \sqrt{2 \frac{\epsilon_{si}}{qN_a} (-2\phi_p)}$$

$$V_B = \frac{qN_a}{2\epsilon_{si}} X_{d,max}^2 = -2\phi_p$$

$$Q_{B,max} = -qN_a X_{d,max} = -\sqrt{2\epsilon_{si}qN_a} (-2\phi_p)$$

$$V_{ox} = \frac{-Q_{B,max} t_{ox}}{\epsilon_{ox}} = \frac{1}{C_{ox}} \sqrt{2q\epsilon_{si}N_a} (-2\phi_p)$$

$$V_{GB} - V_{FB} = V_B + V_{ox}$$

At threshold,  $V_{GB} = V_{Tn}$

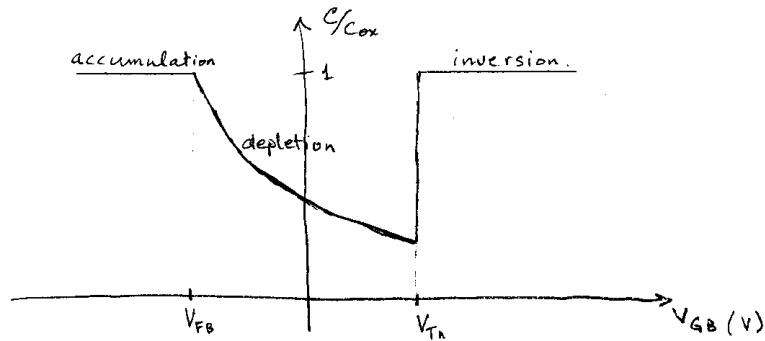
$$V_{Tn} - V_{FB} = V_B + V_{ox} \Rightarrow V_{Tn} = V_{FB} - 2\phi_p + \frac{1}{C_{ox}} \sqrt{2q\epsilon_{si}N_a} (-2\phi_p)$$

When  $V_{GB} > V_{Tn}$ : (Inversion Region)

$$Q_{in} = -C_{ox} (V_{GB} - V_{Tn})$$

↑ inversion charge.

Capacitance of MOS Structure:  
(P-type):



- For accumulation & inversion, the incremental charge is being added on either side of oxide.
- For depletion region, the incremental charge is added by growth of depletion region far from the oxide interface.