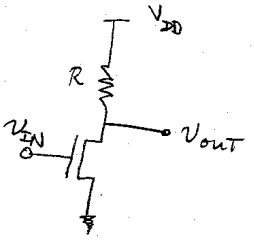
Tutorial Notes - tutorial #5 (10/22/2000 & 10/23/2000)

MOS Inverters

NMOS - Resistor pull-up:



$v_{OUT} = V_{DD} - I_D R$

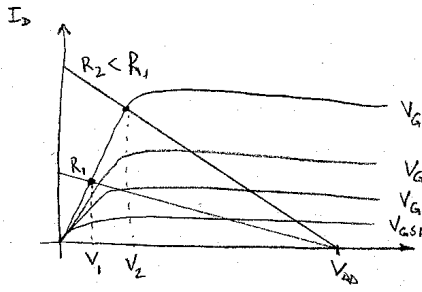
When $I_D = 0$ ($v_{IN} < V_{Tn}$)

$\Rightarrow v_{OUT} = V_{DD}$.

When $v_{IN} > V_{Tn}$, v_{OUT} is low.

How do we increase the noise margins?

- increase transconductance (increase current).
- increase R.



When $v_{IN} < V_{Tn}$

$v_{OUT}{}_{MAX} = V_{DD}$ for both R_s.

When $v_{IN} = v_{GS4}$,

$v_{OUT}{}_{MIN} = V_1$ for bigger load.

$v_{OUT}{}_{MIN} = V_2$ for smaller load.

Conclusion: Bigger load gives greater NM:

$NM_H = V_{OH} - V_{IH}$

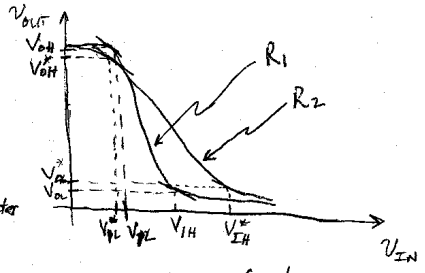
$NM_L = V_{IL} - V_{OL}$

$NM_{HR_1} = V_{OH} - V_{IH}$

$NM_{HR_2} = V_{OH}^* - V_{IH}^*$ ← This is greater

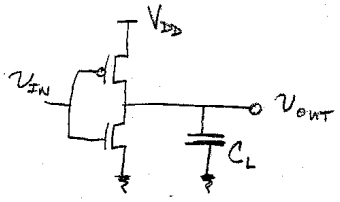
$NM_{LR_1} = V_{IL} - V_{OL}$ ← This is greater

$NM_{LR_2} = V_{IL}^* - V_{OL}^*$

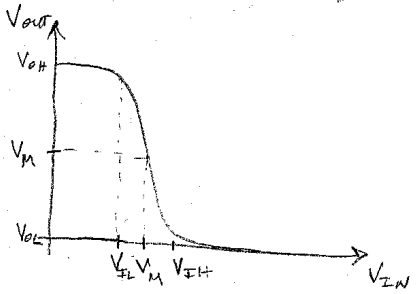


- Drawback of higher R ⇒ greater RC-time delay.
- Drawback of higher g_m ⇒ wider transistor = more capacitance.

A Better Way ⇒ CMOS - inverter:



- When v_{IN} low, NMOSFET in cut off ⇒ C_L charged up to V_{DD} w/ I_D flowing through PFET.
- When v_{IN} high, PFET in cut off ⇒ C_L discharged to 0 w/ I_D flowing through NFET.
- Power source (V_{DD}) has path to ground only for very short time during switching. This leads to higher noise margins, faster switching & lower power consumption.



What is V_M?

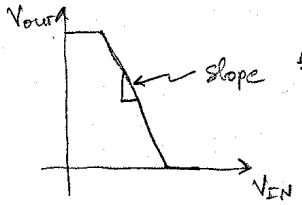
⇒ NFET & PFET both in saturation region when $V_{IN} = V_{OUT} = V_M$

$$I_{Dn} = \frac{1}{2} k_n (V_M - V_{Tn})^2 \quad \& \quad -I_{Dp} = \frac{1}{2} k_p (V_{DD} - V_M + V_{Tp})^2$$

Setting these equal to each other:

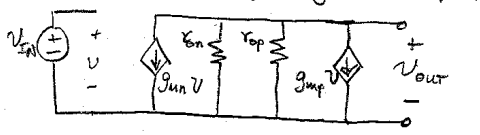
$$V_M = \frac{V_{Tn} + \sqrt{\frac{k_p}{k_n}} (V_{DD} + V_{Tp})}{1 + \sqrt{\frac{k_p}{k_n}}}$$

What is voltage gain?



$$\frac{\Delta V_{OUT}}{\Delta V_{IN}} = A_v$$

CMOS Low frequency small signal



$$g_{mn} = k_n (V_M - V_{Tn})$$

$$r_{on} = \frac{1}{\lambda_n I_{Dn}}$$

$$g_{mp} = k_p (V_{DD} - V_M + V_{Tp})$$

$$r_{oo} = \frac{1}{\lambda_p I_{Dp}}$$

CMOS - inverter

$$A_v = -(g_{mn} + g_{mp})(r_{on} \| r_{op})$$

$$V_{IL} = V_M + \frac{(V_{DD} - V_M)}{A_v} \quad \& \quad V_{IH} = V_M - \frac{V_M}{A_v}$$

$$NM_L = V_{IL} - V_{OL} = V_M + \frac{(V_{DD} - V_M)}{A_v}$$

$$NM_H = V_{OH} - V_{IH} = V_{DD} - V_M + \frac{V_M}{A_v}$$

Transient Analysis:

$t_{PHL} \Rightarrow$ time it takes from input transition from low to high to output transition from high to 50% of $(V_{OH} - V_{OL})$.

$t_{PLH} \Rightarrow$ time it takes from input transition from high to low to output transition from low to 50% of $(V_{OH} - V_{OL})$.

So, $t_{PHL} = \frac{C_L \Delta V}{I_D}$ ← total charge to be removed from load capacitance.
← rate at which the charge can be removed.

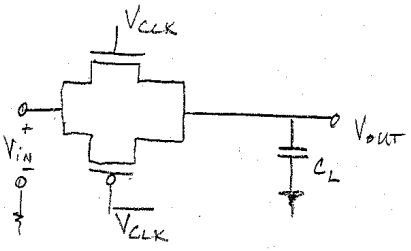
$$t_{PHL} = \frac{C_L \Delta V}{\frac{1}{2} k_n (V_{DD} - V_{Tn})^2} \quad \& \quad C_L = C_G + C_{DB} + C_{wire}$$

$$C_{DB} = W_n L_{diff_n} (C_{J_n}) + W_p L_{diff_p} (C_{J_p}) + (W_n + 2L_{diff_n}) C_{JSWn} + (W_p + 2L_{diff_p}) C_{JSWp}$$

$$C_G = \sum_{\substack{\text{load} \\ \text{inv.}}} C_{IN} \quad \text{where} \quad C_{IN} = C_{ox}(W \cdot L)_p + C_{ox}(W \cdot L)_n$$

C_{wire} is parasitic capacitance of wiring/connections.

Pass Gates



Average NFET Current for a low-to-high transition:

$$\overline{I_{DLHn}} = \frac{I_{DLHn}(V_{OUT} = 0\,V) + I_{DLHn}\left(V_{OUT} = \frac{V_{OH}}{2}\right)}{2}$$

$$= \frac{\frac{k_n}{2}(V_{DD} - V_{Ton})^2 + \frac{k_n}{2}\left(V_{DD} - \frac{V_{OH}}{2} - V_{Tn}\right)^2}{2}$$

Average PFET Current for same transition:

$$\overline{I_{DLHp}} = \frac{k_p}{2}(V_{DD} + V_{Top})^2$$

$$t_{PLH} = \frac{\left(C_{L_{LH}} \frac{V_{OH}}{2}\right)}{\left(\overline{I_{DLHn}} + \overline{I_{DLHp}}\right)}$$

$C_{LLH} = C_G + C_p + \frac{2}{3}(WL)_n C_{ox} + W_p C_{ox}$

- C_G, C_p: parasitics ($= C_{DB} + C_{wire}$).
- gate caps of load.
- $\frac{2}{3}(WL)_n C_{ox}$: NFET C_{gs} in saturation.
- $W_p C_{ox}$: PFET C_{dg} in saturation.

$$t_{PHL} = \frac{\left(C_{LHL} \frac{V_{OH}}{2}\right)}{\left(\overline{I_{DHLn}} + \overline{I_{DHLp}}\right)} \quad \& \quad \overline{I_{DHLp}} = \frac{\frac{k_p}{2}(V_{DD} + V_{Top})^2 + \frac{k_p}{2}\left(V_{DD} - \frac{V_{OH}}{2} + V_{Tp}\right)^2}{2}$$

$$\overline{I_{DHLn}} = \frac{k_n}{2}(V_{DD} - V_{Ton})^2$$

$$C_{LHL} = C_G + C_p + \frac{2}{3}(WL)_p C_{ox} + W_n C_{ox}$$