**Massachusetts Institute of Technology**
**Department of Electrical Engineering and Computer Science**
6.012 Electronic Devices and Circuits
Fall 1999

Design Problem #1 - Digital Circuits
10/20/1999
Due: 11/03/1999

## 0. Before You Begin

This project is to be done in groups of two or individually. Each group will submit one report.

Read section 13.5.3 of Howe & Sodini.

## 1. Introduction

The goal of this assignment is to design a digital circuit known as a “tri-state pad driver.” Its inputs are signals generated on-chip, and the output connects to external wiring and other chips. The circuit is illustrated below.

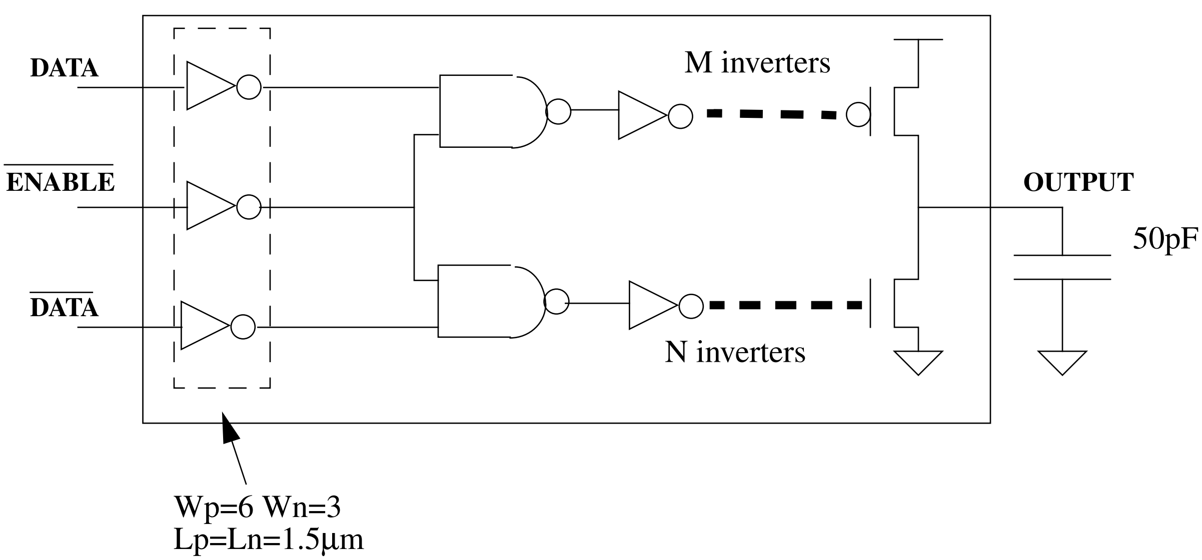


Figure 1: Circuit for Design Problem 1

When the /ENABLE signal is asserted (low), the tri-state driver will transmit the value of DATA to its output. When /ENABLE is deasserted, the output has high impedance, allowing other circuits to drive values onto the line. DATA and /DATA are complementary, in other words they always have opposite logical values. The following truth table provides a logical description of the tri-state driver:

**TABLE 1. Tri-state Inverter Truth Table**

| ENABLE | DATA | OUTPUT |
|---|---|---|
| 0 | 0 | Z (high impedance) |
| 0 | 1 | Z |
| 1 | 0 | 0 |
| 1 | 1 | 1 |

In addition to its logical function, the tri-state driver buffers the input signal. Its inputs can be driven by minimum-sized transistors, and its output can switch a 50pF load at the clock frequency.

## 2. Specifications

The chip has a clock rate of 50MHz (20ns cycle time) and uses a 3.0 volt power supply. The fabrication process has already been determined. Transistor specifications and SPICE models are given below. The minimum dimensions for transistors are W=3um and L=1.5um.

**TABLE 2. Transistor Parameters**

| NMOS | | PMOS | |
|---|---|---|---|
| $V_{t0n}$ | 0.7V | $V_{t0p}$ | -0.7V |
| $t_{ox}$ | 15nm | $t_{ox}$ | 15nm |
| $\lambda_{n,\ min}$ | $.067V^{-1}$ | $\lambda_{p,\ min}$ | $.067V^{-1}$ |
| $C_{jn}$ | $0.1fF/\mu m^2$ | $C_{jp}$ | $0.3fF/\mu m^2$ |
| Cjswn | $0.5fF/\mu m$ | Cjswp | $0.35fF/\mu m$ |
| $L_{diff,\ n}$ | $6\mu m$ | $L_{diff,\ p}$ | $6\mu m$ |
| $\mu_n C_{ox}$ | $50\mu A/V^2$ | $\mu_p C_{ox}$ | $25\mu A/V^2$ |

```
.MODEL N1 NMOS LEVEL=1 VTO=0.7 TOX=1.5E-08 KP=5E-05
+  LAMBDA=6.7E-02 CJ=1.0E-04 CJSW=5E-10 PB=0.8

.MODEL P1 PMOS LEVEL=1 VTO=-0.7 TOX=1.5E-08 KP=2.5E-05
+  LAMBDA=6.7E-02 CJ=3.0E-04 CJSW=3.5E-10 PB=0.8
```

These models are available from the 6.012 webpage, or in the 6.012 locker:
/afs/athena/course/6/6.012/www/design/design1.sp

Information specific to your circuit:

- Your circuit has three inputs: DATA, /DATA, and /ENABLE. DATA and /DATA are complementary signals, in other words they always have opposite logical values.
- You must buffer each input signal with a small inverter (Wp=6u, Wn=3u, L=1.5u). The inputs of these inverters are the only circuits you may connect to DATA, /DATA, and /ENABLE.
- Your circuit has one output node, OUTPUT. For simulation, connect a 50pf capacitor between OUTPUT and ground to model the wires and other circuits connected to the node.
- Your design consists of the following sub-parts:
    - Three inverters to buffer the inputs
    - 2-input NAND gate whose output drives the chain of M inverters.
    - a chain of M inverters connected in series
    - a large PMOS transistor that drives the output
    - 2-input NAND gate whose output drives the chain of N inverters.
    - a chain of N inverters connected in series
    - a large NMOS transistor that drives the output.

- The /ENABLE signal is used to activate/deactivate the entire chip, and changes infrequently. You need to show that your circuit performs the correct logical function with respect to /ENABLE, but you do not need to characterize the timing of your circuit when /ENABLE switches.
- The waveforms below illustrate the inputs, outputs, and timing specifications for your circuit. When /ENABLE is high the circuit is inactive. When /ENABLE is low, the value of OUTPUT should follow the value of DATA.

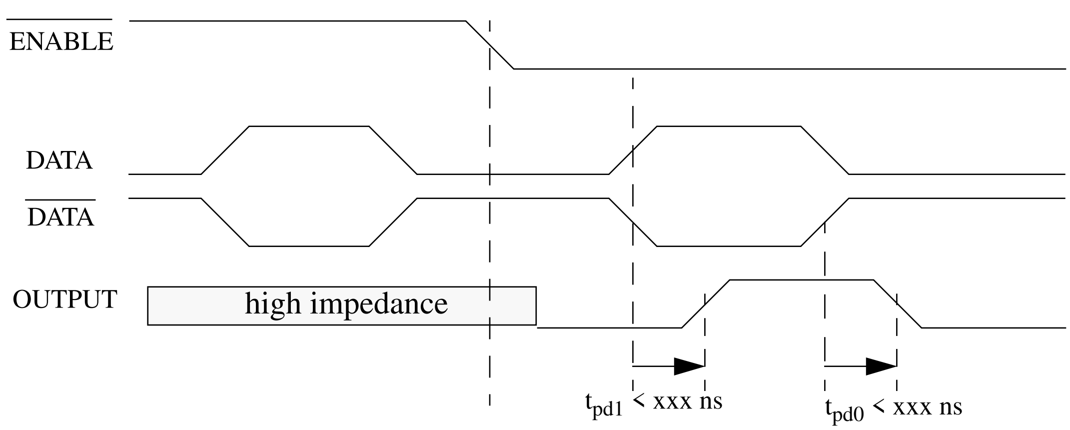


Figure 2: Input and Output waveforms and timing requirements

## 3. Design Objectives

The design goals in order of importance are: (1) to perform the correct logical function, (2) to meet timing constraints, and (3) to minimize power dissipation.

- The delay between DATA inputs changing and OUTPUT reaching the 50% point of its final value must be less than 7.0 ns ( $t_{pd1}$ and $t_{pd0} < 7.0$ns).
- OUTPUT rise and fall times (10%-90%) must be less than 2.5ns.
- All logic gates within your circuit must have noise margins of at least 1.0v. The final stage consisting of the large NMOS and PMOS transistors is excluded.
- DATA, /DATA, and /ENABLE must each be connected to a small inverter (Wp=6u, Wn=3u, Lp=Ln=1.5u). No other circuits can be connected to the inputs.
- Your circuit model and simulation results must reflect the effects of parasitic capacitances. You need to provide SPICE with information that allows it to calculate parasitic capacitances, as described in the following section.
- Average power dissipation when the standard input waveforms are applied must be less than 0.01 watts.

## 4. Preliminary Design and Calculations

This section describes simple models for gate, drain, and source capacitances. Estimating these capacitances requires understanding the layout of the transistor including the areas that the source and drain occupy.

m1 - NMOS

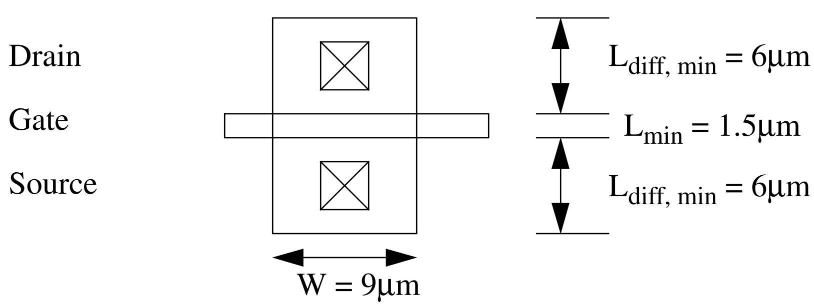


Figure 3: Transistor layout

Gate capacitance is dominated by the capacitance between the gate and the channel. As the gate voltage changes from HIGH to LOW, the transistor goes through all three regions of operations and exact computation of gate capacitance is difficult. For hand calculations, use the worst-case value of $C_g$ (fF)= $C_{ox}$ (fF/µm$^2$) * W (µm) * L (µm).

Drain and source capacitances arise from the pn-junctions between the source/drain regions and the substrate. This junction should always be reverse-biased, so we only need to worry about depletion capacitance. In a modern IC process, the properties of the junction between the bottom of the drain/source area and the substrate is considerably different from the junction around its perimeter. For this reason, SPICE has two capacitance parameters, CJ and CJSW. $C_j$ is the pn-junction capacitance per unit area of the bottom of the source or drain region (units = F/m$^2$). $C_{jsw}$ is the capacitance of the "sidewall," or perimeter, of the drain or source region (units = F/m). For hand-calculation, assume that these capacitances are linear and independent of bias voltage.

You must hand calculate the parasitic drain-substrate and source-substrate capacitances for each transistor, as they have a significant effect on the speed of, and power consumed by, your circuit. As an example, we will find the source and drain capacitances for the transistor illustrated above.

> The outside perimeter of the drain is W + 2*$L_{diff,\ min}$ = 6+9+6μm = 21μm. Note that the gate side of the drain is not included. The drain area is W*Ldiff, min = 9*6μm = 54μm$^2$=54*10$^{-12}$m$^2$ The perimeter and area of the source are identical to those of the drain.
>
> The SPICE model for this transistor is:

```
m1 1 2 3 4 N1 L=1.5u W=9u pd=21u ps=21u ad=54p as=54p
```

> For the drain, 21μm * $C_{jsw}$ + 54μm$^2$ * $C_j$ = 10.5 + 5.5 fF = 16fF. The source has the same dimensions, thus the same capacitance.

## 5. HSPICE Simulation

You will need to do two different kinds of simulations: DC sweeps and transients. The DC sweep is used to find the transfer functions of various stages. The easiest way to run DC sweeps is to create an HSPICE deck that contains transistor models, the sub-circuit under test, and simulation commands. Awaves can plot the input voltage on the x-axis, and the output voltage on the y-axis.

Use a transient simulation to measure propagation delays, as shown in Figure 2. The delay times for CMOS logic circuits are defined as the the period from one signal crossing $V_{DD}$/2 to a second signal crossing $V_{DD}$/2.

We have created a set of standard input waveforms that you will use to measure power dissipation. They are similar to the ones drawn in Figure 2. Look at the 6.012 webpage or Athena locker for the waveforms and instructions. HSPICE has a convenient command to measure the average power dissipation of a circuit during a specified time interval.

```
.measure tran pdiss avg power from=0n to=100n
```

This command will cause a line like the one below to appear in the HSPICE output file:

```
pdiss = 9.6116E-03 from= 0.0000E-00 to= 1.000E-07
```

## 6. Report

Your group will write a report detailing your design efforts. Be clear and concise. The following must be included in the report:

1. An explanation of the approach you took to arrive at the design, in one page or less. What steps did you take to create the correct logical function, meet timing requirements, and minimize power dissipation? This section is very important.
2. A transistor-level schematic diagram that shows transistor sizes (W and L), and how they are connected.
3. Summarize your hand calculations. Show how you arrived at your values of M and N, and the size of each transistor. Show approximate calculations for the expected propagation delays $t_{pd0}$ and $t_{pd1}$, and for power dissipation for the standard input waveforms. What part(s) of the circuit dissipate the most power?
4. Fill in the summary form with the appropriate hand-calculated and simulated values for your circuit.
5. Identify the logic gate with the smallest noise margin (either $V_{NMH}$ or $V_{NML}$). Mark this gate on your schematic diagram. Submit a plot from Awaves of its DC voltage transfer curve. If multiple gates have the smallest noise margin, for example two identical inverters, identify all of them but submit only one plot.
6. Include waveform plots from Awaves that clearly illustrate:
   - correct logical function
   - the propagation delays from DATA to OUTPUT
   - the voltages at the gate terminals of the final stage NMOS and PMOS transistors.
7. Put your HSPICE file(s) in a publicly readable directory in your Athena account, so that we may copy them and run our own simulations of your circuit. Your "Public" directory is a good location. Write your username, the directory, and the filename in the space on the summary page.

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Name(s): ________________________________________

Athena username(s): ________________________________________

HSPICE input filename(s): ________________________________________

| SPECIFICATION | YOUR DESIGN |
|---|---|
| M (number of inverters) | |
| N (number of inverters) | |

| PARAMETER | SPECIFICATION | YOUR CALCULATED VALUE | YOUR SIMULATED VALUE |
|---|---|---|---|
| OUTPUT $t_r$ | <2.5ns | | |
| OUTPUT $t_f$ | <2.5ns | | |
| tpd0 | < 7.0 ns | | |
| tpd1 | < 7.0 ns | | |
| Avg. power dissipation for standard inputs (100ns) | < 0.01 watt | | |
| Minimum noise margin | > 1.0 volt | | |