Massachusetts Institute of Technology
Department of Electrical Engineering and Computer Science
6.012 Electronic Devices and Circuits
Fall 1999

ADDENDUM TO DESIGN PROBLEM #1

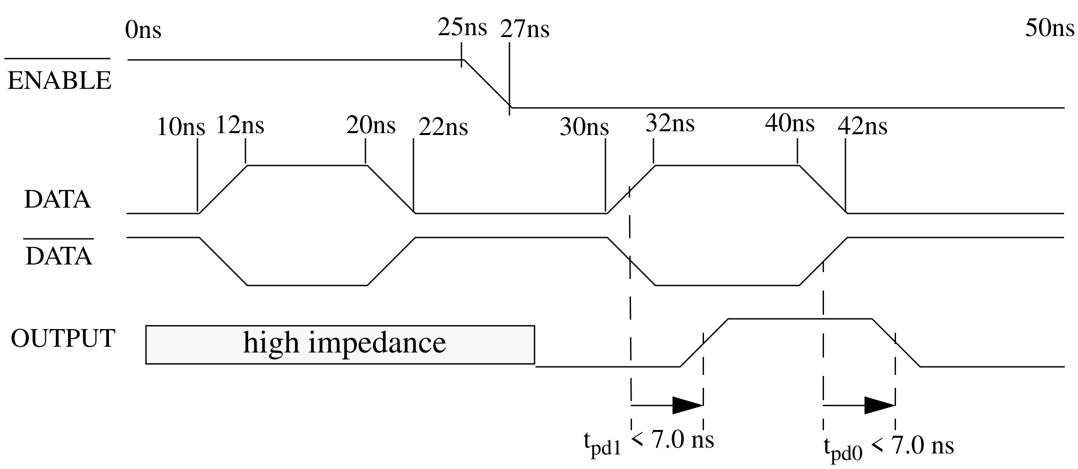
Issued 10/26/1999

We have made some changes and corrections to Design Problem #1.

1. Once you have a circuit that does the correct logical function and meets timing specifications, your objective is to **minimize power dissipation**. There is no specification for power dissipation - so the lower the better.
2. Calculate and simulate the average power dissipation for the input waveforms given below. In HSPICE you should run a transient analysis for 50ns with these input waveforms.
3. You do not need to hand-calculate t_r and t_f for OUTPUT.
4. Please use the corrected summary sheet (last page of this handout) instead of the one from the original handout.
5. In Figure 1, /DATA and DATA are reversed. /DATA should connect to the top inverter, DATA to the bottom inverter.
6. Table 1 is incorrect. The correct truth table is:

TABLE 1. Tri-state Driver Truth Table

/ENABLE	DATA	OUTPUT
0	0	0
0	1	1
1	0	Z (high impedance)
1	1	Z



Standard input waveforms, and expected waveform for OUTPUT.

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Design Problem #1 - Digital Circuits

Name(s): ______________________________

Athena username(s): ______________________________

HSPICE input filename(s): ______________________________

SPECIFICATION	YOUR DESIGN
M (number of inverters)	
N (number of inverters)	

PARAMETER	SPECIFICATION	YOUR CALCULATED VALUE	YOUR SIMULATED VALUE
OUTPUT t_r	<2.5ns		
OUTPUT t_f	<2.5ns		
tpd0	< 7.0 ns		
tpd1	< 7.0 ns		
Avg. power dissipation for standard inputs (50ns)	MINIMIZE		
Minimum noise margin	> 1.0 volt		