Massachusetts Institute of Technology
Department of Electrical Engineering and Computer Science
6.012 Electronic Devices and Circuits
Fall 1999

Design Problem #2 - Amplifiers
Distributed on: 11/23/99
Due on: 12/03/99

1.0 Introduction

In this design project, you will design a two-stage amplifier consisting of a common source and a common drain. Figure 1 shows a schematic diagram of the circuit. Transistor Mn1 is the common source and transistor Mn2 is the common drain. Transistors Mp1 and Mn3 supply current to transistors Mn1 and Mn2 respectively. V_{BIAS} is set such that the amplifier will operate in its high-gain region and v_s is a small-signal voltage source with resistance R_s.

Your job will be to size the four transistors (W/L) and set values for V_A, V_B and V_{BIAS} to meet gain, bandwidth and output voltage swing requirements while minimizing the power dissipation.

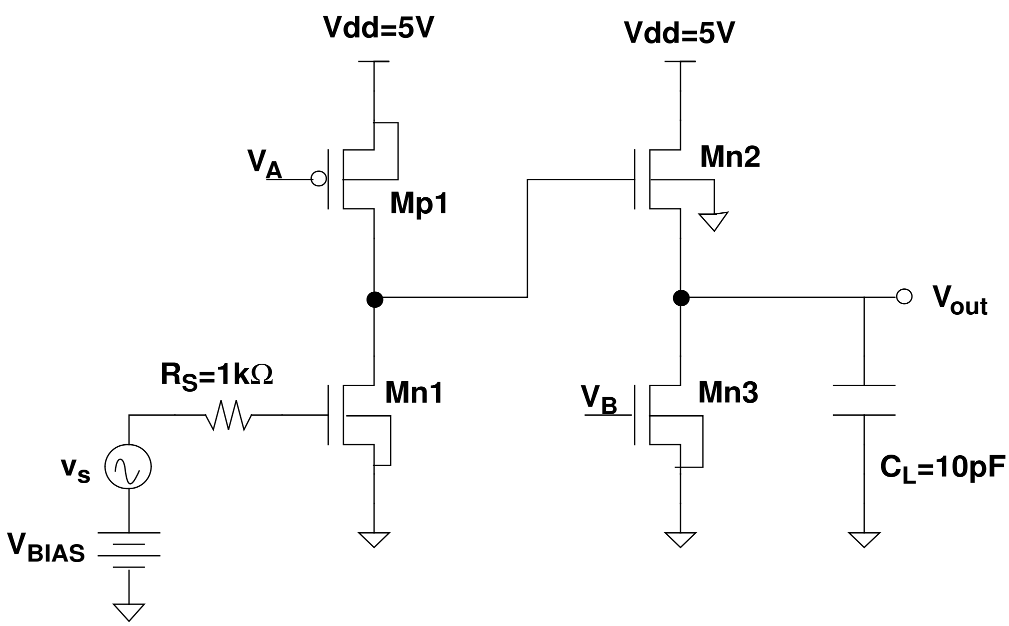

Figure 1. Schematic Diagram of Two-stage Amplifier

2.0 Design Objectives

Your design must meet the following specifications:

1. Overall gain, $|A_v| = v_{out}/v_s > 75$.
2. There are two requirements for the bandwidth (please refer to figure 2):
   a. The location of the first pole (f_{3db}) > 2 MHz
   b. The unity-gain frequency (f_{UNITY}) > 50 MHz
3. The output voltage must be able to swing 2 $V_{peak\text{-}to\text{-}peak}$ (i.e. V_{outmax}-V_{outmin} > 2.0 V) (please see figure 3).
4. The total power dissipation must be minimized.

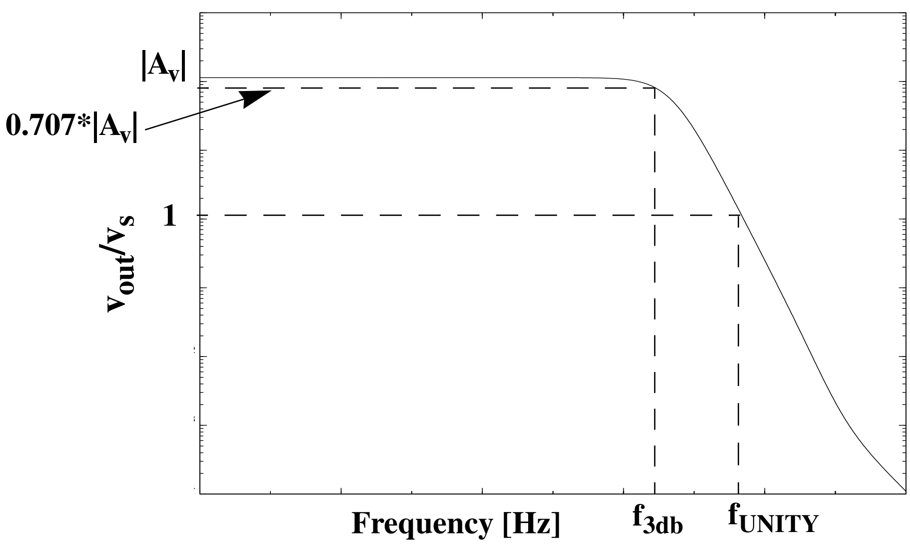

Figure 2. Frequency Response

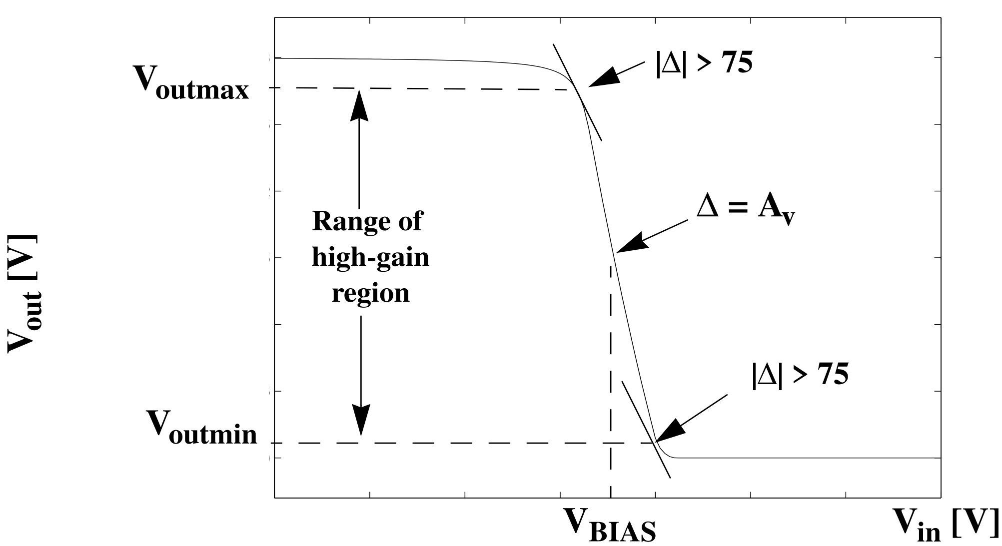

Figure 3. Voltage Transfer Characteristic

3.0 HSPICE models

The device parameters that you will be using are described in table 1. You will design your circuit in a process with a minimum gate length of 1.5 µm and a minimum width of 6 µm. Note that some of these values are different from those given to you in design problem 1.

	NMOS	PMOS
μC_{ox}	50 µA/V^2	25 µA/V^2
V_T	0.7 V	0.7 V
C_{ox}	2 fF/µm^2	2 fF/µm^2
C_{ov}	0.5 fF/µm	0.5 fF/µm
C_{jo}	0.1 fF/µm^2	0.3 fF/µm^2
C_{jsw}	0.5 fF/µm	0.35 fF/µm
Wmin	6 µm	6 µm
Lmin	1.5 µm	1.5 µm
Ldiff	6 µm	6 µm
λ	(0.1 µm/L) V^{-1}	(0.1 µm/L) V^{-1}

TABLE 1. Device Parameters

Also keep in mind that λ depends on the channel length, L. So, you will need to have a different model for each transistor with a different length. The models shown below are for a transistor with length L=1.5 µm.

```
.MODEL N1 NMOS LEVEL=1 VTO=0.7 TOX=1.5E-08 UO=220
+LAMBDA=6.7E-02 GAMMA=0.6 CGSO=1E-9 CGDO=1E-9 CJ=1.0E-04
+CJSW=5.0E-10 PB=0.95

.MODEL P1 PMOS LEVEL=1 VTO=-0.7 TOX=1.5E-08 UO=110
+LAMBDA=6.7E-02 GAMMA=0.6 CGSO=1E-9 CGD0=1E-9 CJ=3.0E-04
+CJSW=3.5E-10 PB=0.9
```

4.0 HSPICE Analysis

4.1 Operating Point

Before attempting an AC simulation on HSPICE, you will need to do a DC sweep on the input voltage to find the exact value for V_{BIAS} such that the circuit is operating in its high-gain region.

The range of V_{BIAS} is usually very small for high gain circuits, so you will need to take very small steps in order to increase the accuracy.

```
vin 1 0 ac=1,0 dc=0.5
.dc vin 0 5 0.001
```

The first line describes a voltage source between nodes 1 and 0 with a small signal source of magnitude 1 and phase 0. The second line tells HSPICE to sweep vin from 0 to 5V with 1 mV steps. The dc and ac values are arbitrary when doing a dc sweep. Figure 3 shows a sample transfer characteristic and how you can find the value for V_{BIAS}. You can also determine the voltage swing from this graph by measuring the range of output values for which the circuit will have the specified gain. You will need to repeat this procedure each time you change your design.

4.2 Gain and Bandwidth

To find the gain and bandwidth of your circuit, you will need to run an ac simulation using the following command.

```
vin 1 0 ac=1,0 dc=0.839 <--- Measured value from previous section
.ac vin dec 40 1 1g
```

The second line tells HSPICE to do an ac simulation and display the results on a log scale collecting 40 points per decade from 1 Hz to 1 GHz. Figure 2 shows a sample frequency response for the circuit. To measure the DC (low frequency) gain, use the Measure tool on awaves. To find the f_{3db} point, measure the frequency where the gain equals the DC gain multiplied by a factor of 0.707. The unity gain frequency, f_{UNITY}, can be found similarly, by measuring the frequency at the point where the gain equals 1.

****TIP**: To change the axis from a linear to a logarithmic scale, place the cursor on the axis and click on the right mouse button.

4.3 Current and Power Measurements

In analog circuits, the power dissipation is completely static and can be measured by taking the product of the supply voltage, Vdd, and the sum of the currents running through each leg of the circuit. For instance, if I'm running 1mA through Mn1 and 1mA through Mn2, the total power dissipation would be: (1mA+1mA)*5V=10 mW. Fortunately, HSPICE measures the static power without any special commands, so you can just read it off the output file where it is given as "total voltage source power dissipation." To find the current through each leg, you will need to add the following line to your input file:

```
.op
```

HSPICE will determine the operating point for each transistor and list all the small-signal parameters in the output file. It is here that you can determine the current running through each transistor.

5.0 Report

You will need to write a report explaining your design. Clarity and conciseness count. Your report should be divided into the following sections:

5.1 Design Summary (1 page)

This section summarizes your design (transistor sizes and currents) as well as the results from hand-calculations and HSPICE simulations. Use the last page of this handout for this purpose.

5.2 Approach (1 page max)

Explain the steps you took to arrive at your final design. Also, discuss any tradeoffs you found between the required specifications (i.e. increasing the gain lowered the bandwidth) as well as how your choice of transistor sizes and bias currents affected the latter (i.e. increasing W/L of transistor MN1 increased g_m and therefore the overall gain).

5.3 Circuit Schematic (1 page)

Draw a schematic diagram of your circuit neatly labeling the transistor names, currents, sizes and node names. (Please keep the same name convention for the transistors as shown in figure1).

5.4 Hand Calculations (4 pages max)

In three pages, summarize your hand calculations for the gain, f_{3db}, f_{UNITY}, output swing and power. Include a diagram of the small-signal model for the entire circuit. If you decide to use Matlab, Excel, or any other number-crunching software for this purpose, please explain the formulas you used and write down the final values. Any code or output from software other than HSPICE will not be read nor be considered as part of your report.

5.5 HSPICE input files (1 page max)

Include the HSPICE input file you used to verify your final design. In addition, please place them in your Public directory on athena.

5.6 HSPICE Output Plots (2 pages max)

Include HSPICE output plots similar to the ones shown in figures 2 and 3. Clearly label the values for V_{BIAS}, gain, f_{3db}, f_{UNITY} and output swing.

6.0 A Note on Grading

Approximately 10% of your grade for this project will depend on how your power dissipation compares with that of your peers. The remaining 90% will focus on the other specificiations and the quality of your report.

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Due Date: December 3, 1999
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Name(s): ______________________________

Athena username(s): ______________________________

HSPICE input filename(s): ______________________________

Parameter	**Value**	**Parameter**	**Value**
$(W/L)_{MN1}$		V_A	
$(W/L)_{MP1}$		V_B	
$(W/L)_{MN2}$		I(MN1)	
$(W/L)_{MN3}$		I(MN2)	

PARAMETER	**SPECIFICATION**	**CALCULATED VALUE**	**SIMULATED VALUE**
$\|Av\|$	> 75		
f_{3db}	> 2 MHz		
f_{UNITY}	> 50 MHz		
Output Swing	> 2 Vp-p		
Power Dissipation	MINIMIZE		