Massachusetts Institute of Technology
Department of Electrical Engineering and Computer Science

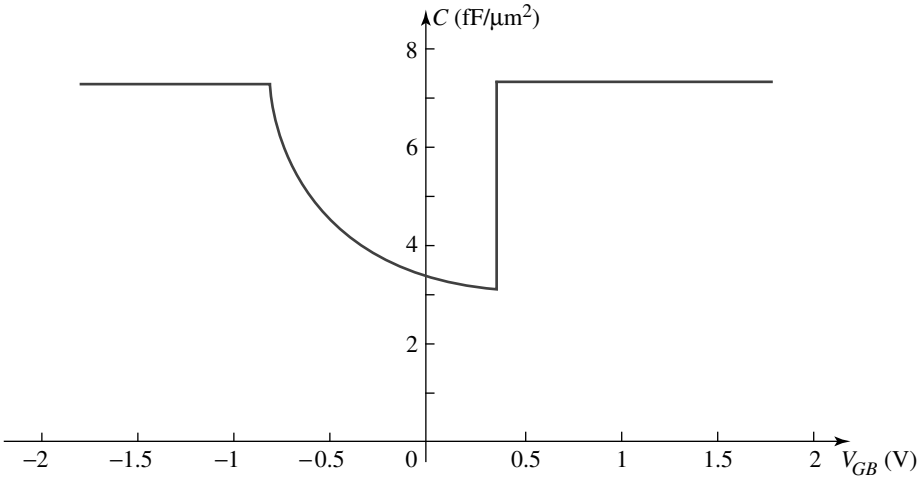
6.012
Microelectronic Devices and Circuits
Fall 1999

October 1, 1999- Homework #4
Due – October 8, 1999

Reading: Chapter 3.8 - 3.9 and 4.1 - 4.5

Problem 1 The capacitance-voltage curve for an MOS capacitor with a n^+ polysilicon gate is shown below.

a) What is the flatband voltage V_{FB}?
b) What is the threshold voltage V_T?
c) What is the gate oxide thickness?
d) What is the substrate type?
e) What is the substrate doping concentration?



Problem 2 Given an MOS capacitor with an p+ polysilicon gate, a 15 nm gate oxide, and a p-type substrate with a doping concentration of 5×10^{16} cm^{-3}

a) What is the gate-to-bulk voltage, if the gate charge is $Q_G = 5\text{x}10^{-6}$ C/ cm^2 ?
b) Sketch the charge density through the MOS capacitor with $Q_G = 5\text{x}10^{-6}$ C/ cm^2.
c) Sketch the electric field through the MOS capacitor with $Q_G = 5\text{x}10^{-6}$ C/ cm^2.
d) Sketch the potential through the MOS capacitor with $Q_G = 5\text{x}10^{-6}$ C/ cm^2.
e) What is the value of the gate charge to have the surface concentration of holes equal to 5×10^{16} cm^{-3} ?
f) What is the value of the gate charge to have the surface concentration of electrons equal to 5×10^{16} cm^{-3} ?
g) Sketch the charge density, electric field and potential through the MOS capacitor using the value for gate charge calculated in (f).

Problem 3 The control of the threshold voltage is critical for VLSI CMOS processes. In this problem we explore the implications for the control of gate oxide thickness. We would like the threshold voltage to be V_{Tn} = 500 mV ± 50 mV in a process that uses a p-type substrate doped at $N_a = 5 \times 10^{16}$ cm^{-3}.

a) Find the required average oxide thickness such that the average V_{Tn} = 500 mV.
b) Assuming that the substrate doping is $N_a = 5 \times 10^{16}$ cm^{-3} and is perfectly controlled, what is the allowable variation in the gate oxide thickness?
c) Now consider that Na = $5 \times 10^{16} \pm 1 \times 10^{15}$ cm^{-3}. What are the highest and lowest threshold voltages? Use the average oxide thickness calculated in (a).

Problem 4 In a particular CMOS technology n+ polysilicon is used for the gate material and the substrate doping is $N_a = 10^{17}$ cm^{-3}.

a) Calculate the gate oxide thickness such that the NMOS transistor threshold voltage V_{TOn} = 0.7 V.
b) What is the doping concentration of the n-well required such that the PMOS transistor threshold voltage V_{TOp} = -0.7 V using the gate oxide thickness calculated in (a).
c) Calculate the surface potential ϕ_{son} for the NMOS device in thermal equilibrium using the gate oxide thickness calculated in (a).
d) Calculate the surface potential ϕ_{sop} for the PMOS device in thermal equilibrium using the gate oxide thickness calculated in (a).

Problem 5 Howe & Sodini P4.1