Design Project - April 20, 2001

Driver for Long Interconnect and Output Pad

Due: May 9, 2001 at recitation
(late project reports not accepted)

1. Overview

In this design problem, interface circuitry must be designed to bring a signal from the core of a large digital IC chip to an output pad where it is made available to the outside world. From the location where the signal is produced to the assigned output pad, there is a certain distance that needs to be covered by a long interconnect with a certain capacitance. The output pad and the rest of the world also represent a sizable capacitive load. The goal of the design problem is to design interface logic that accomplishes the job within the alloted time delay budget while minimizing power consumption.

2. Design problem statement

The design of large digital ICs involves a difficult compromise between speed and power consumption. With the increased emphasis on portable systems, there is a premium on ICs that squeeze more performance out of a very limited power budget. In an effort to address the requirements of this lucrative portable market, the IC industry has recently developed *dual threshold voltage* microfabrication processes in which two families of CMOS transistors with different threshold voltages coexist on the same wafer. These two types of transistors have the following general characteristics:

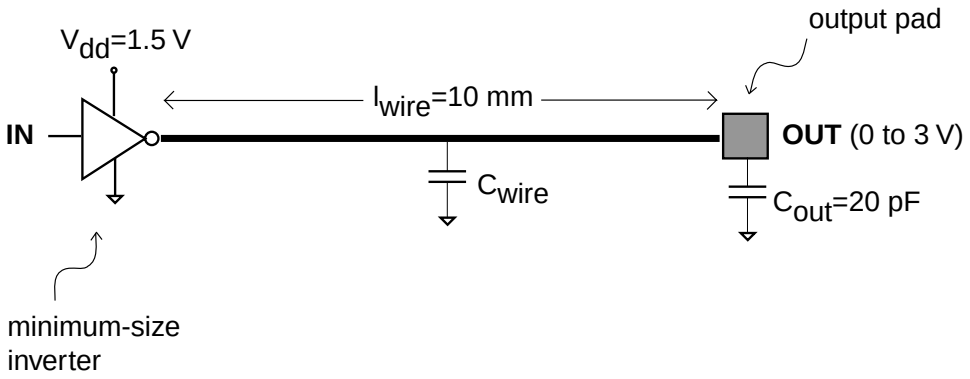

Figure 1: Goal of design problem: to bring a signal **IN** from a minimum-size inverter deep inside a large digital chip to an outside pad through a 10 mm long wire.

- *Low-V_T CMOS*: runs at a reduced voltage and is used for the large logic core of the chip.
- *High-V_T CMOS*: runs at a higher voltage rating and is used at the output pads that connect to the outside world.

These two kinds of transistors can be made available simultaneously on the same wafer by suitably adjusting the ion-implantation step that controls the threshold voltage of the device. Circuit designers choose the most suitable transistor option for every function inside the chip. The logic core contains the highest transistor count in the entire chip. As a result, a large amount of power is consumed there. For the core, the low-V_T devices are selected running at a reduced voltage so that overall power is minimized. In the periphery, signals have to be made available to the rest of the world. For the periphery, high-V_T devices are used and they operate at the voltage supply that the rest of the world expects.

In this design project, a large digital chip is being designed with a core that runs at a reduced voltage of 1.5 V. The chip, however, is going to be used as part of a chip set that operates at 3 V. The logic signals coming out of the chip must therefore be referred to 3 V. The job that has been assigned to you is to design an output interface for a logic signal that is coming out of the core. The signal **IN** goes through a minimum-size inverter (an inverter with transistors that have the minimum allowable size, see below for details) at a distance of 10 mm away from the output pad that has been assigned to it. The signal **IN** has logic levels of 0 and 1.5 V. This signal must be brought to its assigned output pad where it must appear with logic levels of 0 and 3 V. In consequence, the signal not only must be made to traverse a large distance on the chip, but a suitable logic level conversion must be performed at some point. A schematic illustration of the output interface is shown in Fig. 1.

You must design suitable circuitry to drive the long interconnect line and the output pad, and to perform the required logic level conversion. Your circuitry can sit immediately after the minimum size inverter through which **IN** goes, immediately before the output pad, anywhere in between, or split in any fashion that you want in between. For example, it is perfectly acceptable to have a design in which some circuitry is located immediately after the minimum-size inverter and some more circuitry is placed right before the output pad. You can choose to make the logic voltage conversion from 1.5 V to 3 V at any point you want.

A schematic representation of the signals involved in this design project is given in Fig. 2. These are 67 MHz signals with 1 ns rise and fall times.

The specs that the output interface must meet are the following:

1. The total delay from **IN** to **OUT** must be less than 10 ns. This applies to both the up transition as well as the down transition.
2. From a logic point of view, **OUT** = **IN** (not **OUT** = $\overline{\textbf{IN}}$).
3. The power budget alloted to this function (from **IN** to **OUT**) is 15 mW. You must try to minimize as much as possible below this figure.
4. The logic level **HI** at the output must not fall below 2.8 V. The logic level **LO** at the output must not be higher than 0.2 V.

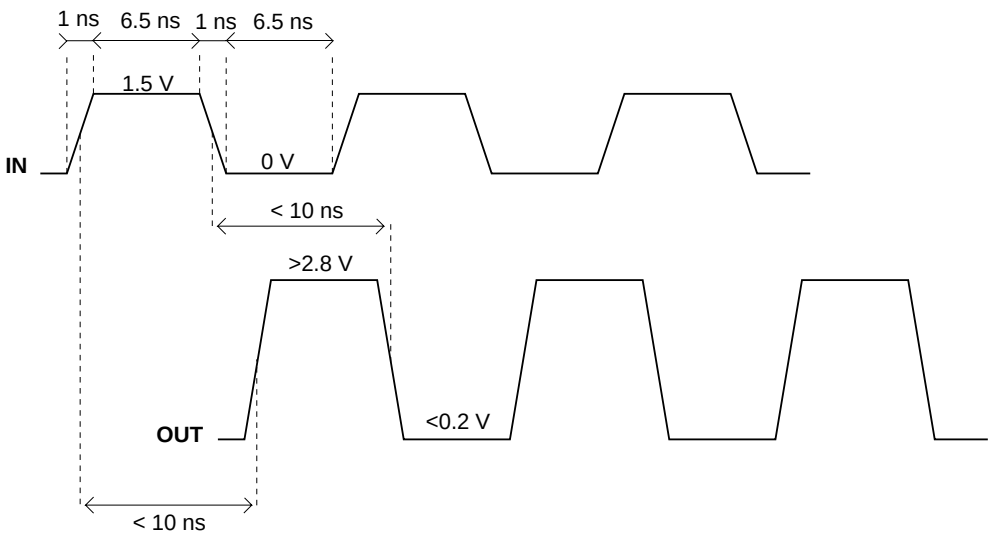

Figure 2: Time signals of design project.

5. To assure good voltage conversion even in the presence of noise, the first 3 V inverter where the voltage conversion is done must have a noise-margin-low of 0.6 V or better, and a noise-margin-high of 1.8 V or better.

3. Device models

There are two different sets of CMOS devices available in this process. The *low-V_T* devices run at a supply voltage of 1.5 V. The *high-V_T* devices run out of 3 V. You must use the correct supply with every transistor family.

The model parameters for minimum-size transistors of these two kinds are listed in Table I. All minimum size transistors have dimensions: $L_n = 1.5\ \mu m$, $W_n = 3\ \mu m$, $L_p = 1.5\ \mu m$, $W_p = 6\ \mu m$. For all minimum-size transistors, $L_{diff} = 4.5\ \mu m$.

Your design will require the use of bigger transistors too. W and L can scale up in increments no smaller than 0.5 μm. The parameter LAMBDA must be changed according to the transistor gate length, as indicated in the table. Read §4.6 of Howe & Sodini to see how transistor capacitances scale with geometry.

The wire is 5 μm wide. The capacitance per unit area of this metal is $C_w = 0.04 fF/\mu m^2$.

4. Deliverables

The deliverables of this design problem are as follows.

	low-V_T devices		high-V_T devices		
	NMOS	PMOS	NMOS	PMOS	units
VTO	0.5	-0.5	0.75	-0.75	V
TOX	1.5E-08	1.5E-08	1.5E-08	1.5E-08	m
KP	100E-06	50E-06	100E-06	50E-06	A/V^2
LAMBDA	7E-02$\frac{1.5}{L(\mu m)}$	7E-02$\frac{1.5}{L(\mu m)}$	7E-02$\frac{1.5}{L(\mu m)}$	7E-02$\frac{1.5}{L(\mu m)}$	V^{-1}
CJ	1E-04	3E-04	1E-04	3E-04	F/m^2
CJSW	5E-10	3.5E-10	5E-10	3.5E-10	F/m
PB	0.9	0.9	0.9	0.9	V

Table 1: SPICE parameters for both families of transistors available in the process.

1. (*20 points*) *Answer sheet with summary of results*. This sheet should show the location of all inverters, the size of all transistors and the voltage at which the inverters operate. It should also show the results of your hand calculations, and the results of HSPICE simulations for the specs listed above. You can use the sheet at the end of this handout for this purpose.
2. (*60 points*) A technical report with the following parts:

   (a) *Summary of hand calculations*. Here you should show a schematic diagram of your design. You should also indicate the selected transistor dimensions and operating voltages for each inverter. Then you should describe and comment on the following hand calculations:

   - Current drivability of each inverter.
   - Input capacitance presented by each inverter.
   - Dynamic power required in driving each stage.
   - Delays through every inverter.
   - Noise margins at the first 3 V inverter.

   Brief analysis: Your hand calculations should be commented appropriately. You should describe the thought process that you followed in your design, what where the tradeoffs that you faced and how did you arrive at the values you selected for the design parameters.

   (b) *HSPICE scripts and printouts*. You should carry out the following HSPICE simulations:

   - Transfer characteristics of the first 3V inverter with an extraction of the noise margins. This should be done with the inverter all by itself, that is, in isolation from the rest of the design. You will need a separate HSPICE deck for that. In order to get the transfer characteristics of this inverter, you should sweep V_{in} from 0 to 3 V and monitor V_{out}. Turn in a printout of the script and the resulting transfer characteristics.
   - Transient simulation for the entire design showing waveforms for **IN** and **OUT** signals. This script should extract the propagation delays from **IN** to **OUT** and the power dissipation. To avoid initial transitory effects, use 3rd or 4th clock cycles for these extractions. Turn in a printout of the script and the resulting waveforms.

The HSPICE scripts should be placed in your Athena Public directory for our examination. Make sure to give us your username and the complete path to these scripts in the summary page so that we can run them.

Brief analysis: You should comment on the following points. How did you arrive at the final values for the design parameters? How do these design parameters differ from those selected in the hand calculations and why?

3. (*20 points*) A *one-page design review abstract*. This is an abstract summarizing your project for a design review meeting. This abstract should concisely state the nature of the problem, the key design issues and trade-offs involved, your design strategy arguing why it is a good one, and the key results. This should be an attractively written abstract. It should bring up to speed other designers that will attend the design review. At the design review, your design (as well as others for other parts of the chip) will be presented. Please type this abstract.

5. Rules and assorted advice

You are encouraged to work on this design problem with a partner. However, both members of the team must have carried out all aspects of the design problem. It is not allowed to break the design problem into two pieces and have each partner carry out only one of these pieces. Each individual must also turn in a complete set of deliverables as outlined above. The partner's name should be identified in the answer sheet.

The deadline for this assignment is firm. We will not accept late submissions.

Use HSPICE in Athena. For help on how to get started in HSPICE, refer to the manuals that are available on the 6.012 web site. Use 25 ^{o}C as temperature in HSPICE. Also, specify LEVEL=1.

When doing hand calculations, include the drain-body, source-body and gate-source capacitance for your transistors, as they all have a significant effect on the speed and power dissipation of the circuit. To simplify the hand calculations, assume the gate-source capacitance is equal to WLC_{ox}. Also assume that the source-body and drain-body capacitors are bias independent with a value equal to the zero voltage capacitance. This will produce a conservative design, as the average capacitance is less than the zero voltage capacitance.

In general, a "hand calculation" means the use of simple equations to calculate results. In this case, these are the equations derived in class and in the book for delay, noise margins, etc. "Hand calculations" using these equations can be done any way you want - on paper, on a calculator, with a script in Matlab, in Excel, etc.

The effort involved in this assignment is substantial. You should start early. There are many aspects to this design problem that will require sustained attention on your part for a substantial amount of time. There is also a learning curve associated with HSPICE. This assignment cannot be done at the last minute!

Ask us plenty of questions. While every effort has been made for the specs to be reasonable and for the design project to be well described, there might be residual ambiguities. The first line of advice is the TA's. After that, don't hesitate to approach the recitation instructors and the lecturer.

Design Project - Summary Answer Sheet

Name: _____ Recitation: _____

Username: _____ HSPICE deck filename(s): _____

Partner's name: _____

Table 1: Results

Specification	Hand calculation	SPICE simulation	Required specs
total power dissipation (mW)			< 15
delay **IN**→**OUT**, t_{PLH} (ns)			< 10
delay **IN**→**OUT**, t_{PHL} (ns)			< 10
NM_L at first 3V inverter (V)			> 0.6
NM_H at first 3V inverter (V)			> 1.8
output swing **LO** (V)			< 0.2
output swing **HI** (V)			> 2.8

Table 2: Inverter specifications (fill as many entries as there are inverters in your design)

inverter #	distance from **IN** (mm)	V_{dd} (V)	L_n (μm)	W_n (μm)	L_p (μm)	W_p (μm)
1 (minimum)	0	1.5	1.5	3	1.5	6
2						
3						
4						
5						
6						
7						
8						
9						
10						