Lecture 6 - PN Junction and MOS Electrostatics (III)

Electrostatics of pn Junction under Bias

February 27, 2001

Contents:

1. electrostatics of pn junction under bias
2. depletion capacitance

Reading assignment:

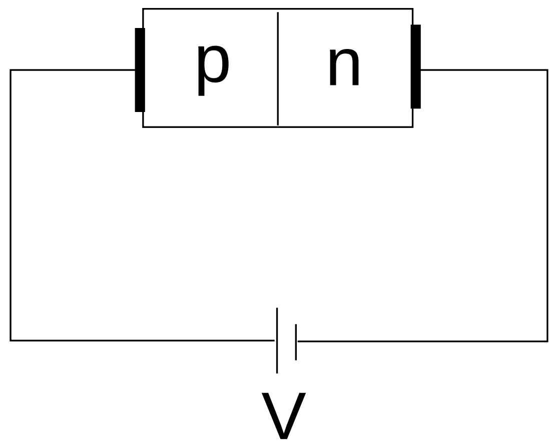
Howe and Sodini, Ch. 3, §§3.5-3.6

Key questions

- What happens to the electrostatics of a pn junction if a voltage is applied across its terminals?
- Why does a pn junction behave in some way like a capacitor?

1. Electrostatics of pn junction under bias

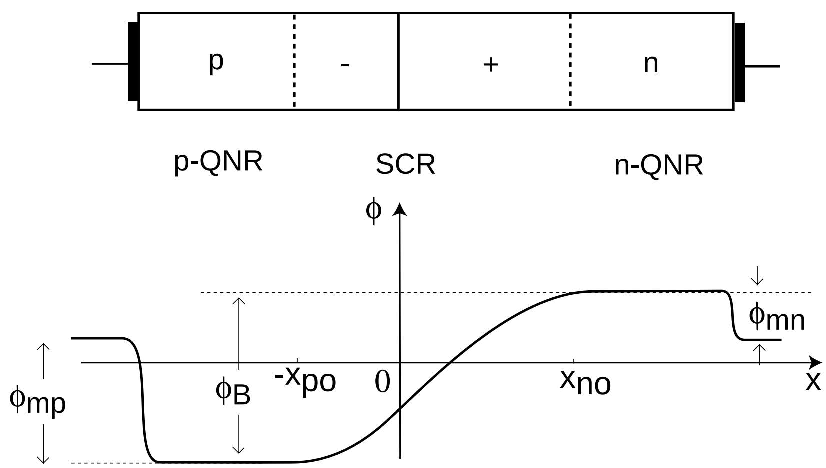
Bias convention for pn junction:



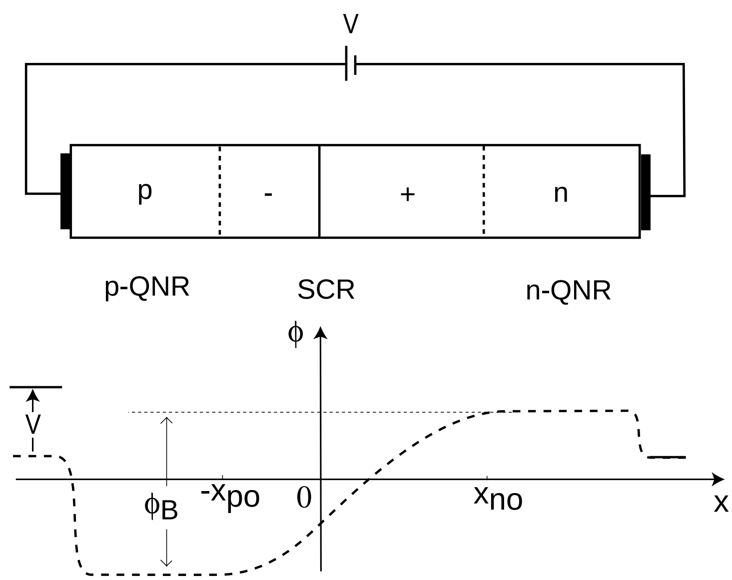
$V > 0$ *forward* bias

$V < 0$ *reverse* bias

• Potential distribution across pn junction in thermal equilibrium:

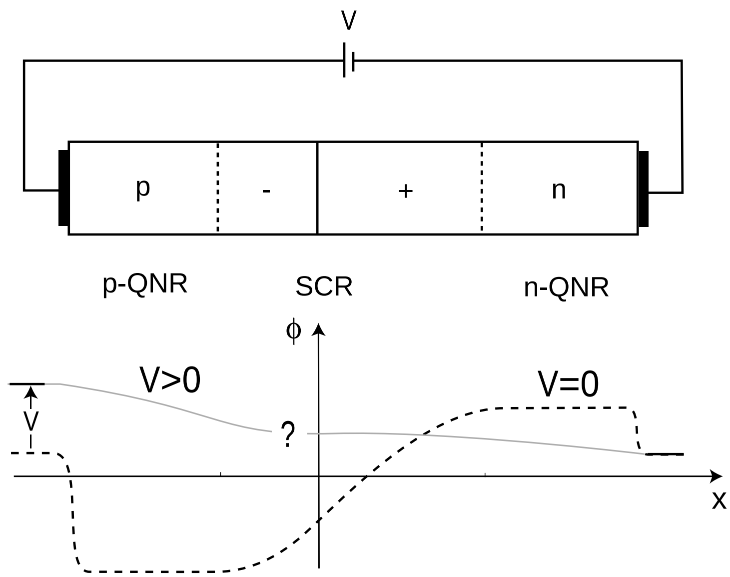


• Apply voltage to p-side with respect to n-side:



Battery imposes a potential difference across diode

How does potential distribution inside junction change as a result of bias?

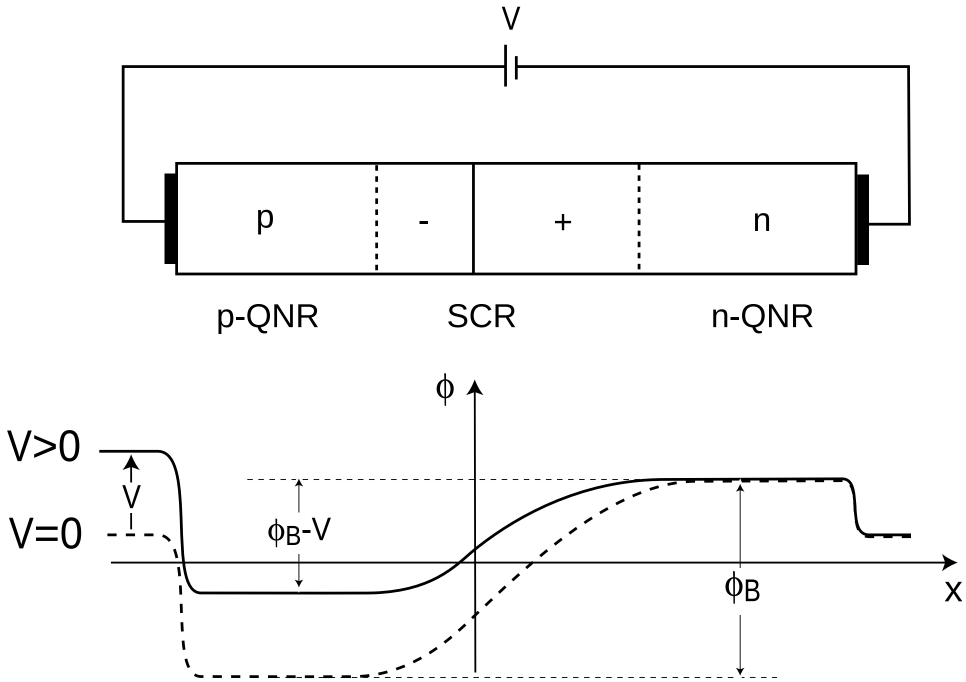


V can drop across five regions:

- metal/p-QNR contact
- p-QNR
- SCR
- n-QNR
- metal/n-QNR contact

In which region does V drop most?

Essentially, all applied voltage drops across SCR:

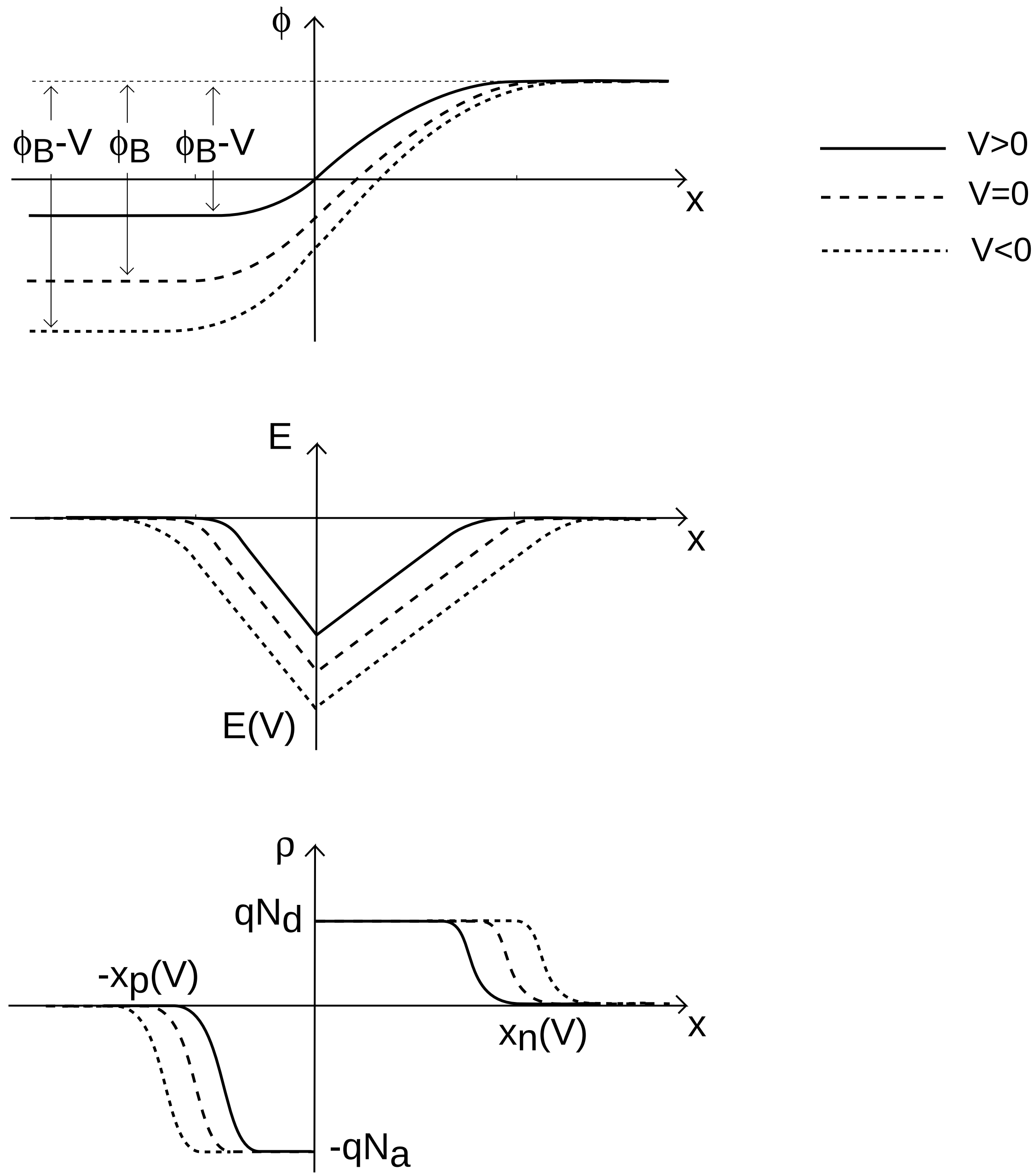


Potential difference across junction (potential "barrier"):

- in equilibrium: ϕ_B
- in forward bias: $\phi_B - V < \phi_B$
- in reverse bias: $\phi_B - V > \phi_B$ (since $V < 0$)

What happens to SCR electrostatics?

SCR electrostatics under bias:



forward bias: built-in potential $\downarrow \Rightarrow |E| \downarrow \Rightarrow x_d \downarrow$
reverse bias: built-in potential $\uparrow \Rightarrow |E| \uparrow \Rightarrow x_d \uparrow$

Fundamentally,

- electrostatics of SCR under bias unchanged from thermal equilibrium
- SCR dipole of charge modulated to accommodate modified potential build up across junction

Useful consequence:

- Analytical formulation of electrostatics of SCR identical to that of thermal equilibrium if:

$$\phi_B \longrightarrow \phi_B - V$$

Then:

$$x_n(V) = \sqrt{\frac{2\epsilon(\phi_B - V)N_a}{q(N_a + N_d)N_d}} \qquad x_p(V) = \sqrt{\frac{2\epsilon(\phi_B - V)N_d}{q(N_a + N_d)N_a}}$$

$$x_d(V) = \sqrt{\frac{2\epsilon(\phi_B - V)(N_a + N_d)}{qN_aN_d}}$$

$$|E|(V) = \sqrt{\frac{2q(\phi_B - V)N_aN_d}{\epsilon(N_a + N_d)}}$$

Can all be rewritten as:

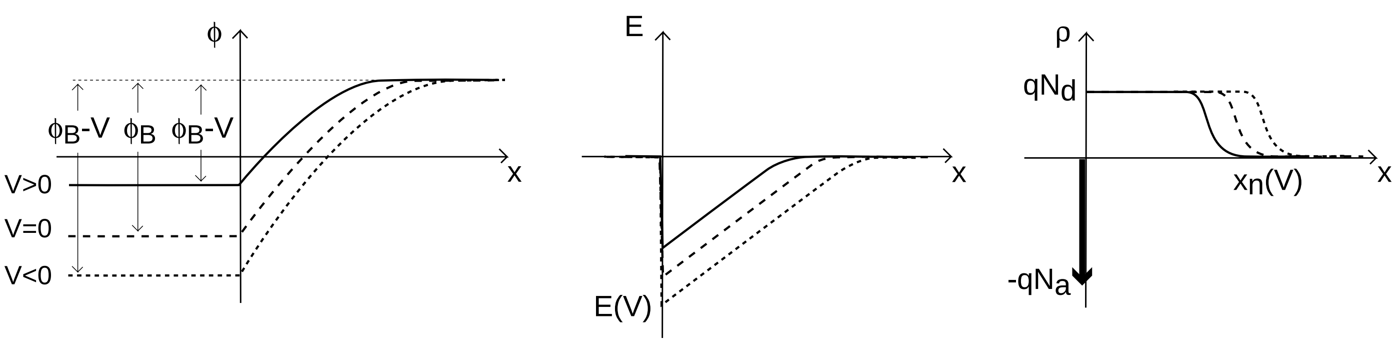
$$x_n(V) = x_{no}\sqrt{1 - \frac{V}{\phi_B}}$$

$$x_p(V) = x_{po}\sqrt{1 - \frac{V}{\phi_B}}$$

$$x_d(V) = x_{do}\sqrt{1 - \frac{V}{\phi_B}}$$

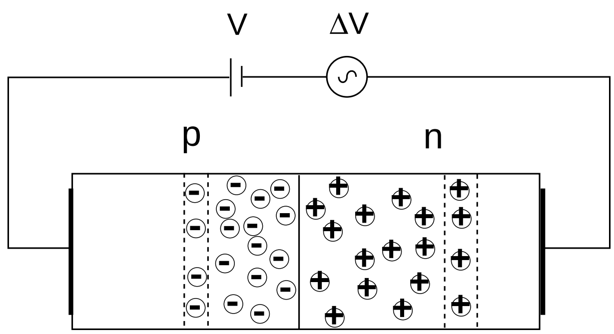
$$|E|(V) = |E_o|\sqrt{1 - \frac{V}{\phi_B}}$$

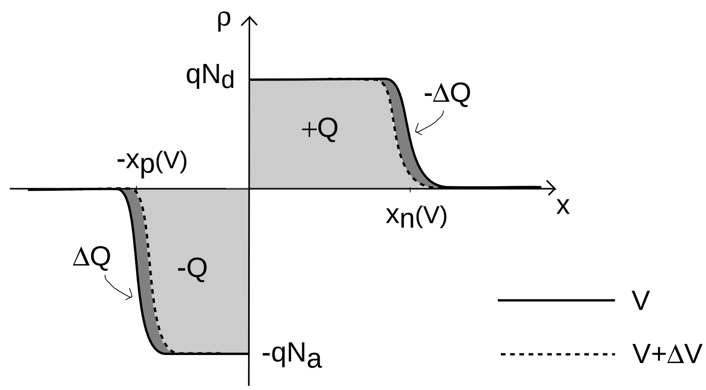
In strongly asymmetric junction, all changes take place in lowly doped side:

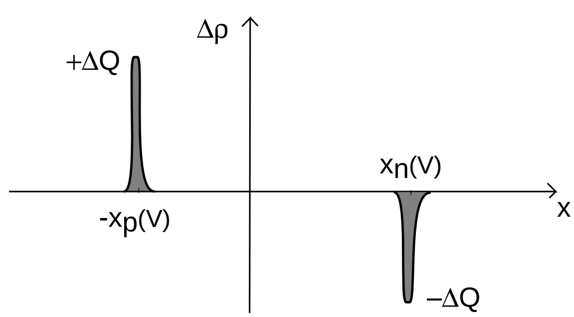


2. Depletion capacitance

Apply *small signal* on top of bias:





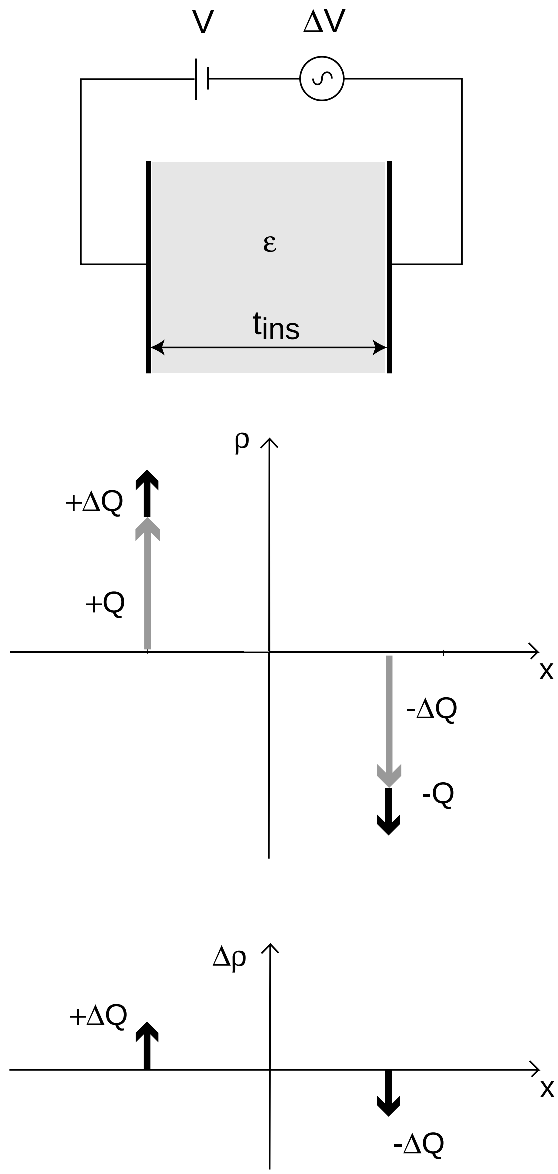


Change in ΔV across diode:

$\Rightarrow$ change of ΔQ at $-x_p$

$\Rightarrow$ change of $-\Delta Q$ at x_n

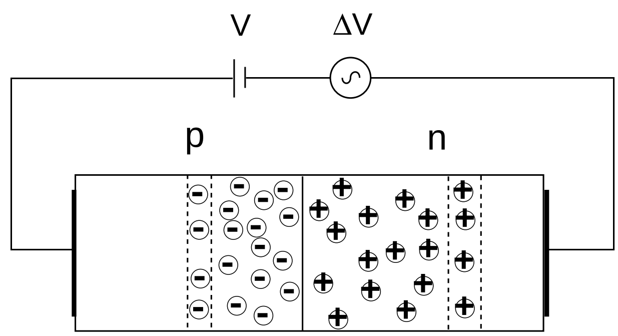
Looks like parallel-plate capacitor:

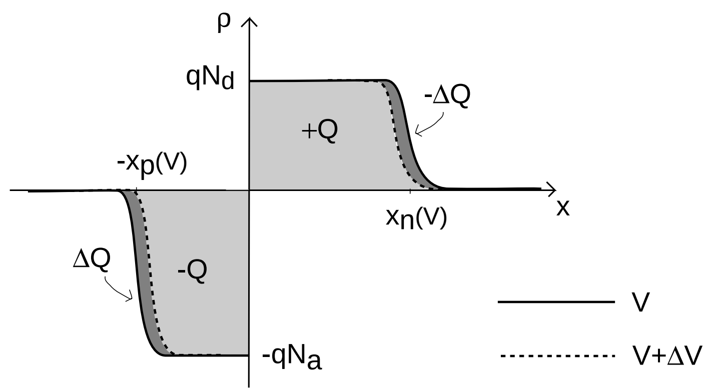


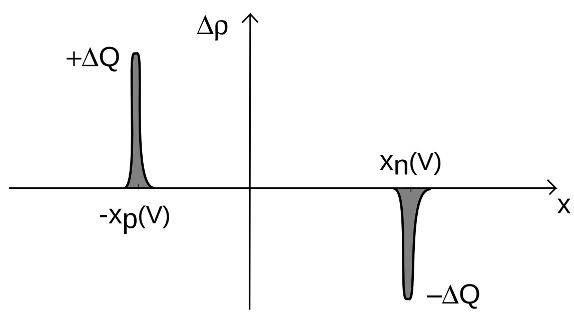
Capacitance per unit area:

$$C = \frac{\epsilon}{t_{ins}}$$

In analogy, in pn junction:







Depletion capacitance per unit area:

$$C_j(V) = \frac{\epsilon}{x_d(V)} = \sqrt{\frac{q\epsilon N_a N_d}{2(\phi_B - V)(N_a + N_d)}} = \frac{C_{jo}}{\sqrt{1 - \frac{V}{\phi_B}}}$$

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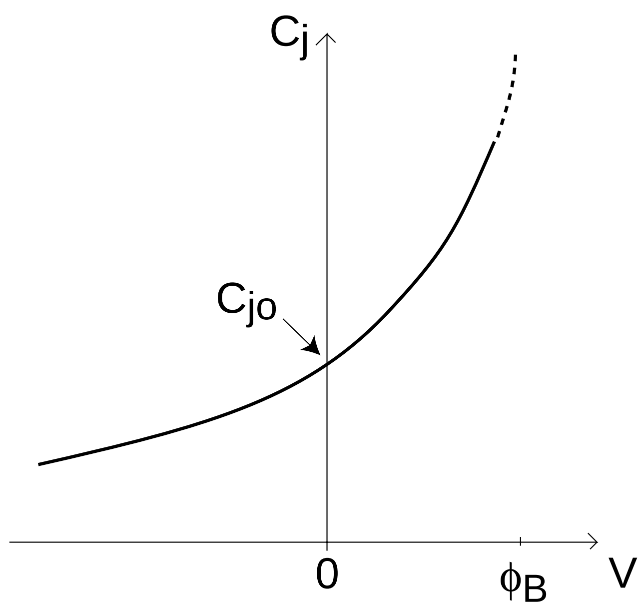
Key dependencies of C_j:

- C_j depends on bias (because x_d depends on bias)



- C_j depends on doping: $N_a,\ N_d \uparrow \Rightarrow C_j \uparrow$

- In strongly asymmetric junction (*i.e.* p$^+$-n junction):

$$C_j(V) \simeq \sqrt{\frac{q\epsilon N_d}{2(\phi_B - V)}}$$

capacitance dominated by lowly-doped side.

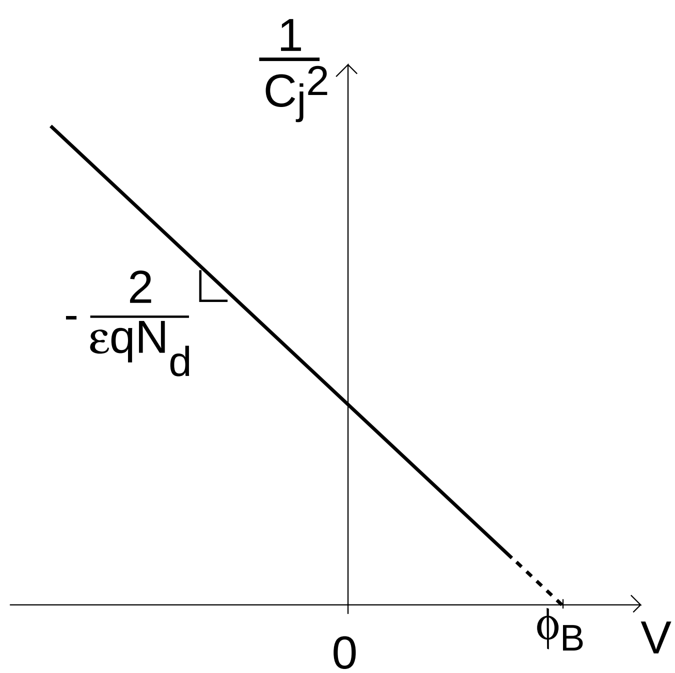
Relevance of capacitance-voltage characteristics of diode:

1. pn diode= variable capacitor (*varactor*):
   $\Rightarrow$ useful for *voltage-controlled oscillators* (VCO)

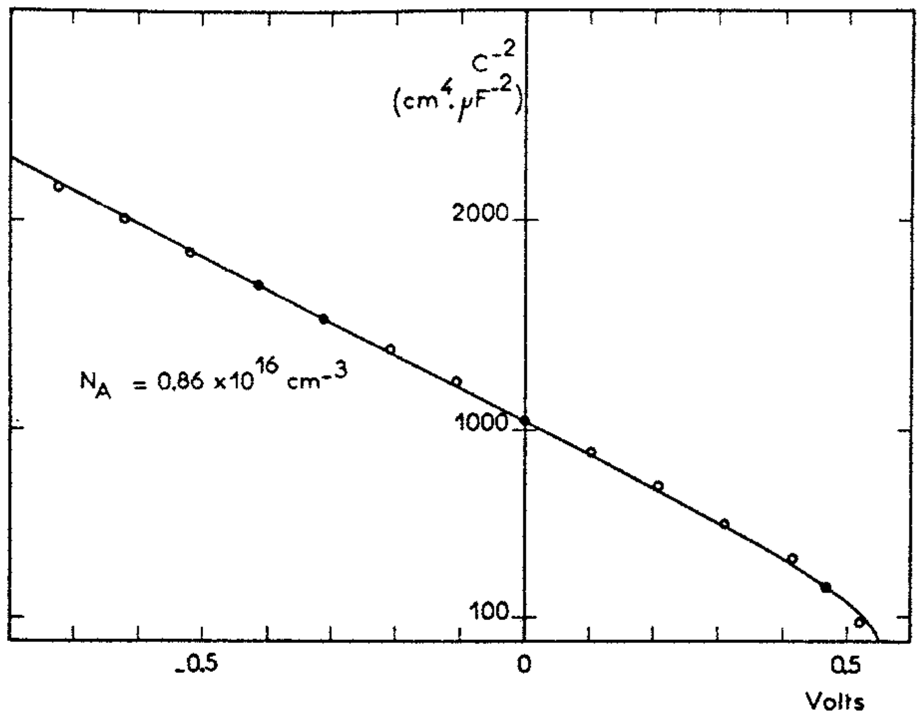
2. C_j: important consideration in dynamics of pn diode

3. powerful characterization technique:
   i.e. $1/C_j^2$ *vs.* V yields ϕ_B and N_d in strongly asymmetric p$^+$-n junction:

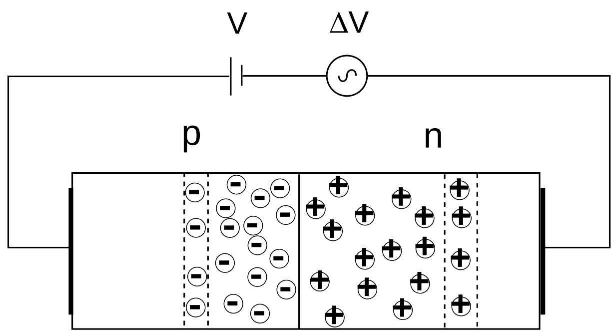
$$\frac{1}{C_j^2} \simeq \frac{2(\phi_B - V)}{q\epsilon N_d}$$

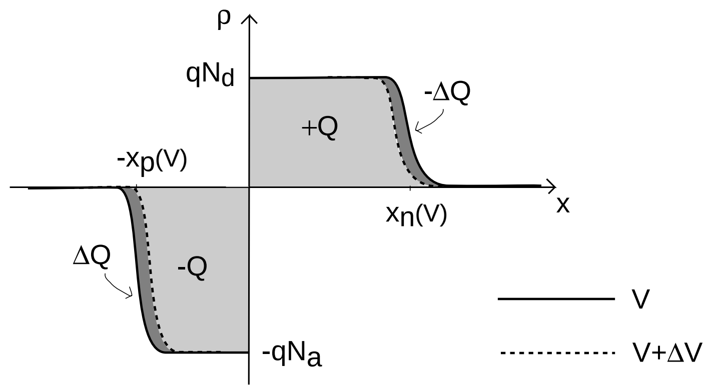


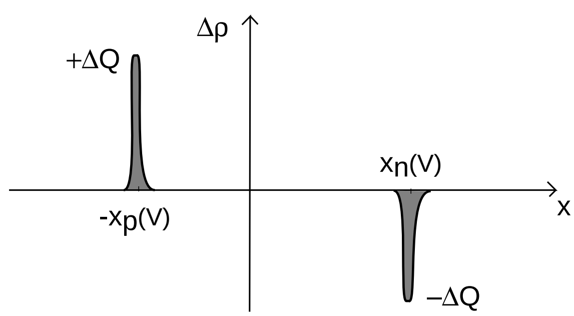
Experimental data [from *Fortini et al., IEEE Trans. Electron Dev. ED-29, 1604 (1982)*]:



Alternative view of capacitance: *depletion charge*







$$Q_j(V) = \sqrt{\frac{2q\epsilon N_a N_d(\phi_B - V)}{N_a + N_d}} = Q_{jo}\sqrt{1 - \frac{V}{\phi_B}}$$

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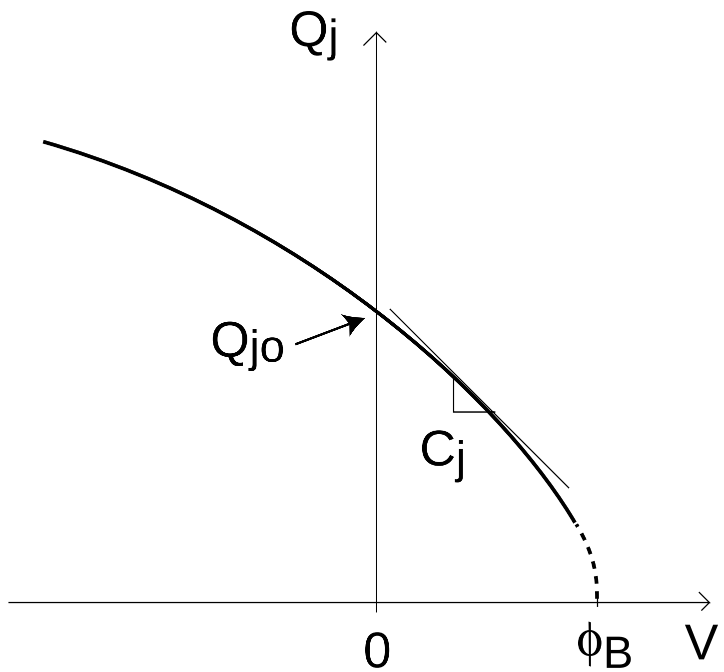


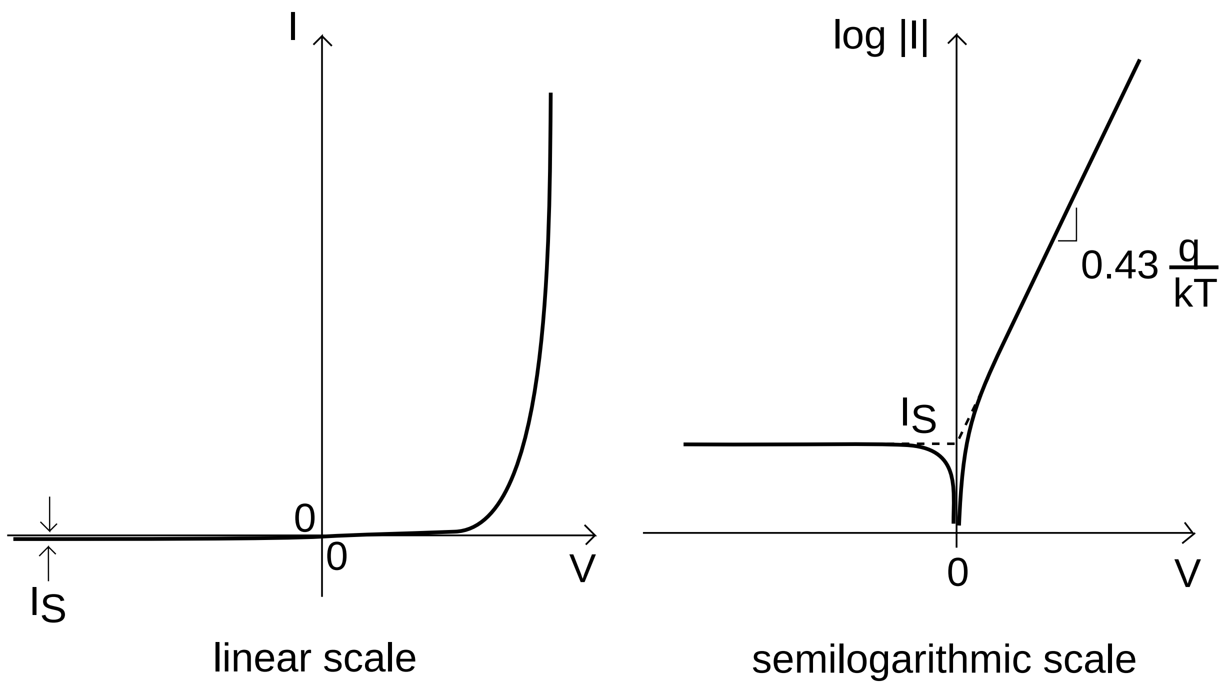
C_j is slope of Q_j vs. V characteristics:

$$C_j = \frac{dQ_j}{dV}$$

but not:

$$C_j = \frac{Q_j}{V}$$

Application of voltage to pn junction also results in current: pn diode.



Will study after MOSFET and CMOS digital circuits.

Key conclusions

- Voltage applied to pn junction drops across SCR:
  $\Rightarrow$ SCR electrostatics modified
  - in forward bias: $x_d \downarrow,\ |E| \downarrow$
  - in reverse bias: $x_d \uparrow,\ |E| \uparrow$
- Analytical formulation for SCR electrostatics in thermal equilibrium valid under bias if:

$$\phi_B \longrightarrow \phi_B - V$$

- As V changes, SCR charge changes too:
  $\Rightarrow$ *depletion capacitance*
- pn junction depletion capacitance depends on bias