Lecture 9 - MOSFET (I)

MOSFET I-V CHARACTERISTICS

March 8, 2001

Contents:

1. MOSFET: cross-section, layout, symbols
2. Qualitative operation
3. I-V characteristics

Reading assignment:

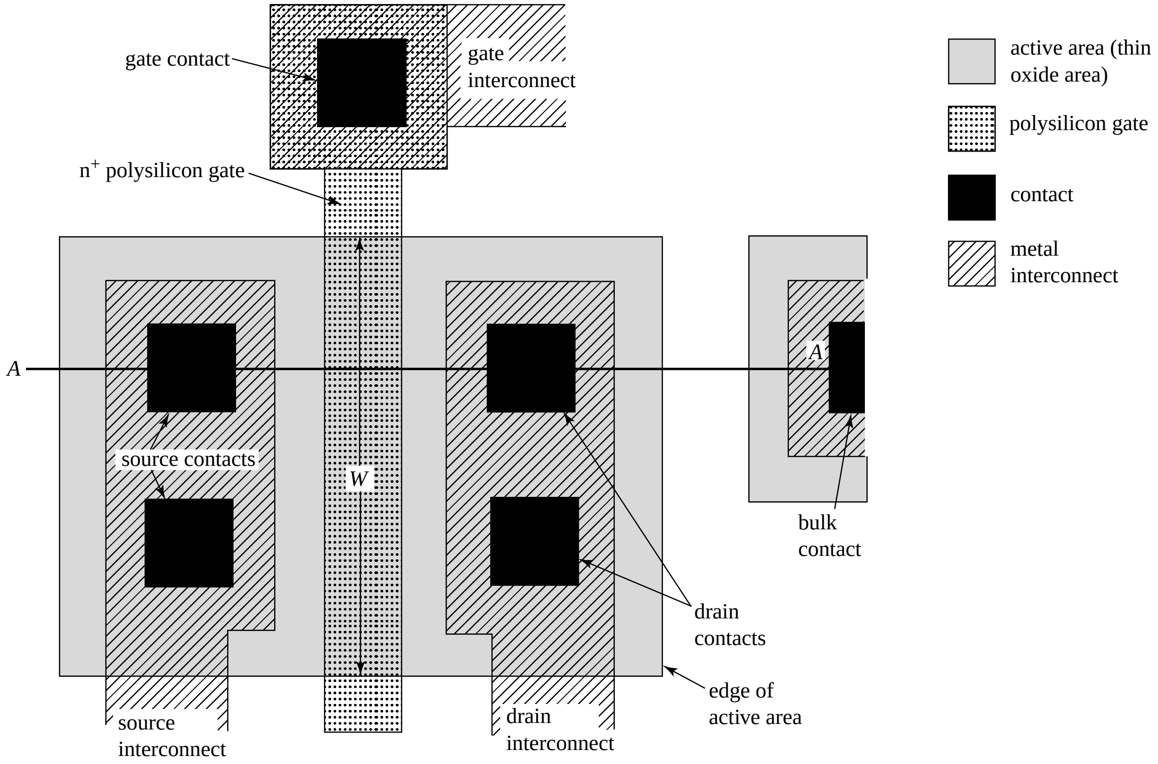
Howe and Sodini, Ch. 4, §§4.1-4.3

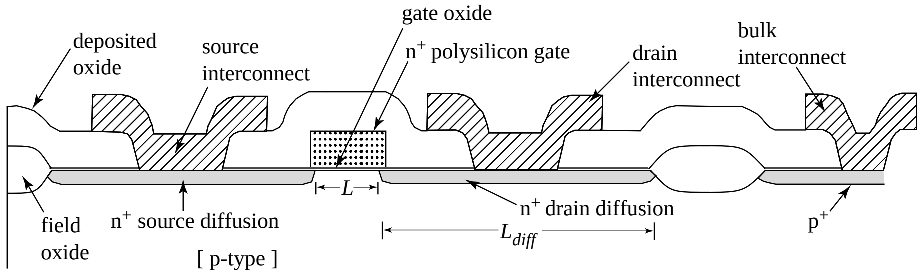
Announcements: Quiz #1, March 14, 7:30-9:30 PM, Walker Memorial; covers Lectures #1-9; open book; must have calculator.

Key questions

- How can carrier inversion be exploited to make a transistor?
- How does a MOSFET work?
- How does one construct a simple first-order model for the current-voltage characteristics of a MOSFET?

1. MOSFET: layout, cross-section, symbols





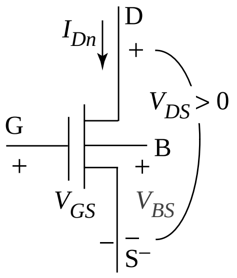
Key elements:

- inversion layer under *gate* (depending on gate voltage)
- heavily-doped regions reach underneath gate ⇒ inversion layer electrically connects *source* and *drain*
- 4-terminal device: *body* voltage important

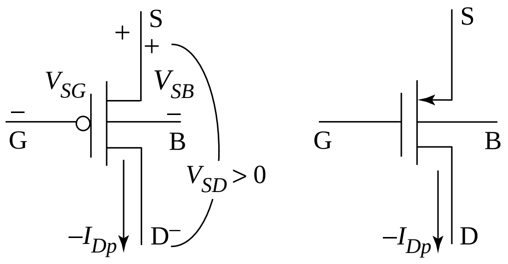
☐ Circuit symbols

Two complementary devices:

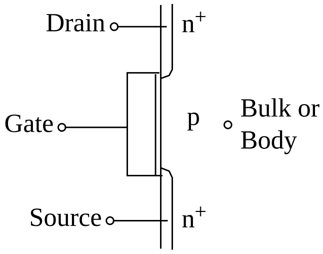
- n-channel device (n-MOSFET) on p-Si substrate (uses electron inversion layer)
- p-channel device (p-MOSFET) on n-Si substrate (uses hole inversion layer)

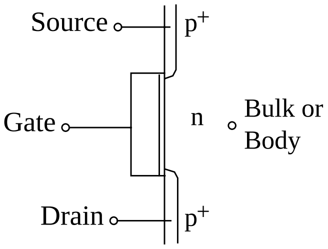


(a) n-channel MOSFET



(b) p-channel MOSFET

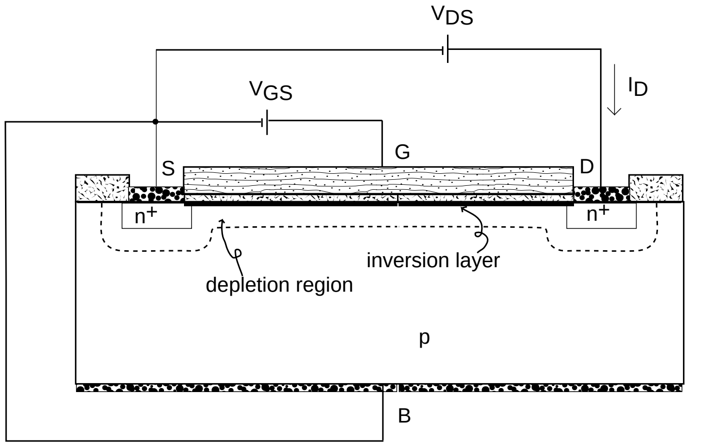


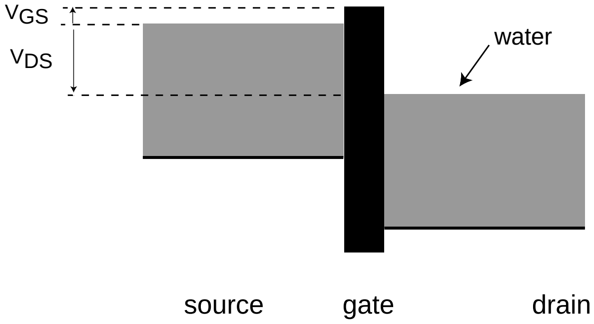


2. Qualitative operation

Water analogy of MOSFET:

- *Source*: water reservoir
- *Drain*: water reservoir
- *Gate*: gate between source and drain reservoirs





Want to understand MOSFET operation as a function of:

- gate-to-source voltage (gate height over source water level)
- drain-to-source voltage (water level difference between reservoirs)

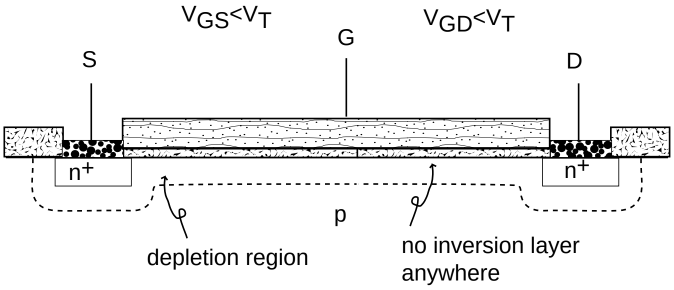
Initially consider source tied up to body (substrate or back).

Three regimes of operation:

□ *Cut-off regime*:

- MOSFET: $V_{GS} < V_T$, $V_{GD} < V_T$ with $V_{DS} > 0$.

- Water analogy: gate closed; no water can flow regardless of relative height of source and drain reservoirs.

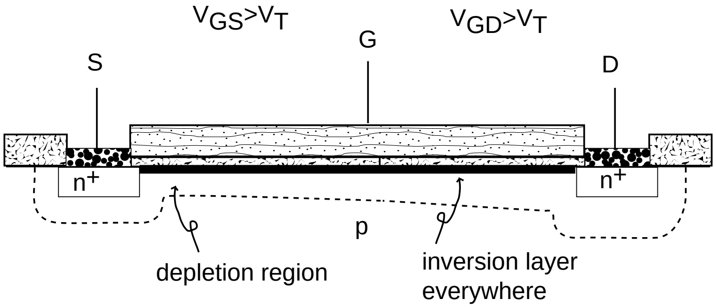


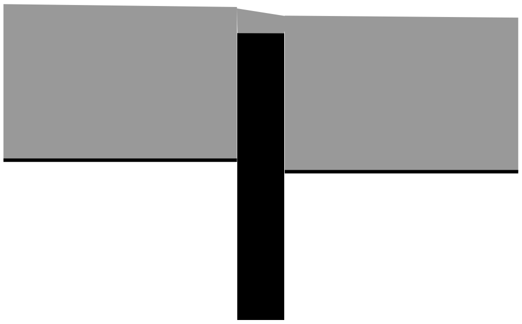

no water flow

$I_D = 0$

□ *Linear* or *Triode regime*:

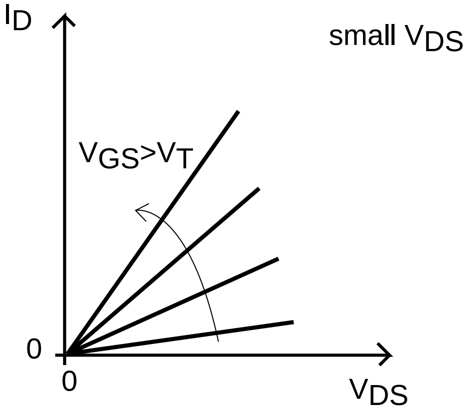
- MOSFET: $V_{GS} > V_T$, $V_{GD} > V_T$, with $V_{DS} > 0$.
- Water analogy: gate open but small difference in height between source and drain; water flows.





Electrons drift from source to drain ⇒ electrical current!

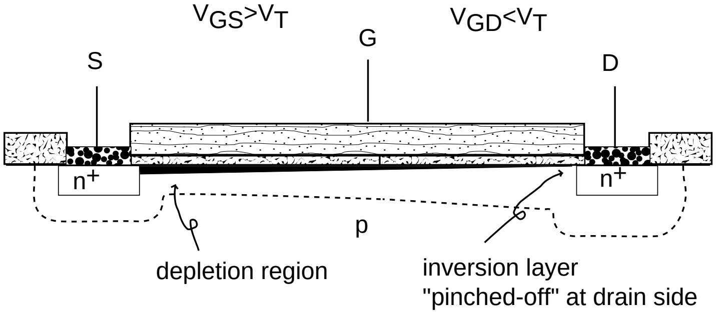
- $V_{GS} \uparrow \rightarrow\ |Q_n| \uparrow \rightarrow\ I_D \uparrow$
- $V_{DS} \uparrow \rightarrow\ E_y \uparrow \rightarrow I_D \uparrow$

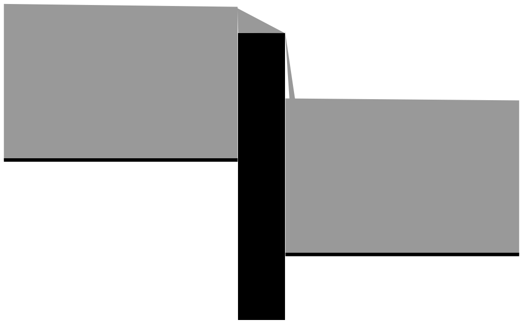


☐ *Saturation regime*:

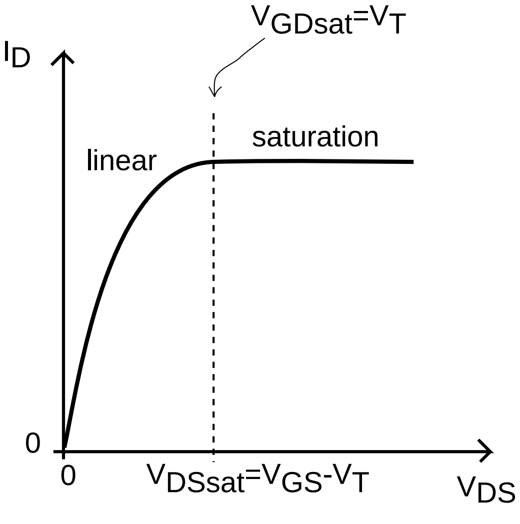
- MOSFET: $V_{GS} > V_T$, $V_{GD} < V_T$ ($V_{DS} > 0$).

- Water analogy: gate open; water flows from source to drain, but free-drop on drain side ⇒ total flow independent of relative reservoir height!



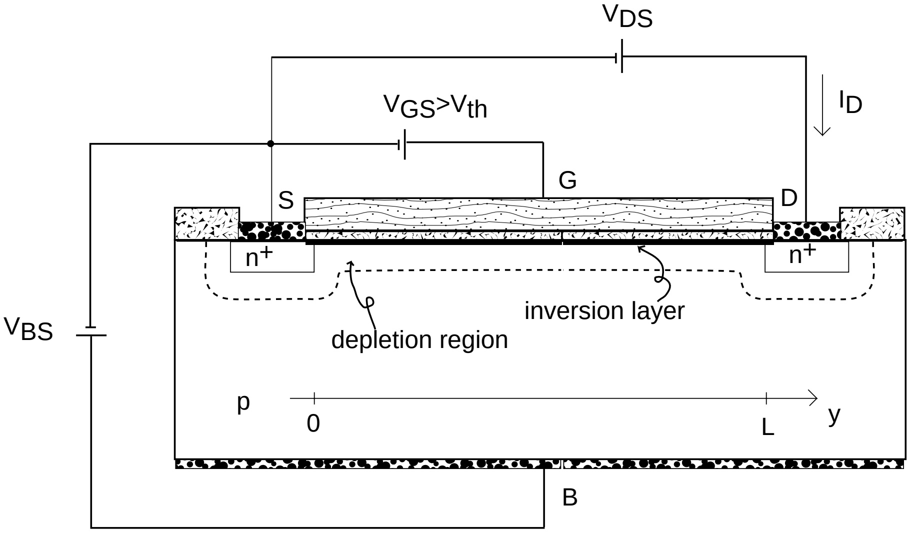


I_D independent of V_{DS}: $I_D = I_{Dsat}$



3. I-V characteristics

Geometry of problem:



☐ General expression of channel current

Current can only flow in y-direction:

$$J_y = Q_n(y)v_y(y)$$

Total channel current:

$$I_y = WQ_n(y)v_y(y)$$

Drain current is equal to *minus* channel current:

$$I_D = -WQ_n(y)v_y(y)$$

$$I_D = -WQ_n(y)v_y(y)$$

Rewrite in terms of voltage at channel location y, $V_c(y)$:

- If electric field is not too big:

$$v_y(y) \simeq -\mu_n E_y(y) = \mu_n \frac{dV_c(y)}{dy}$$

- For $Q_n(y)$ use charge-control relation at location y:

$$Q_n(y) = -C_{ox}[V_{GS} - V_c(y) - V_T]$$

for $V_{GS} - V_c(y) \geq V_T$.

All together:

$$I_D = W\mu_n C_{ox}(V_{GS} - V_c(y) - V_T)\frac{dV_c(y)}{dy}$$

Simple linear first-order differential equation with one unknown, the channel voltage $V_c(y)$.

Solve by separating variables:

$$I_D dy = W\mu_n C_{ox}(V_{GS} - V_c - V_T)dV_c$$

Integrate along the channel in the linear regime:

-for $y = 0$, $V_c(0) = 0$

-for $y = L$, $V_c(L) = V_{DS}$ (linear regime)

Then:

$$I_D \int_0^L dy = W\mu_n C_{ox} \int_0^{V_{DS}} (V_{GS} - V_c - V_T)dV_c$$

or:

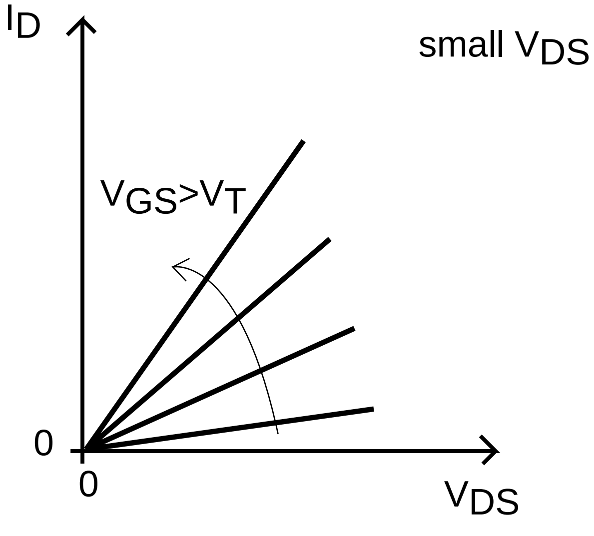
$$I_D = \frac{W}{L}\mu_n C_{ox}(V_{GS} - \frac{V_{DS}}{2} - V_T)V_{DS}$$

For small V_{DS}:

$$I_D \simeq \frac{W}{L}\mu_n C_{ox}(V_{GS} - V_T)V_{DS}$$

Key dependencies:

- $V_{DS} \uparrow \rightarrow I_D \uparrow$ (higher lateral electric field);
- $V_{GS} \uparrow \rightarrow I_D \uparrow$ (higher electron concentration);
- $L \uparrow \rightarrow I_C \downarrow$ (lower lateral electric field).
- $W \uparrow \rightarrow I_C \uparrow$ (wider conduction channel).



This is the *linear* or *triode* regime.

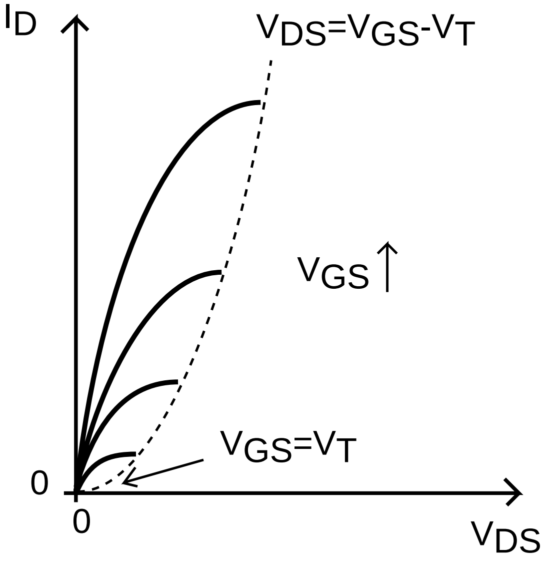
In general,

$$I_D = \frac{W}{L}\mu_n C_{ox}(V_{GS} - \frac{V_{DS}}{2} - V_T)V_{DS}$$

Equation valid if $V_{GS} - V(y) \geq V_T$ *at every y.*

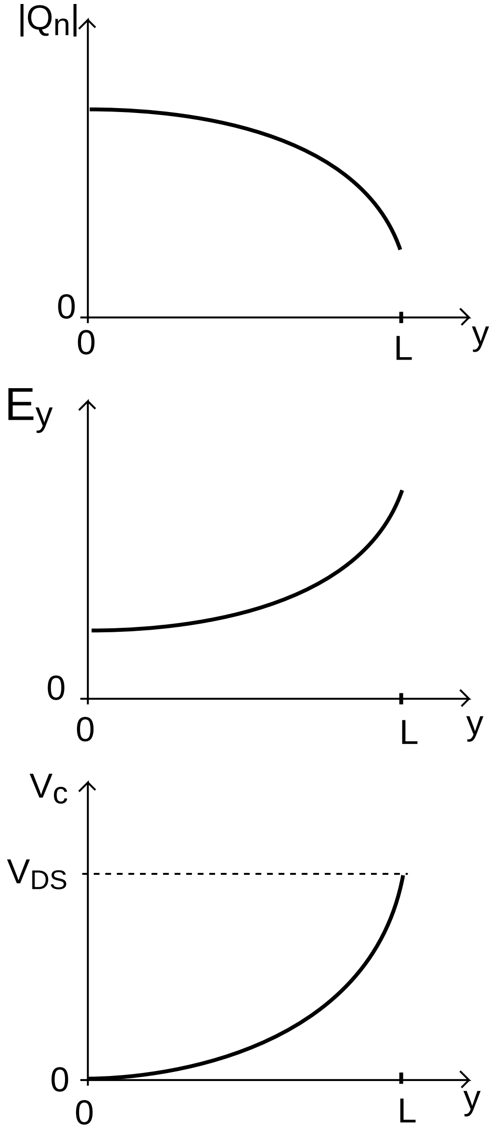
Worst point is $y = L$, where $V(y) = V_{DS}$, hence, equation valid if $V_{GS} - V_{DS} \geq V_T$, or:

$$V_{DS} \leq V_{GS} - V_T$$



term responsible for bend over of I_D: $-\frac{V_{DS}}{2}$

To understand why I_D bends over, must understand first *channel debiasing*:

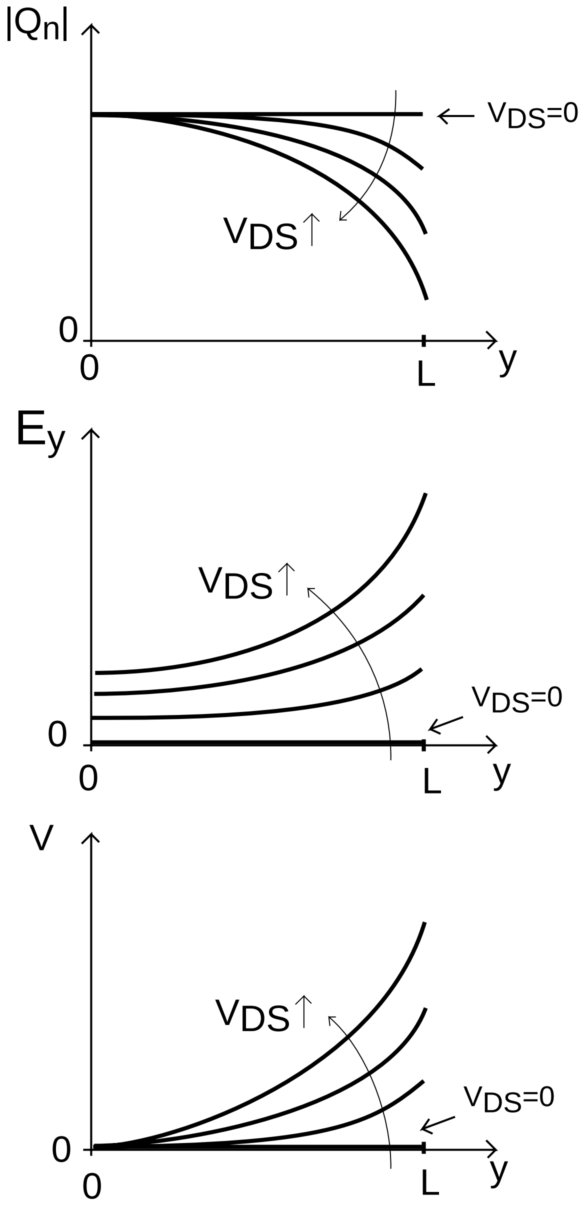


Along channel from source to drain:

$$y \uparrow \rightarrow \; V_c(y) \uparrow \rightarrow |Q_n(y)| \downarrow \rightarrow E_y(y) \uparrow$$

Local "channel overdrive" reduced closer to drain.

Impact of V_{DS}:



As $V_{DS} \uparrow$, channel debiasing more prominent

$\Rightarrow I_D$ rises more slowly with V_{DS}

□ Drain current saturation

As V_{DS} approaches

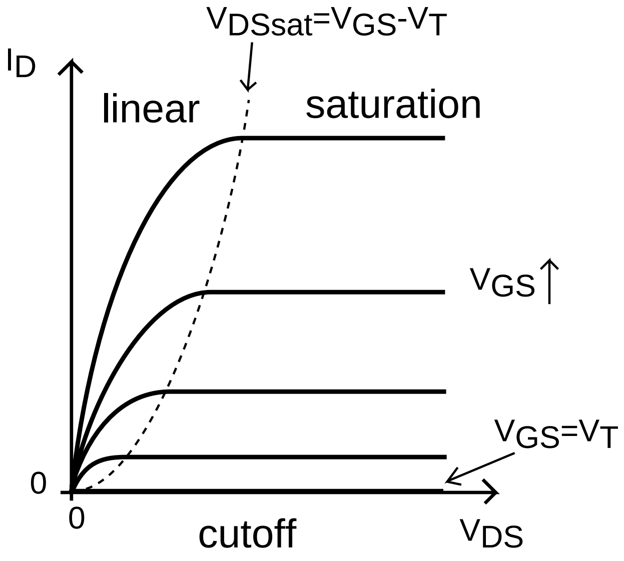
$$V_{DSsat} = V_{GS} - V_T$$

increase in E_y compensated by decrease in $|Q_n|$
$\Rightarrow I_D$ saturates to:

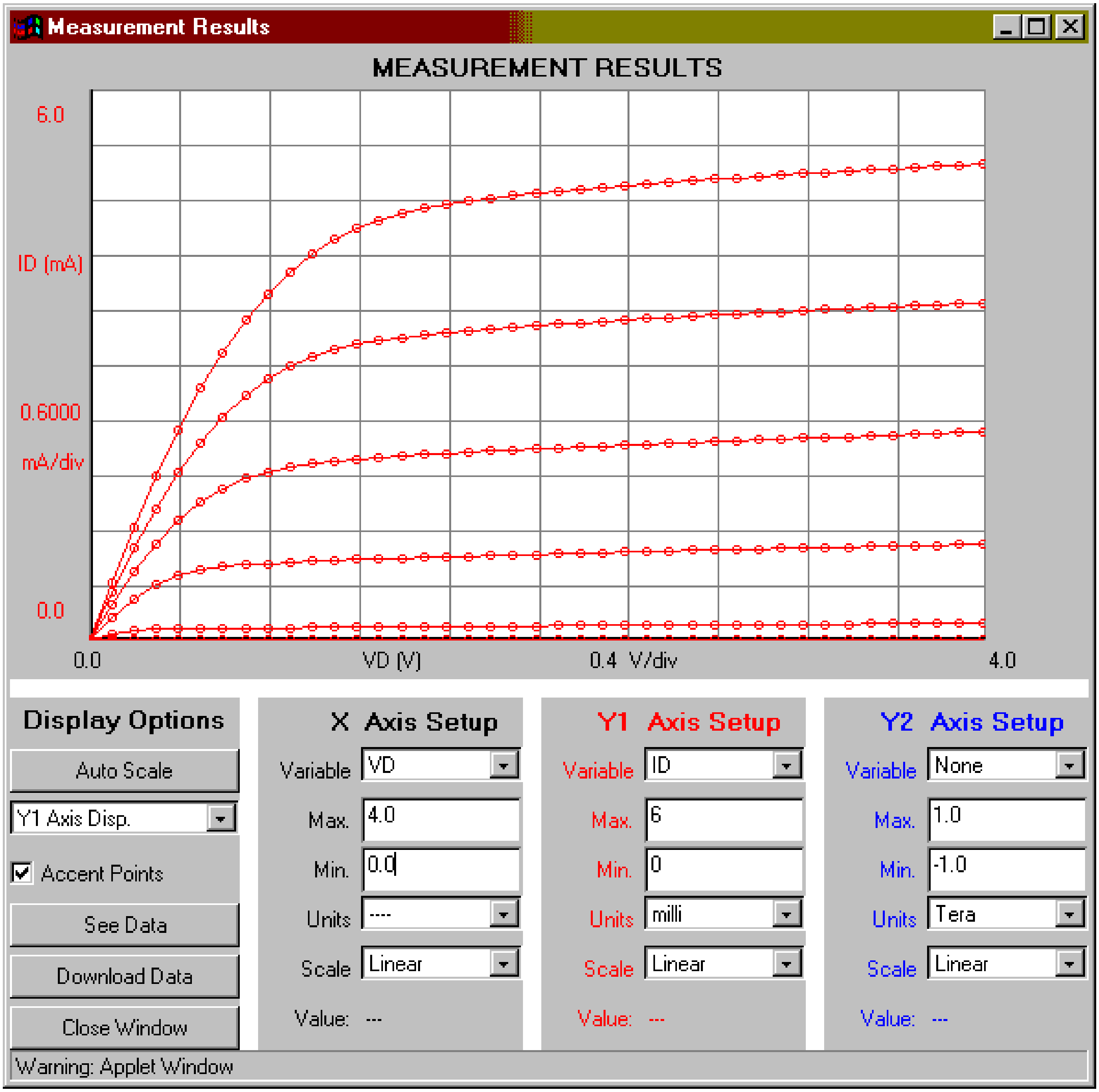
$$I_{Dsat} = I_{Dlin}(V_{DS} = V_{DSsat} = V_{GS} - V_T)$$

then

$$I_{Dsat} = \frac{W}{2L}\mu_n C_{ox}(V_{GS} - V_T)^2$$



Will talk more next time about saturation regime.



Display Options

Y1 Axis Disp.

☑ Accent Points

X Axis Setup

Variable: VD

Max.: 4.0

Min.: 0.0

Units: ----

Scale: Linear

Value: ---

Y1 Axis Setup

Variable: ID

Max.: 6

Min.: 0

Units: milli

Scale: Linear

Value: ---

Y2 Axis Setup

Variable: None

Max.: 1.0

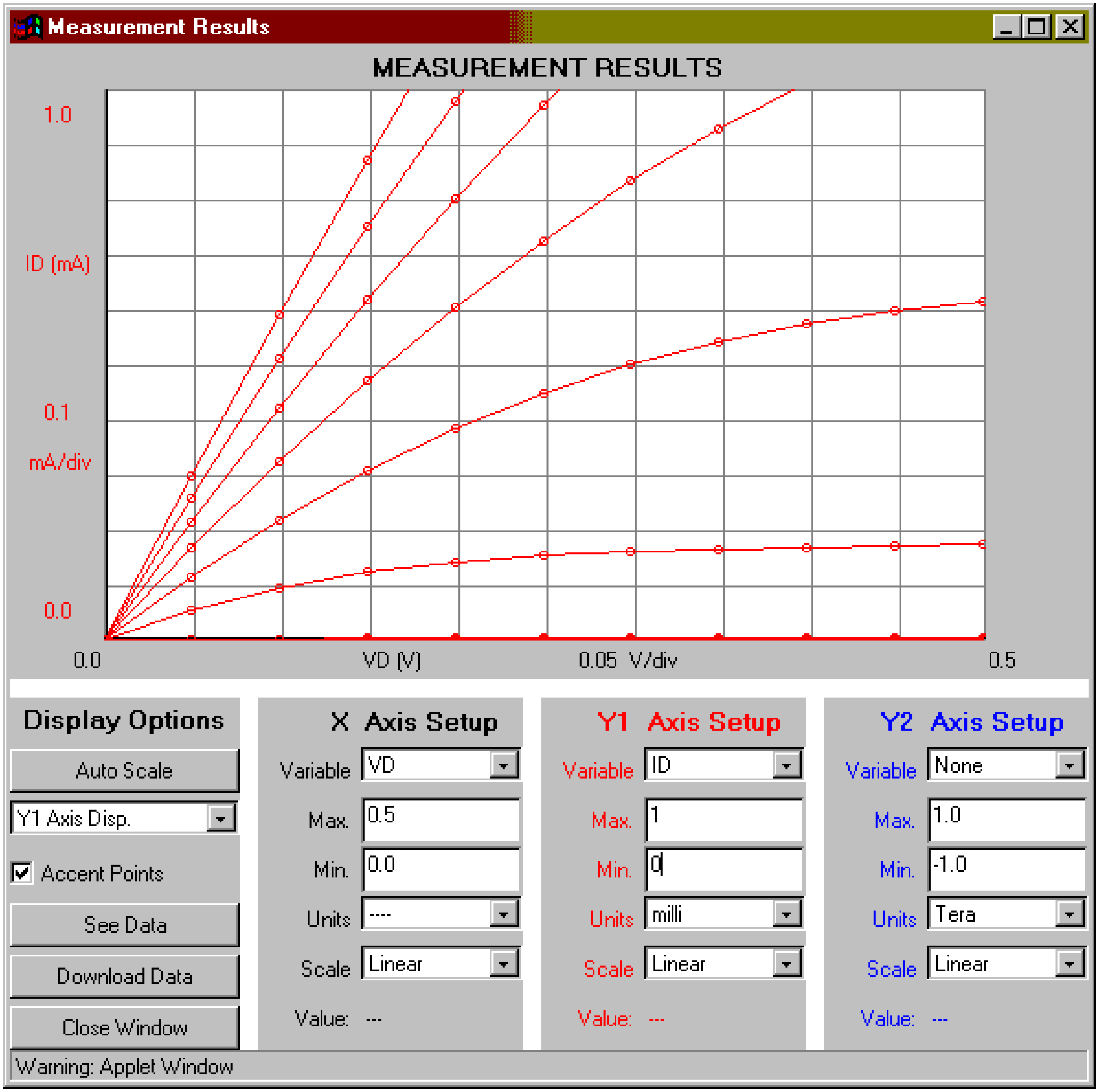
Min.: -1.0

Units: Tera

Scale: Linear

Value: ---

Warning: Applet Window



Y1 Axis Disp.

☑ Accent Points

	X Axis Setup	Y1 Axis Setup	Y2 Axis Setup
Variable	VD	ID	None
Max.	0.5	1	1.0
Min.	0.0	0	-1.0
Units	----	milli	Tera
Scale	Linear	Linear	Linear
Value:	---	---	---

Warning: Applet Window

Key conclusions

- The MOSFET is a *field-effect transistor*:
  - the amount of charge in the inversion layer is controlled by the field-effect action of the gate
  - the charge in the inversion layer is mobile ⇒ conduction possible between source and drain
- In the *linear regime*:
  - $V_{GS} \uparrow \Rightarrow I_D \uparrow$: more electrons in the channel
  - $V_{DS} \uparrow \Rightarrow I_D \uparrow$: stronger field pulling electrons out of the source
- *Channel debiasing*: inversion layer "thins down" from source to drain ⇒ current saturation as V_{DS} approaches:

$$V_{DSsat} = V_{GS} - V_T$$