

Lecture 20 - Transistor Amplifiers (II)

OTHER AMPLIFIER STAGES

April 26, 2001

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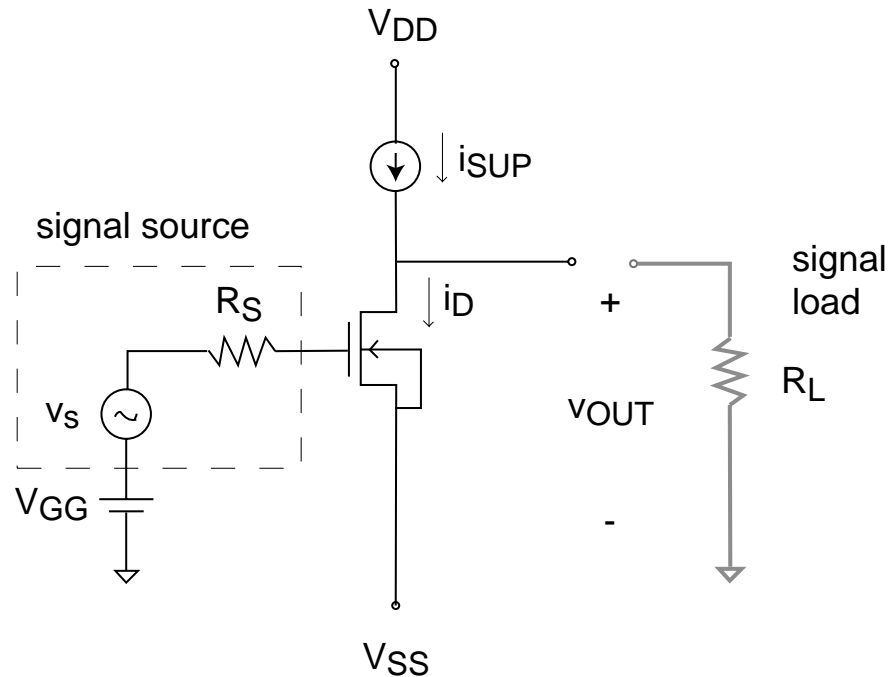
Reading assignment:

Howe and Sodini, Ch. 8, §§8.7-8.9

Key questions

- What other amplifier stages can one build with a single MOSFET and a current source?
- What is the uniqueness of these other stages?

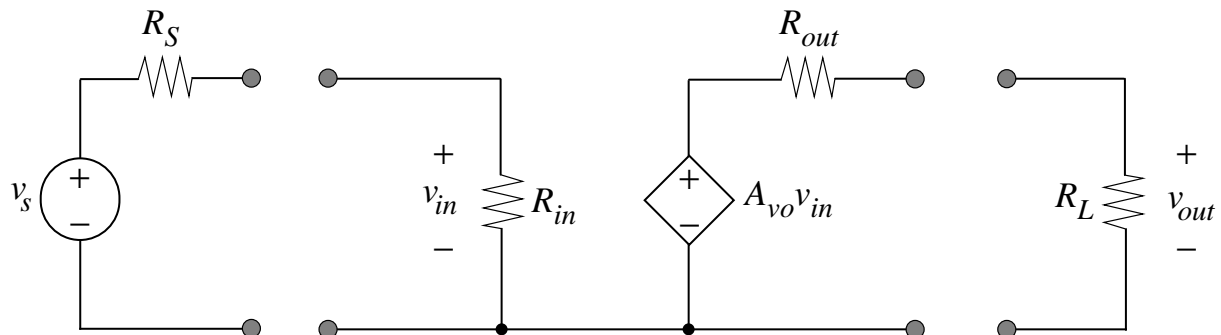
1. Common-source amplifier with current source supply (*summary*)



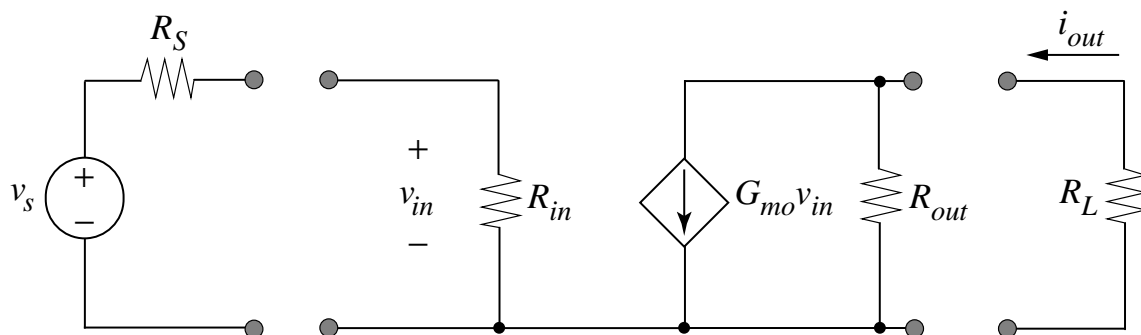
Summary of small-signal results:

- Unloaded voltage gain: $A_{vo} = -g_m(r_o // r_{oc})$
- Input resistance: $R_{in} = \infty$
- Output resistance: $R_{out} = r_o // r_{oc}$

Common-source amplifier is acceptable *voltage* amplifier
(want high R_{in} , high A_{vo} , low R_{out}):



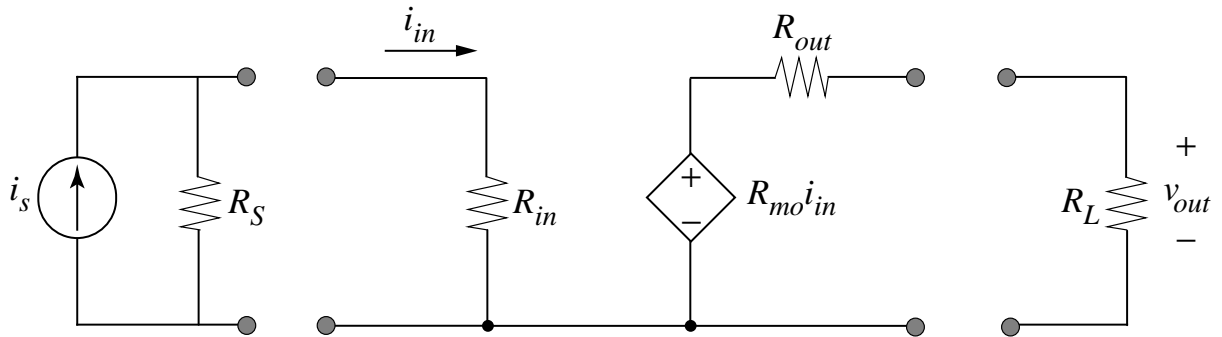
... but excellent *transconductance* amplifier
(want high R_{in} , high G_{mo} , high R_{out}):



For common-source amplifier:

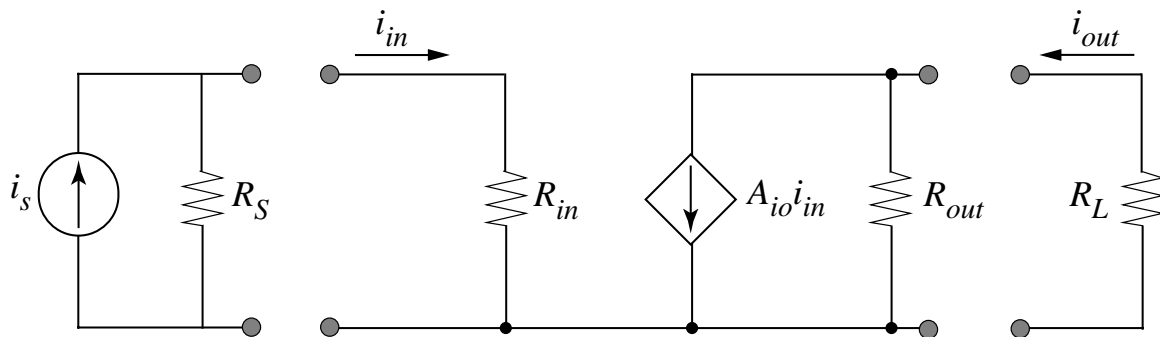
$$G_{mo} = g_m$$

Common-source amplifier does not work as *transresistance* amplifier (want low R_{in} , high R_{mo} , low R_{out}):



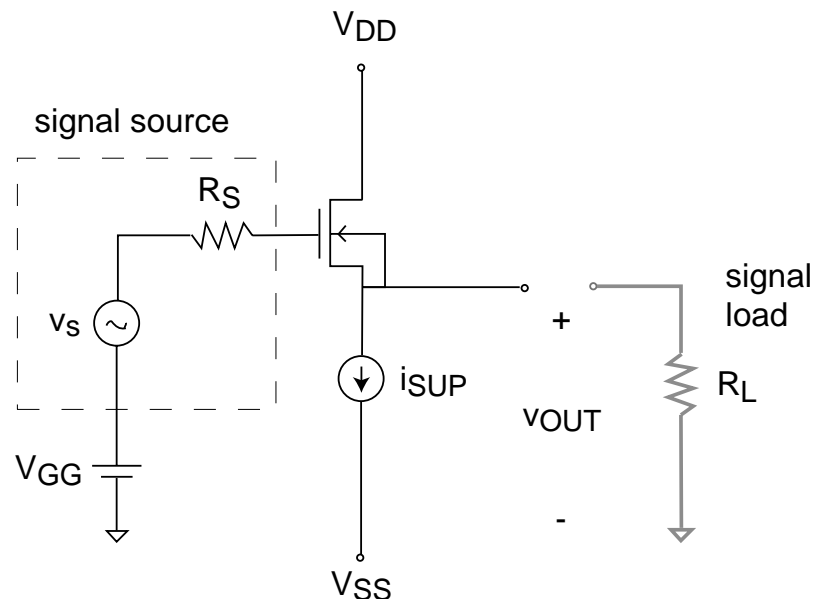
nor as *current* amplifier

(want low R_{in} , high A_{io} , high R_{out}):



Need new amplifier configurations.

2. Common-drain amplifier

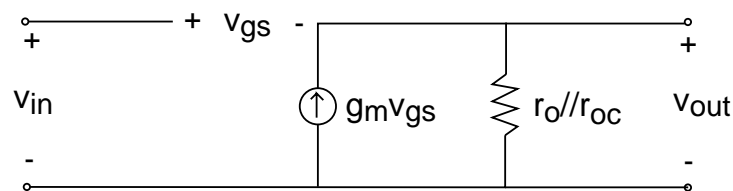
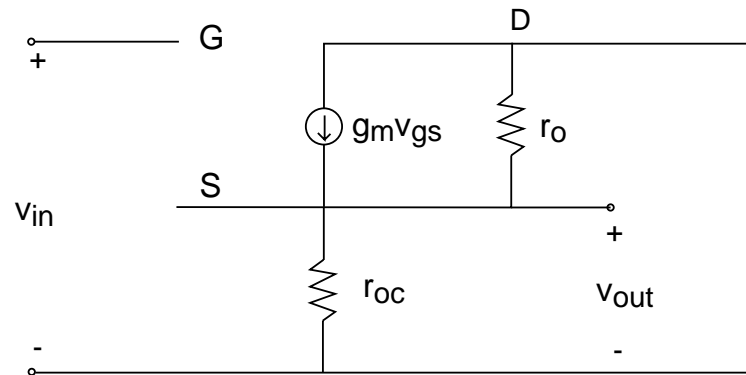


How does it work?

- V_{GG} , I_{SUP} , and W/L selected to bias MOSFET in saturation, obtain desired output bias point, and desired output swing.
- $v_G \uparrow \Rightarrow i_D$ can't change $\Rightarrow v_{OUT} \uparrow$
(*source follower*)
- to first order, no voltage gain: $v_{out} \simeq v_s$
- but R_{out} small: effective *voltage buffer* stage
(good for making voltage amp in combination with common-source stage).

□ *Small-signal analysis*

Unloaded small-signal equivalent circuit model:



$$v_{in} = v_{gs} + v_{out}$$

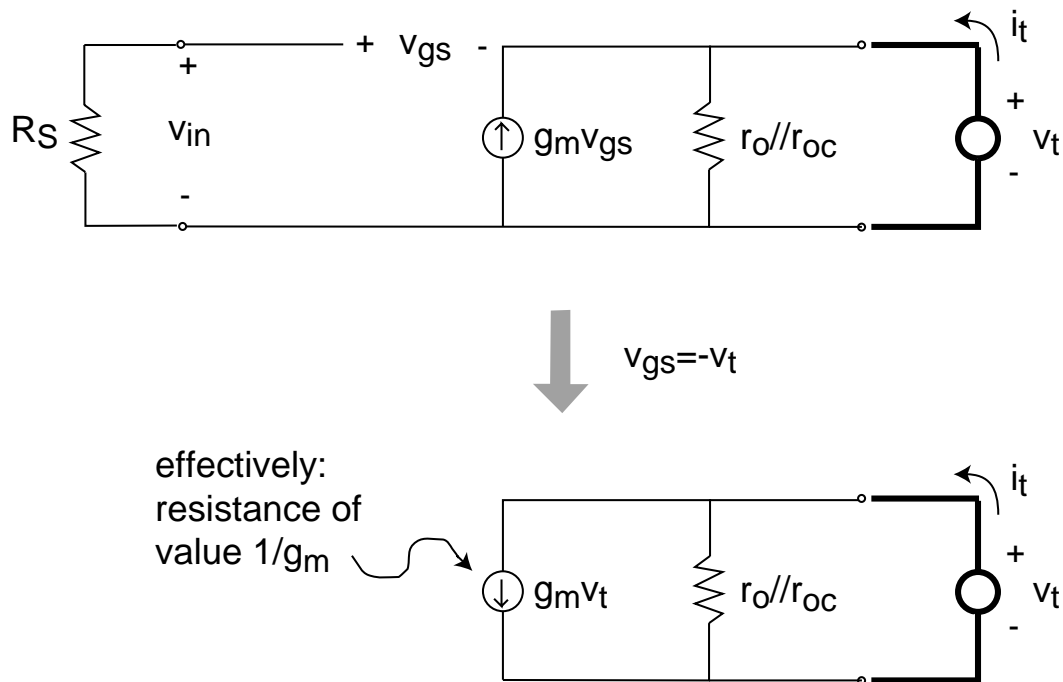
$$v_{out} = g_m v_{gs} (r_o // r_{oc})$$

Then:

$$A_{vo} = \frac{g_m}{g_m + \frac{1}{r_o // r_{oc}}} \simeq 1$$

Input impedance: $R_{in} = \infty$

Output impedance:



$$R_{out} = \frac{1}{g_m + \frac{1}{r_o // r_{oc}}} \simeq \frac{1}{g_m}$$

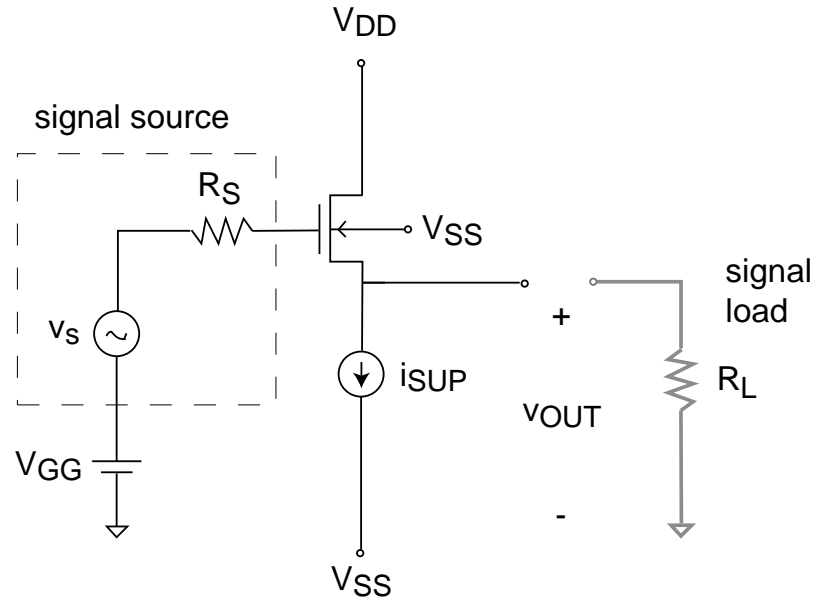
small!

Loaded voltage gain:

$$A_v = A_{vo} \frac{R_L}{R_L + R_{out}} \simeq \frac{R_L}{R_L + \frac{1}{g_m}} \simeq 1$$

□ Effect of back bias:

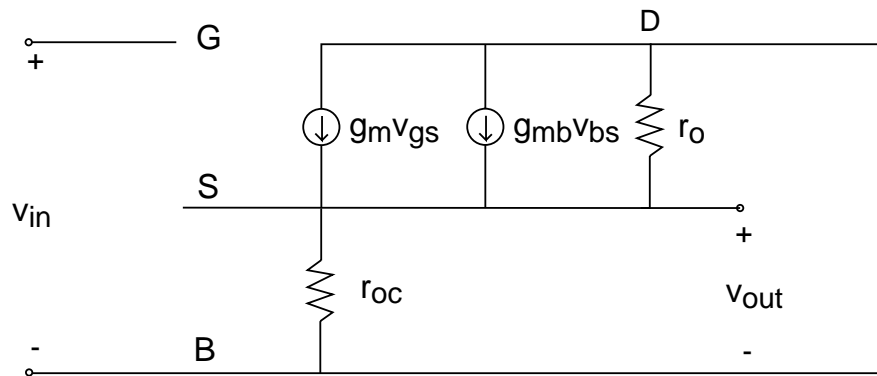
If MOSFET not fabricated on isolated p-well, then body is tied up to wafer substrate (connected to V_{SS}):



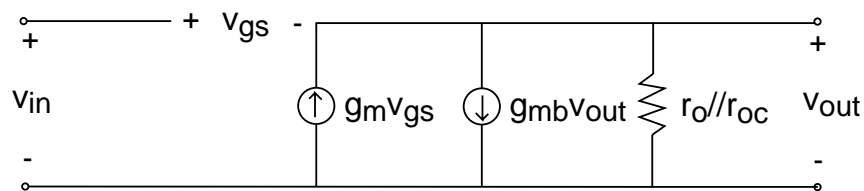
Two consequences:

- Bias affected: V_T depends on $V_{BS} = V_{SS} - V_{OUT} \neq 0$
- Small-signal figures of merit affected: signal shows up between B and S ($v_{bs} = -v_{out}$).

Small-signal equivalent circuit model:



$$V_{bs} = -V_{out}$$



$$A_{vo} = \frac{g_m}{g_m + g_{mb} + \frac{1}{r_o // r_{oc}}} \simeq \frac{g_m}{g_m + g_{mb}} < 1$$

Also:

$$R_{out} = \frac{1}{g_m + g_{mb} + \frac{1}{r_o // r_{oc}}} \simeq \frac{1}{g_m + g_{mb}}$$

□ Relationship between circuit figures of merit and device parameters:

$$g_m = \sqrt{2 \frac{W}{L} \mu_n C_{ox} I_D}$$

$$g_{mb} = \frac{\gamma}{2\sqrt{-2\phi_p - V_{BS}}} g_m$$

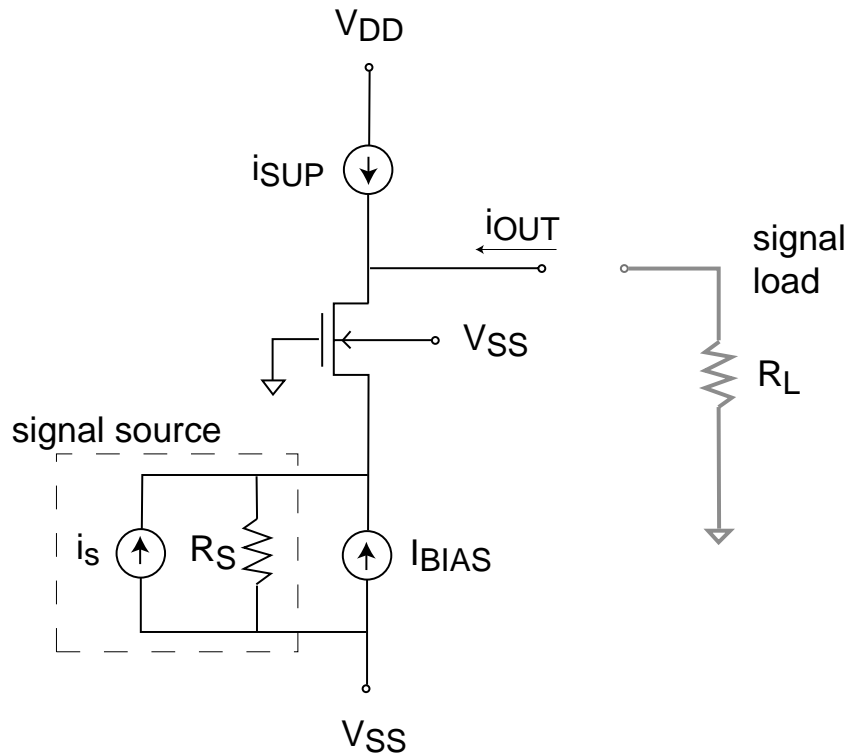
Device * Parameters	Circuit Parameters		
	$ A_{vo} $	R_{in}	R_{out}
	$\frac{g_m}{g_m + g_{mb}}$	∞	$\frac{1}{g_m + g_{mb}}$
$I_{SUP} \uparrow$	-	-	\downarrow
$W \uparrow$	-	-	\downarrow
$\mu_n C_{ox} \uparrow$	-	-	\downarrow
$L \uparrow$	-	-	\uparrow

* adjustments are made to V_{GG} so none of the other parameters change

CD amp useful as a *voltage buffer* to drive small loads (in a multistage amp, other stages will be used to provide voltage gain).

3. Common-gate amplifier

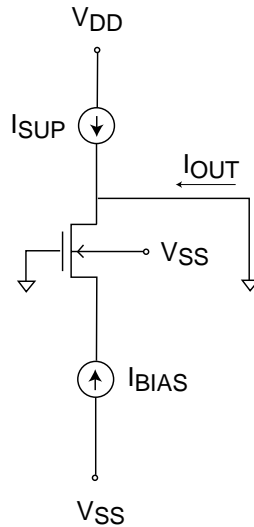
Need to handle current-mode signal sources:



How does it work?

- since source is signal input terminal, body cannot be tied up to source
- i_{SUP} , I_{BIAS} , and W/L selected to bias MOSFET in saturation, obtain desired output bias point, and desired output swing
- $i_s \uparrow \Rightarrow i_D \downarrow \Rightarrow i_{OUT} \downarrow$
- no current gain: $i_s = -i_{out}$ (*current buffer*)

□ *Bias*: select I_{SUP} , I_{BIAS} , and W/L to get proper quiescent I_{OUT} and keep MOSFET in saturation.



$$I_{SUP} + I_{OUT} + I_{BIAS} = 0$$

Select bias so that $I_{OUT} = 0 \Rightarrow V_{OUT} = 0$.

Assume MOSFET in saturation (no channel modulation):

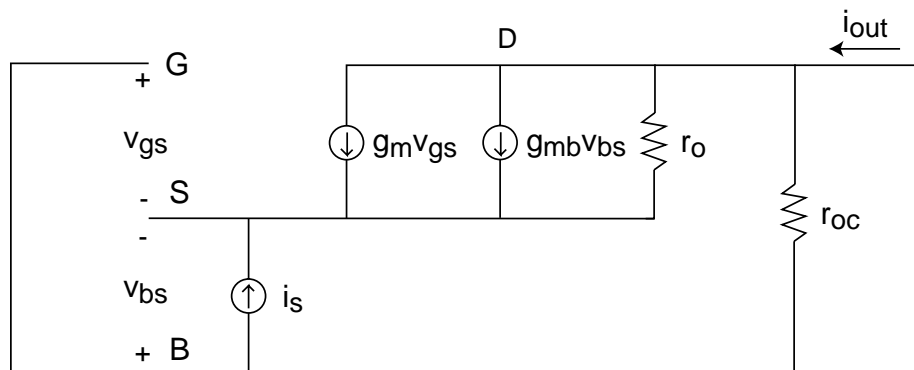
$$I_D = \frac{W}{2L} \mu_n C_{ox} (V_{GS} - V_T)^2 = I_{SUP} = -I_{BIAS}$$

but V_T depends on V_{BS} :

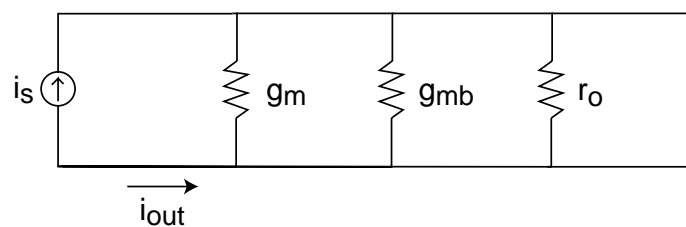
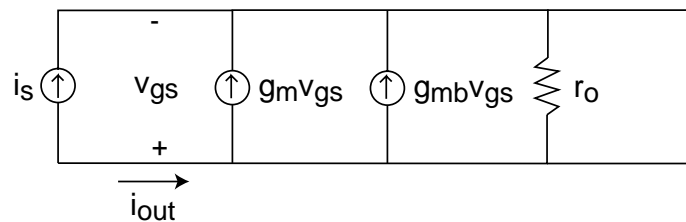
$$V_T = V_{To} + \gamma_n (\sqrt{-2\phi_p - V_{BS}} - \sqrt{-2\phi_p})$$

Must solve these two equations iteratively to get V_S .

□ *Small-signal circuit* (unloaded)



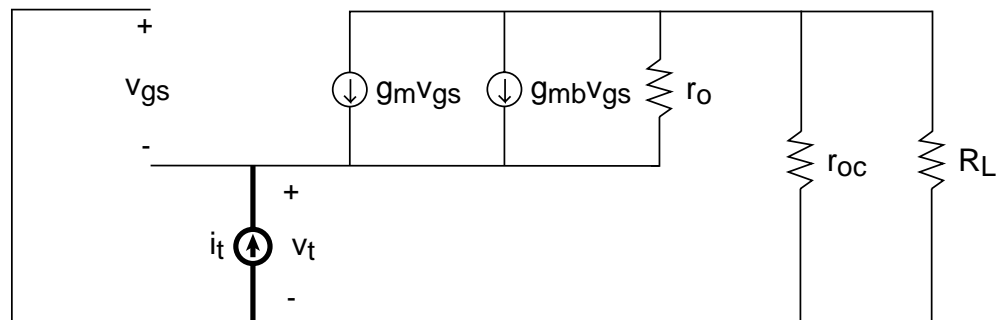
$$v_{bs} = v_{gs}$$



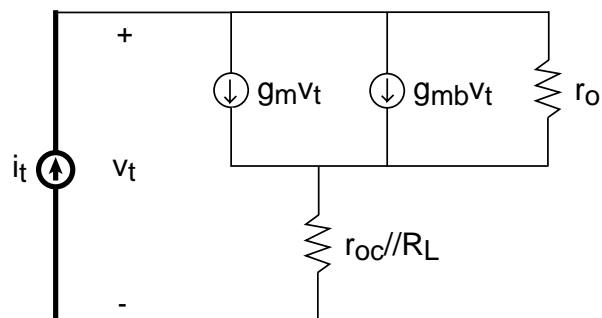
$$i_s = -i_{out} \Rightarrow A_{io} = -\frac{i_{out}}{i_s} = -1$$

Not surprising, since in a MOSFET: $i_g = 0$.

Input resistance:



$$v_{gs} = -v_t$$



Do KCL on input node:

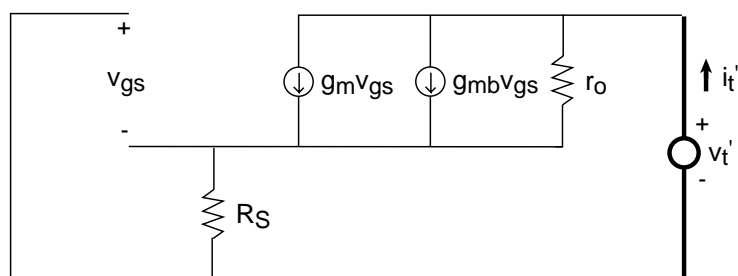
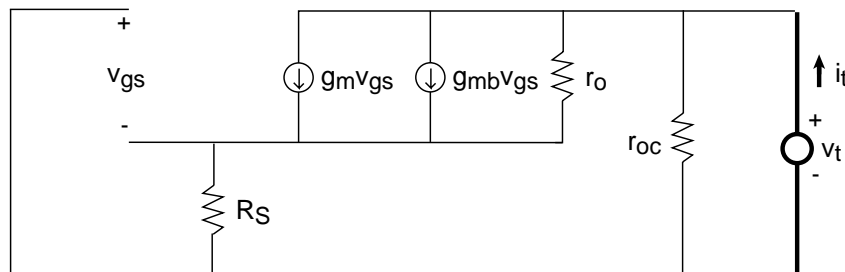
$$i_t - g_m v_t - g_{mb} v_t - \frac{v_t - (r_{oc} // R_L) i_t}{r_o} = 0$$

Then:

$$R_{in} = \frac{1 + \frac{r_{oc} // R_L}{r_o}}{g_m + g_{mb} + \frac{1}{r_o}} \simeq \frac{1}{g_m + g_{mb}}$$

Very small.

Output resistance:



Do KCL on input node:

$$i_t' - g_m v_{gs} - g_{mb} v_{gs} - \frac{v_t' + v_{gs}}{r_o} = 0$$

Notice also:

$$v_{gs} = -i_t' R_S$$

Then:

$$R_{out} = r_{oc} // \left\{ r_o \left[1 + R_S \left(g_m + g_{mb} + \frac{1}{r_o} \right) \right] \right\} \simeq r_{oc} // [r_o (1 + g_m R_S)]$$

Very large, because of the feedback effect of R_S .

Summary of MOSFET amplifier stages:

stage	A_{vo}, G_{mo}, A_{io}	R_{in}	R_{out}	key function
common source	$G_{mo} = g_m$	∞	$r_o // r_{oc}$	transconductance amp.
common drain	$A_{vo} \simeq \frac{g_m}{g_m + g_{mb}}$	∞	$\frac{1}{g_m + g_{mb}}$	voltage buffer
common gate	$A_{io} \simeq -1$	$\frac{1}{g_m + g_{mb}}$	$r_{oc} // [r_o(1 + g_m R_S)]$	current buffer

In order to design amplifiers with suitable performance, need to combine these stages \Rightarrow *multistage amplifiers*

Key conclusions

Different MOSFET stages designed to accomplish different goals:

- *Common-source stage:*
 - large voltage gain and transconductance, high input resistance, large output resistance
 - excellent transconductance amplifier, reasonable voltage amplifier
- *Common-drain stage:*
 - no voltage gain, but high input resistance and low output resistance
 - good voltage buffer
- *Common-gate stage:*
 - no current gain, but low input resistance and high output resistance
 - good current buffer