Lecture 11

Digital Circuits (I)

THE INVERTER

Outline

• Introduction to digital circuits
  – The inverter
• NMOS inverter with resistor pull-up

Reading Assignment:
Howe and Sodini; Chapter 5, Sections 5.1-5.3
1. Introduction to digital circuits: the inverter

In digital circuits, digitally-encoded information is represented by means of two distinct voltage ranges:

- **Logic 0:** $V_{\text{MIN}} \leq V \leq V_{\text{OL}}$
- **Logic 1:** $V_{\text{OH}} \leq V \leq V_{\text{MAX}}$
- **Undefined logic value:** $V_{\text{OL}} \leq V \leq V_{\text{OH}}$

**The Static Definition**

- **Logic 0:** $V_{\text{MIN}} \leq V \leq V_{\text{OL}}$
- **Logic 1:** $V_{\text{OH}} \leq V \leq V_{\text{MAX}}$
- **Undefined logic value:** $V_{\text{OL}} \leq V \leq V_{\text{OH}}$

Logic operations are performed using *logic gates*.

Simplest logic operation of all: *inversion* $\Rightarrow$ inverter
Ideal inverter

\[ V_M \equiv \text{input voltage for which } V_{\text{OUT}} = V_{\text{IN}} \]

- For \( 0 \leq V_{\text{IN}} < V_M \) \( \Rightarrow V_{\text{OUT}} = V^+ \)
- For \( V_M < V_{\text{IN}} \leq V^+ \) \( \Rightarrow V_{\text{OUT}} = 0 \)

Define \textit{switching point} or \textit{logic threshold}:

Circuit representation and ideal transfer function:

Ideal inverter returns well defined logical outputs (0 or \( V^+ \)) even in the presence of considerable noise in \( V_{\text{IN}} \) (from voltage spikes, crosstalk, etc.) \( \Rightarrow \) signal is \textit{regenerated}!
“Real” inverter

In a real inverter, valid logic levels defined as follows:

- **Logic 0:**
  - $V_{\text{MIN}}$ ≡ output voltage for which $V_{\text{IN}} = V^+$
  - $V_{\text{OL}}$ ≡ smallest output voltage where slope = -1
- **Logic 1:**
  - $V_{\text{OH}}$ ≡ largest output voltage where slope = -1
  - $V_{\text{MAX}}$ ≡ output voltage for which $V_{\text{IN}} = 0$
Two other important voltages:

Define:

\[ V_{IL} \equiv \text{smallest input voltage where slope} = -1 \]

\[ V_{IH} \equiv \text{highest input voltage where slope} = -1 \]

If range of output values \( V_{OL} \) to \( V_{OH} \) is \underline{wider} than the range of input values \( V_{IL} \) to \( V_{IH} \), then the inverter exhibits some noise immunity. \((|\text{Voltage gain}| > 1)\)

Quantify this through \underline{noise margins}.\]
Define *noise margins*:

\[
\begin{align*}
NM_H & \equiv V_{OH} - V_{IH} & \text{noise margin high} \\
NM_L & \equiv V_{IL} - V_{OL} & \text{noise margin low}
\end{align*}
\]
Simplifications for hand calculations: Logic levels and noise margins

It is hard to compute points in transfer function with slope = -1.

Approximate in the following way:

- Assume $V_{OL} \approx V_{MIN}$ and $V_{OH} \approx V_{MAX}$
- Trace tangent of transfer function at $V_M$
  - Slope = small signal voltage gain ($A_v$) at $V_M$
- $V_{IL} \approx$ intersection of tangent with $V_{OUT} = V_{MAX}$
- $V_{IH} \approx$ intersection of tangent with $V_{OUT} = V_{MIN}$
Transient Characteristics

Inverter switching in the time domain:

\[ t_R \equiv \text{rise time} \quad \text{between 10\% and 90\% of total swing} \]
\[ t_F \equiv \text{fall time} \quad \text{between 90\% and 10\% of total swing} \]
\[ t_{PHL} \equiv \text{propagation delay from high-to-low} \quad \text{between 50\% points} \]
\[ t_{PLH} \equiv \text{propagation delay from low-to-high} \quad \text{between 50\% points} \]

Propagation delay:

\[ t_P = \frac{1}{2}(t_{PHL} + t_{PLH}) \]
Simplifications for hand calculations: 
Propagation delay

- Consider input waveform is an ideal square wave
- Propagation delay times = delay times to 50% point

**SPICE essential for accurate delay analysis**
2. NMOS inverter with “pull-up” resistor

Essential features:
- $V_{BS} = 0$ (typically not shown)
- $C_L$ summarizes capacitive loading of the following stages (other logic gates, interconnect lines, etc.)

Basic Operation:
- If $V_{IN} < V_T$, MOSFET is OFF
  - $\Rightarrow V_{OUT} = V_{DD}$
- If $V_{IN} > V_T$, MOSFET is ON
  - $\Rightarrow V_{OUT}$ small
  - Value set by resistor / nMOS divider
Transfer function obtained by solving:

\[ I_R = I_D \]

Can solve graphically: I–V characteristics of load:
Overlap I–V characteristics of resistor pull-up on I–V characteristics of transistor:

Transfer function:
For $V_{\text{MAX}}$, transistor is cut-off, $I_D = 0$:

$$V_{\text{MAX}} = V_{DD}$$

For $V_{\text{MIN}}$, transistor is in linear regime; solve:

$$I_D = \frac{W}{L} \mu_n C_{\text{ox}} \left( V_{DD} - \frac{V_{\text{MIN}}}{2} - V_T \right) \Rightarrow V_{\text{MIN}} = I_R = \frac{V_{DD} - V_{\text{MIN}}}{R}$$

For $V_M$, transistor is in saturation; solve:

$$I_D = \frac{W}{2L} \mu_n C_{\text{ox}} (V_M - V_T)^2 = I_R = \frac{V_{DD} - V_M}{R}$$
Noise Margins:

Small signal equivalent circuit model at $V_M$ (transistor in saturation):

$$A_v = \frac{V_{out}}{V_{in}} = -g_m \left( r_o // R \right) \approx -g_m R$$
What did we learn today?

Summary of Key Concepts

• Logic circuits must exhibit immunity to noise in the input signal
  – *Noise margins*

• Logic circuits must be *regenerative*
  – Able to restore clean logic values even if input is noisy.

• *Propagation delay*: time for logic gate to perform its function.

• Concept of *load line*: graphical technique to visualize transfer characteristics of inverter.

• First-order solution (by hand) of inverter figures-of-merit easy if *regions of operation* of transistor are correctly identified.

• For more accurate solutions, use SPICE (or other CAD tool).