Lecture 6

PN Junction and MOS Electrostatics(III)

Outline

1. Introduction to MOS structure
2. Electrostatics of MOS in thermal equilibrium
3. Electrostatics of MOS with applied bias

Reading Assignment:
Howe and Sodini, Chapter 3, Sections 3.7-3.8
1. Introduction

Metal-Oxide-Semiconductor structure

MOS at the heart of the electronics revolution:

- Digital and analog functions
  - Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET) is key element of Complementary Metal-Oxide-Semiconductor (CMOS) circuit family

- Memory function
  - Dynamic Random Access Memory (DRAM)
  - Static Random Access Memory (SRAM)
  - Non-Volatile Random Access Memory (NVRAM)

- Imaging
  - Charge Coupled Device (CCD) and CMOS cameras

- Displays
  - Active Matrix Liquid Crystal Displays (AMLCD)
2. MOS Electrostatics in equilibrium

Idealized 1D structure:

- **Metal**: does not tolerate volume charge
  - ⇒ charge can only exist at its surface
- **Oxide**: insulator and does not have volume charge
  - ⇒ no free carriers, no dopants
- **Semiconductor**: can have volume charge
  - ⇒ Space charge region (SCR)

In thermal equilibrium we assume Gate contact is shorted to Bulk contact. (i.e, \( V_{GB} = 0 \text{V} \))
For most metals on p-Si, equilibrium achieved by electrons flowing from metal to semiconductor and holes from semiconductor to metal:

Remember: \( n_o p_o = n_i^2 \)

Fewer holes near Si / SiO\(_2\) interface

⇒ ionized acceptors exposed (volume charge)
Space Charge Density

- In semiconductor: space-charge region close Si / SiO₂ interface
  - can use depletion approximation
- In metal: sheet of charge at metal / SiO₂ interface
- Overall charge neutrality

\[
x = -t_{ox}; \\
-t_{ox} < x < 0; \\
0 < x < x_{do}; \\
x > x_{do};
\]

\[
\sigma = Q_G \\
\rho_o(x) = 0 \\
\rho_o(x) = -qN_a \\
\rho_o(x) = 0
\]
Electric Field

Integrate Poisson’s equation

\[ E_o(x_2) - E_o(x_1) = \frac{1}{\varepsilon} \int_{x_1}^{x_2} \rho(x') \, dx' \]

At interface between oxide and semiconductor, there is a change in permittivity ⇒ change in electric field

\[ \varepsilon_{ox} E_{ox} = \varepsilon_s E_s \]

\[ \frac{E_{ox}}{E_s} = \frac{\varepsilon_s}{\varepsilon_{ox}} \approx 3 \]
Start integrating from deep inside semiconductor:

\[ x > x_{do}; \quad E_o(x) = 0 \]

\[ 0 < x < x_{do}; \quad E_o(x) - E_o(x_{do}) = \frac{1}{\varepsilon_s} \int_{x_{do}}^{x} -qN_a \, dx' = -\frac{qN_a}{\varepsilon_s} (x - x_{do}) \]

\[ -t_{ox} < x < 0; \quad E_o(x) = \frac{\varepsilon_s}{\varepsilon_{ox}} E_o(x = 0^+) = \frac{qN_a x_{do}}{\varepsilon_{ox}} \]

\[ x < -t_{ox}; \quad E(x) = 0 \]
Electrostatic Potential
(with $\phi = 0$ @ $n_o = p_o = n_i$)

$$\phi = \frac{kT}{q} \cdot \ln \frac{n_o}{n_i} \quad \phi = -\frac{kT}{q} \cdot \ln \frac{p_o}{n_i}$$

In QNRs, $n_o$ and $p_o$ are known $\Rightarrow$ can determine $\phi$

in p-QNR: $p_o = N_a \Rightarrow \phi_p = -\frac{kT}{q} \cdot \ln \frac{N_a}{n_i}$

in $n^+$-gate: $n_o = N_d^+ \Rightarrow \phi_g = \phi_{n^+}$

Built-in potential:

$$\phi_B = \phi_g - \phi_p = \phi_{n^+} + \frac{kT}{q} \cdot \ln \frac{N_a}{n_i}$$
To obtain $\phi_o(x)$, integrate $E_o(x)$; start from deep inside semiconductor bulk:

$$\phi_o(x_2) - \phi_o(x_1) = -\int_{x_1}^{x_2} E_o(x') \, dx'$$

$x > x_{do}$;

$$\phi_o(x) = \phi_p$$

$0 < x < x_{do}$;

$$\phi_o(x) - \phi_o(x_{do}) = -\int_{x_{do}}^x \frac{qN_a}{\varepsilon_s} (x' - x_{do}) \, dx'$$

$$\phi_o(x) = \phi_p + \frac{qN_a}{2\varepsilon_s} (x - x_{do})^2$$

$AT \quad x = 0 \quad \phi_o(x) = \phi_p + \frac{qN_a}{2\varepsilon_s} (x_{do})^2$

$-t_{ox} < x < 0$;

$$\phi_o(x) = \phi_p + \frac{qN_a x_{do}^2}{2\varepsilon_s} + \frac{qN_a x_{do}}{\varepsilon_{ox}} (-x)$$

$x < -t_{ox}$;

$$\phi_o(x) = \phi_n$$

Almost done ....
Still do not know $x_{do} \Rightarrow$ need one more equation

Potential difference across structure has to add up to $\phi_B$:

$$\phi_B = V_{B,o} + V_{ox,o} = \frac{qN_a x_{do}^2}{2\varepsilon_s} + \frac{qN_a x_{do} t_{ox}}{\varepsilon_{ox}}$$

Solve quadratic equation:

$$x_{do} = \frac{\varepsilon_s}{\varepsilon_{ox}} t_{ox} \left[ \sqrt{1 + \frac{2\varepsilon_{ox}^2 \phi_B}{q \varepsilon_s N_a t_{ox}^2}} - 1 \right]$$

$$= \frac{\varepsilon_s}{C_{ox}} \left[ \sqrt{1 + \frac{2 C_{ox}^2 \phi_B}{q \varepsilon_s N_a}} - 1 \right]$$

where $C_{ox}$ is the capacitance per unit area of oxide

$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}$$

Now problem is completely solved!
There are also contact potentials
⇒ total potential difference from contact to contact is zero!
3. MOS with applied bias $V_{GB}$

Apply voltage to gate with respect to semiconductor:

Electrostatics of MOS structure affected
⇒ potential difference across entire structure now ≠ 0

How is potential difference accommodated?
Potential difference shows up across oxide and SCR in semiconductor

Oxide is an insulator ⇒ no current anywhere in structure

In SCR, quasi-equilibrium situation prevails
⇒ New balance between drift and diffusion

- Electrostatics qualitatively identical to thermal equilibrium (but amount of charge redistribution is different)
- \( np = n_i^2 \)
Apply $V_{GB}>0$: potential difference across structure increases ⇒ need larger charge dipole ⇒ SCR expands into semiconductor substrate:

Simple way to remember:
with $V_{GB}>0$, gate attracts electrons and repels holes.
Qualitatively, physics unaffected by application of $V_{GB} > 0$. Use mathematical formulation in thermal equilibrium, but:

$$\phi_B \rightarrow \phi_B + V_{GB}$$

For example, to determine $x_d(V_{BG})$:

$$\phi_B + V_{GB} = V_B(V_{GB}) + V_{ox}(V_{GB})$$

$$= \frac{qN_a x_d^2(V_{GB})}{2\varepsilon_S} + \frac{qN_a x_d(V_{GB})t_{ox}}{\varepsilon_{ox}}$$

$$x_d(V_{GB}) = \frac{\varepsilon_S}{C_{ox}} \left[ \sqrt{1 + \frac{2C_{ox}^2 (\phi_B + V_{GB})}{\varepsilon_S qN_a}} - 1 \right]$$

$$\phi(0) = \phi_S = \phi_p + \frac{qN_a x_d^2(V_{GB})}{2\varepsilon_S}$$

$\phi_S$ gives n & p concentration at the surface
What did we learn today?

Summary of Key Concepts

• Charge redistribution in MOS structure in thermal equilibrium
  – SCR in semiconductor
  – ⇒ built-in potential across MOS structure.
• In most cases, we can use depletion approximation in semiconductor SCR
• Application of voltage modulates depletion region width in semiconductor
  – No current flows