

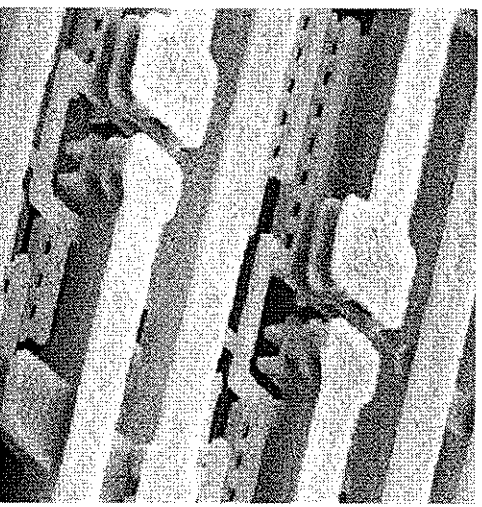
6.02 Lecture 2 - Wires and Models

(After notes and Examples)

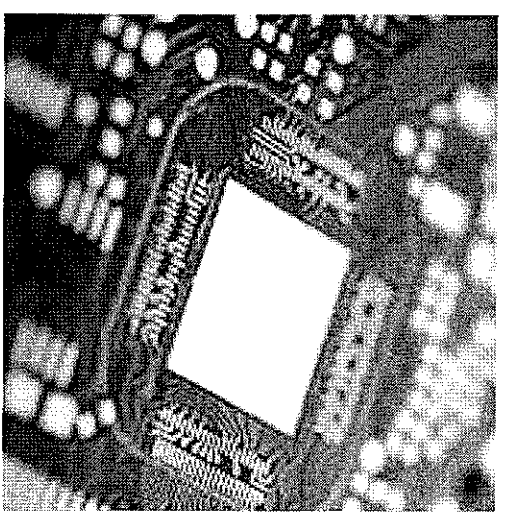
- **Non-Ideal Transmission**
 - Example wires and signal impact
 - Intersymbol Interference
 - Eye Diagrams
- **Modeling Wires**
 - Causality
 - Time-invariance
 - Linearity
- **SUPERPOSITION**
 - Demonstrating why it is so super

Types of Real "Wires"

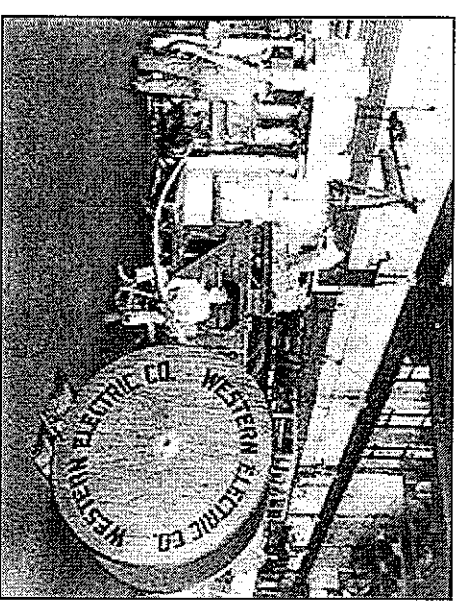
IC Interconnect



Printed Circuit Board



Transatlantic Cable

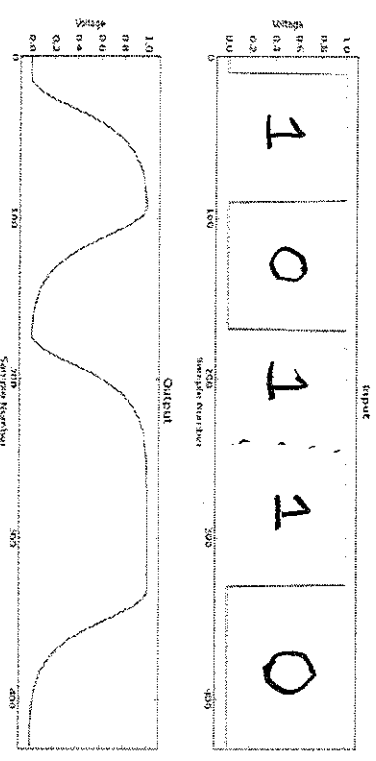


http://metrhdls.usask.ca/images/photos/SEMof31a.vic&Intercomp98_61F

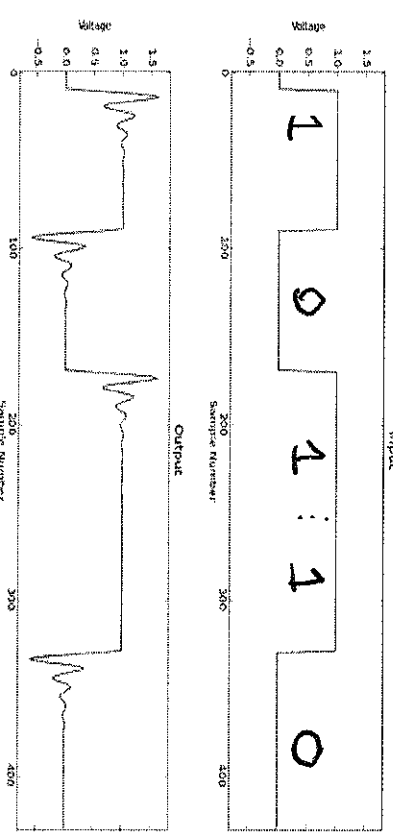
http://www.gpi-pcb.com/Files/Bilder/Fabrikier/chemholic/Chem_Pcb_hel.jpg

<http://www.satamerica.com/imgens/4a27897r1.jpg>

Slow Response



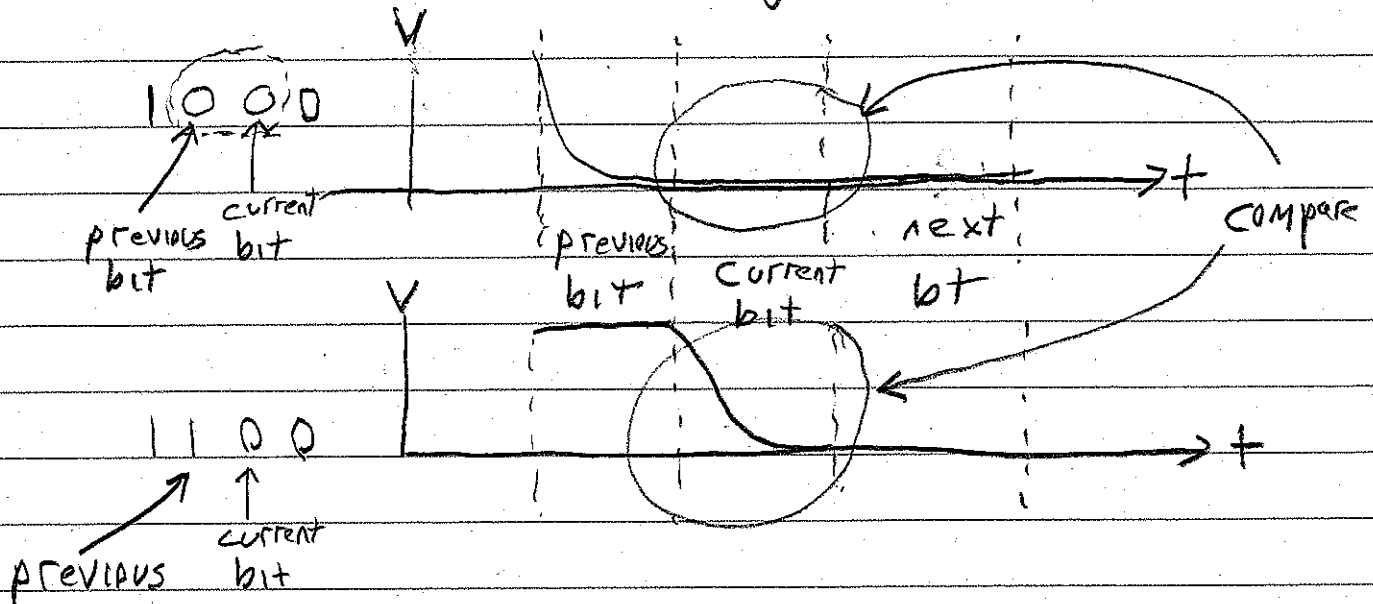
Ringling



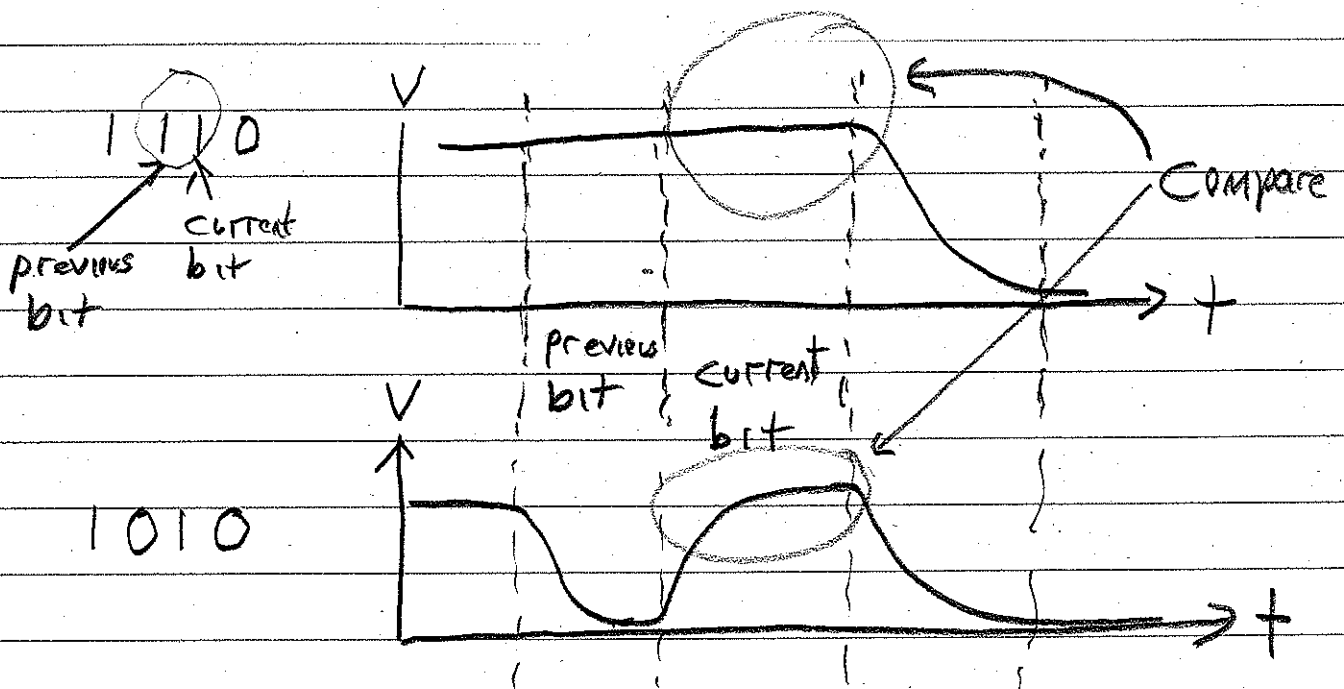
May also have long delays (Receiver does NOT know)

Intersymbol Interference - Slow Channel

- Consider Transmitting Two bits



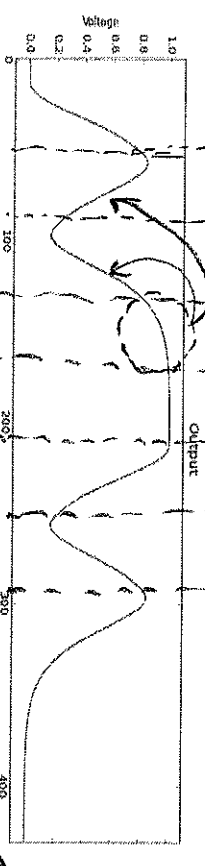
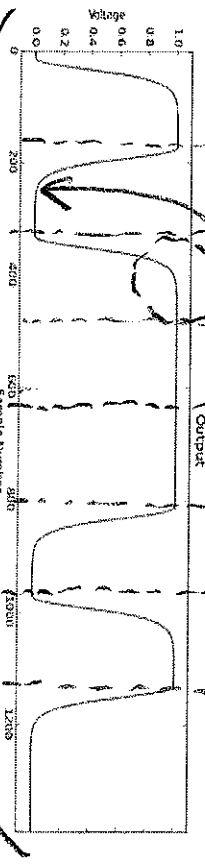
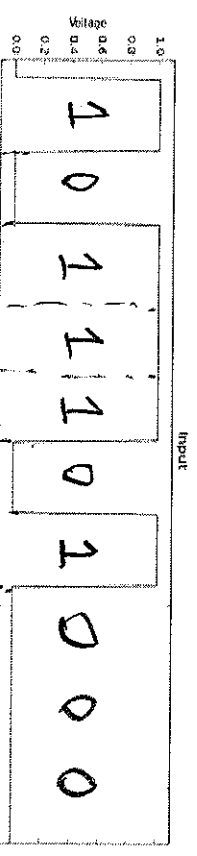
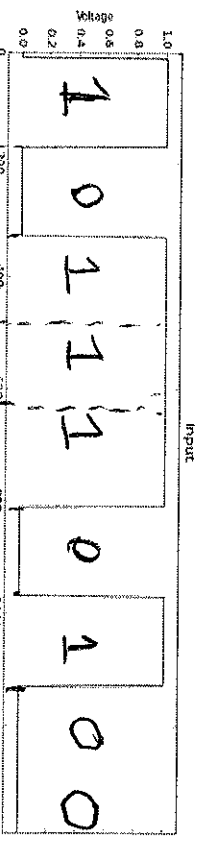
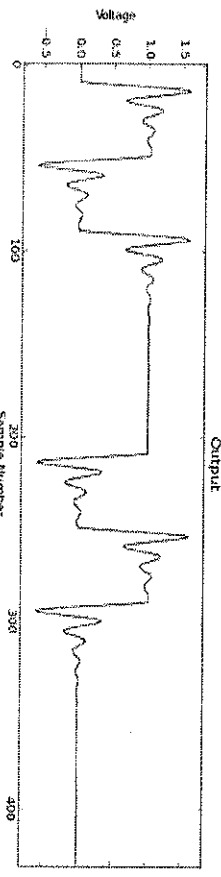
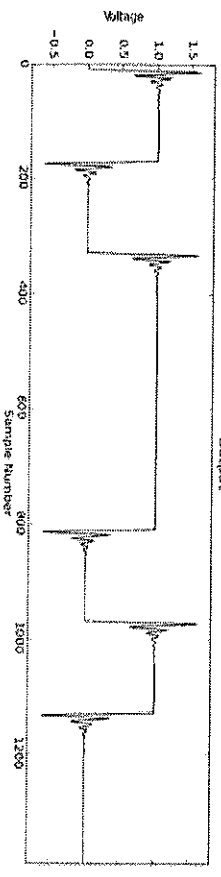
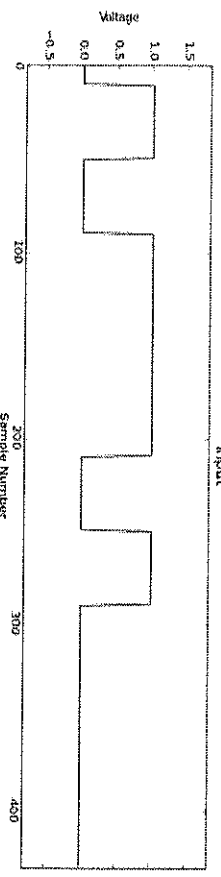
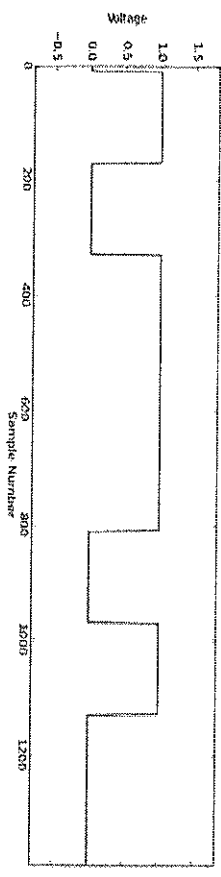
That the previous bit was a one "interferes" with the current bit being a zero



Previous bit = zero interferes with Current bit = 1

Intersymbol Interference

Long Bit Period (slow rate) Short Bit Period (Fast Rate)

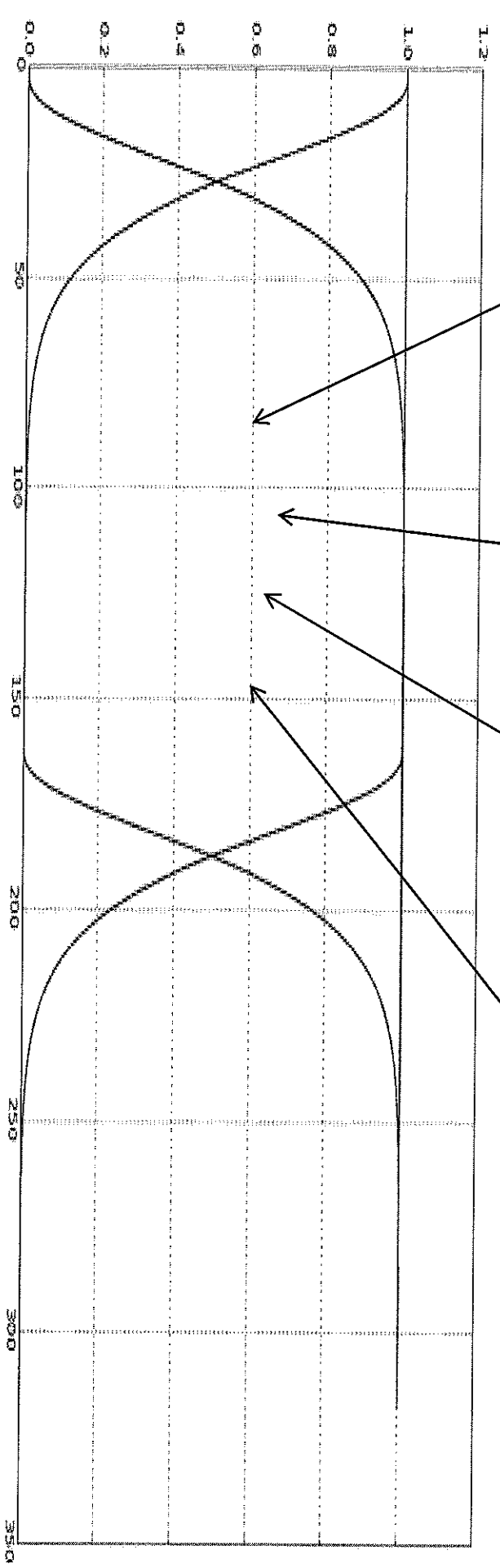
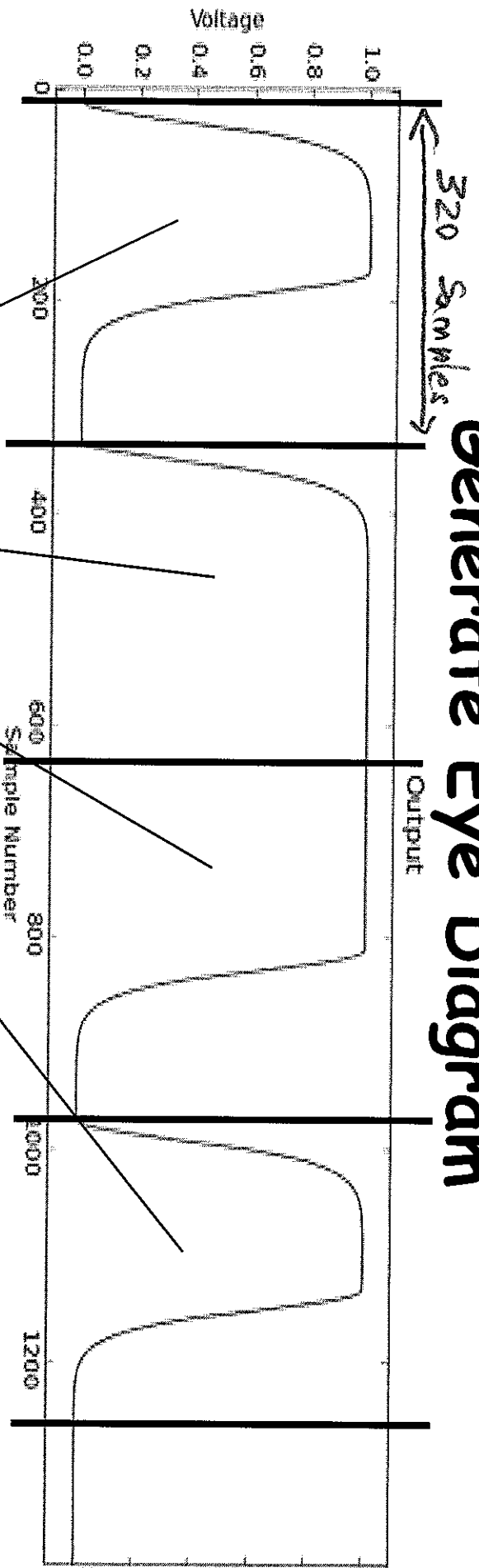


6.02 spring 2009

Only previous bit interferes

Previous two bits interfere.

Generate Eye Diagram



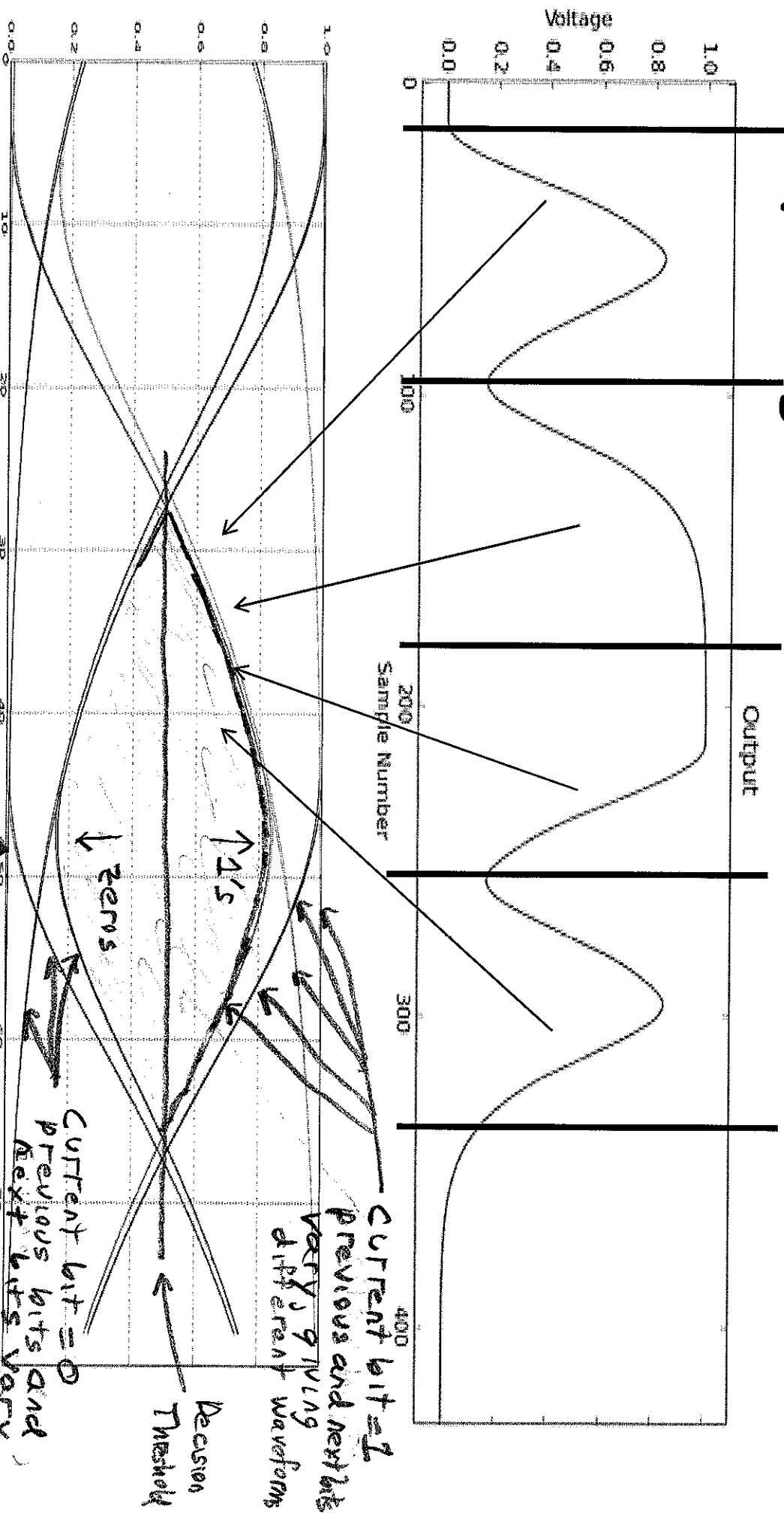
Eye Diagram Generated with 160 samples per bit

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Overlap voltage waveforms from every two-bit period section.

6

Eye Diagram for Shorter Bit Periods

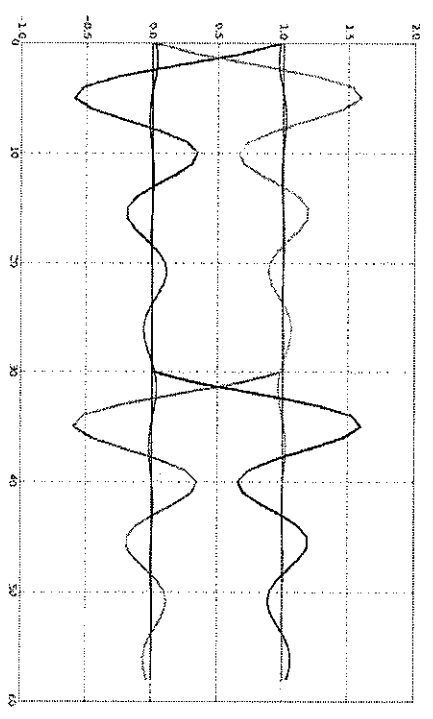


Eye diagram generated from 40 samples per bit and using a 200 bit long random sequence.

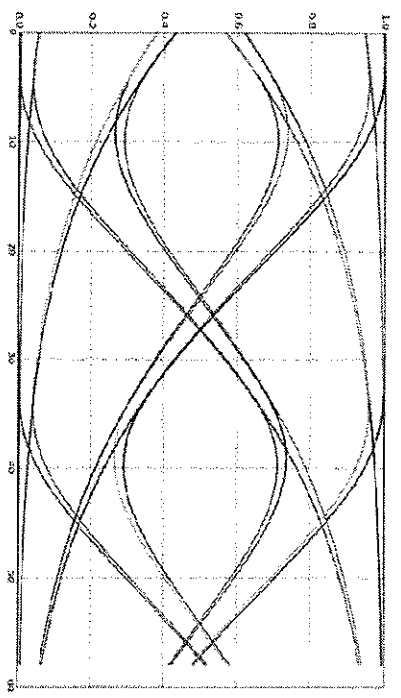
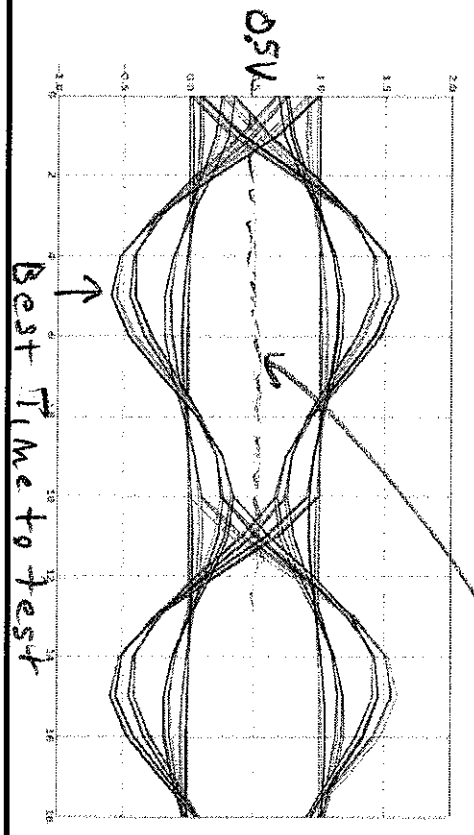
66

Eyes for Ringing versus Slow System

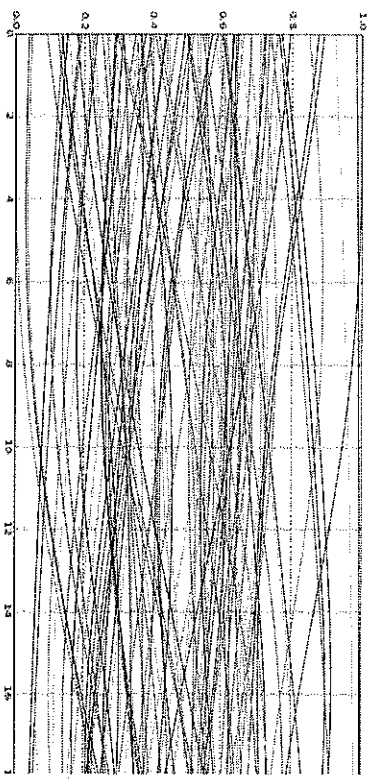
Medium Bit Period



Short Bit Period



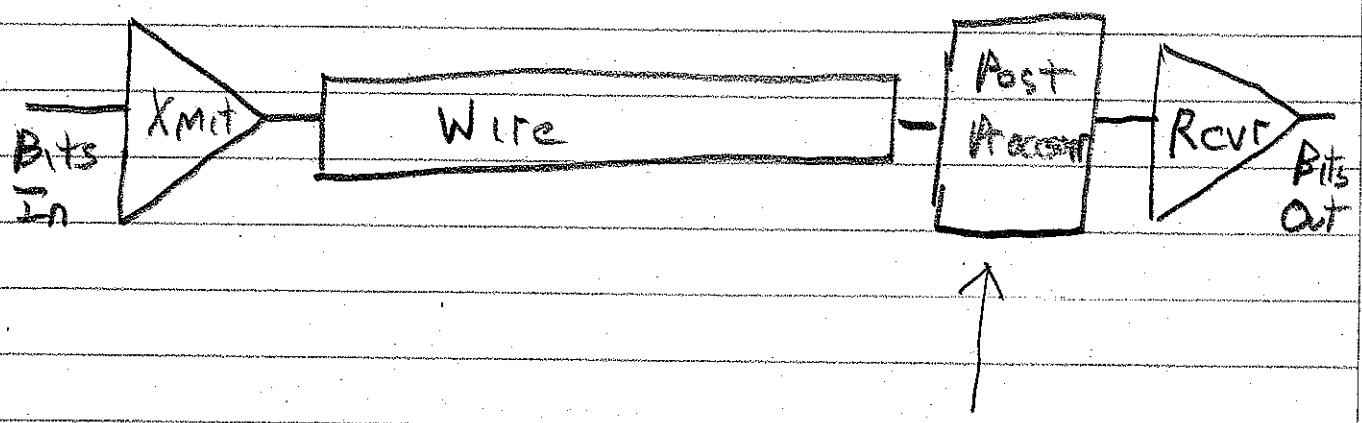
S
I
O
W



Non ideal Wires Create Intersymbol Interference

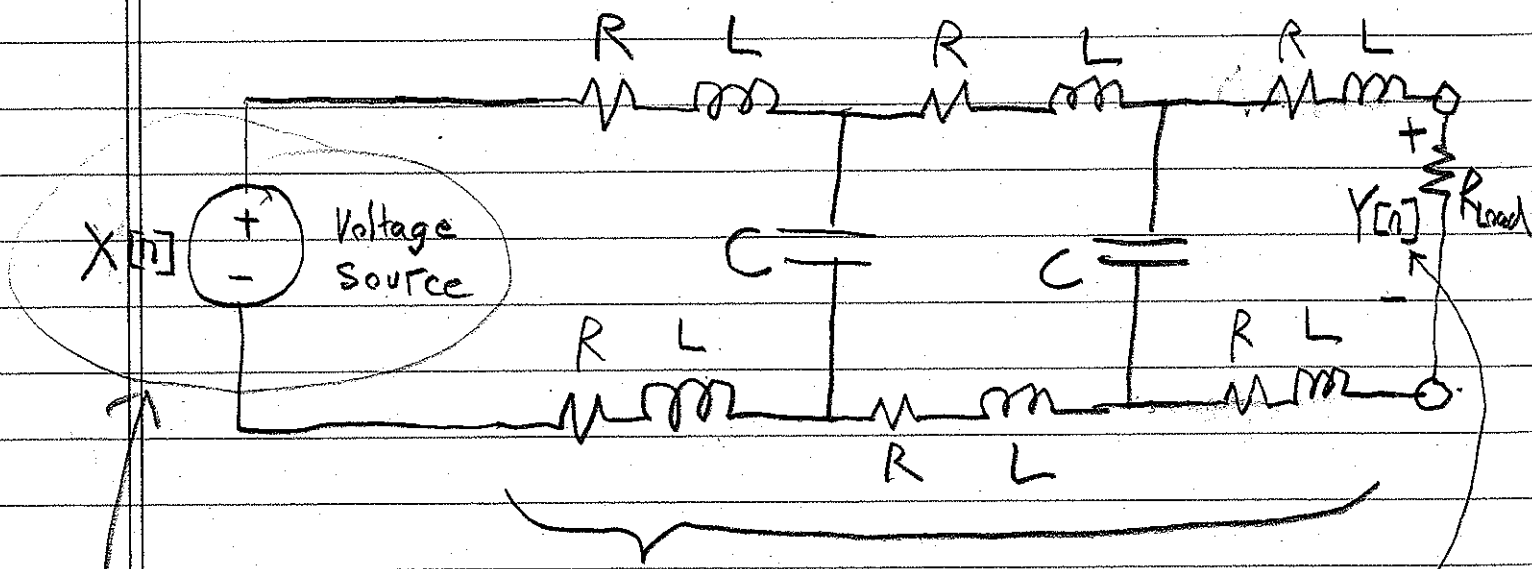
- Makes detecting bits more difficult
- Limits the bits/second that can be transmitted accurately.

Can we post-process the signal from the wire to improve performance?



Need a model of the wire to design a post-processor

Example Model of a Physical Wire

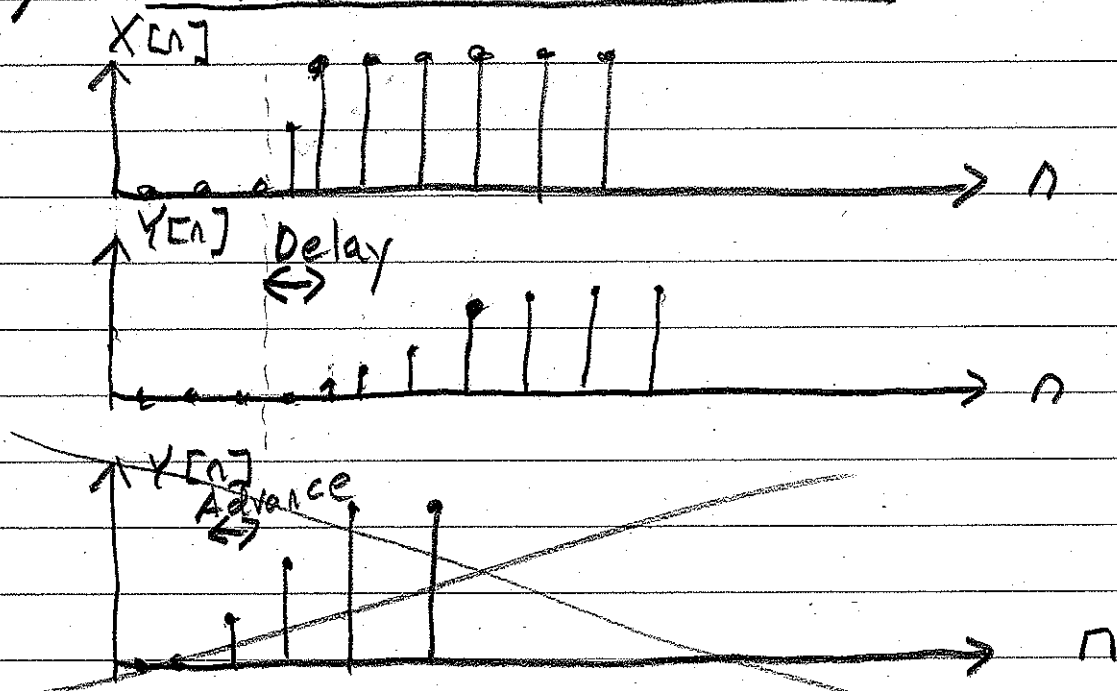


Transmitter Model

Circuit Model of Wire (Example)

Sampled Output

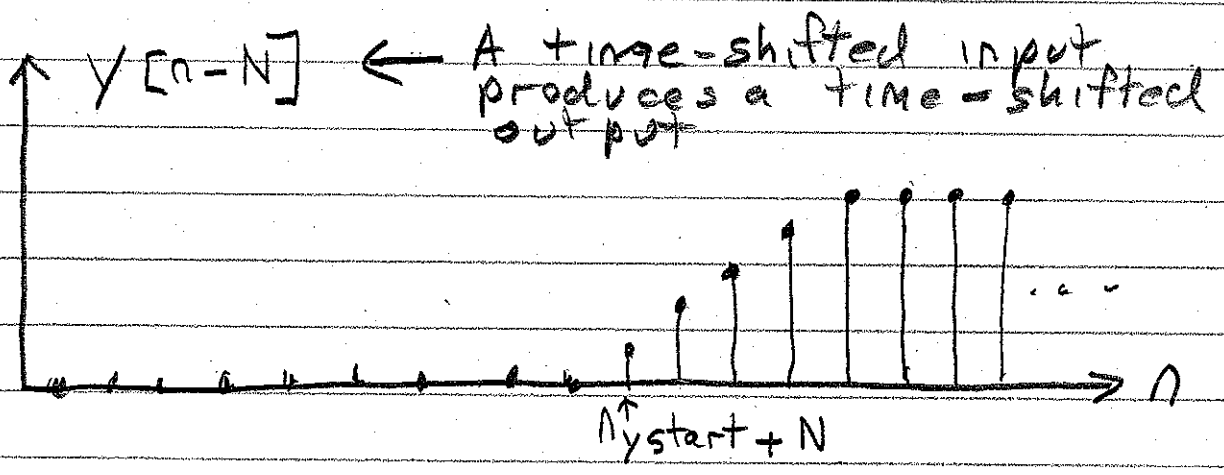
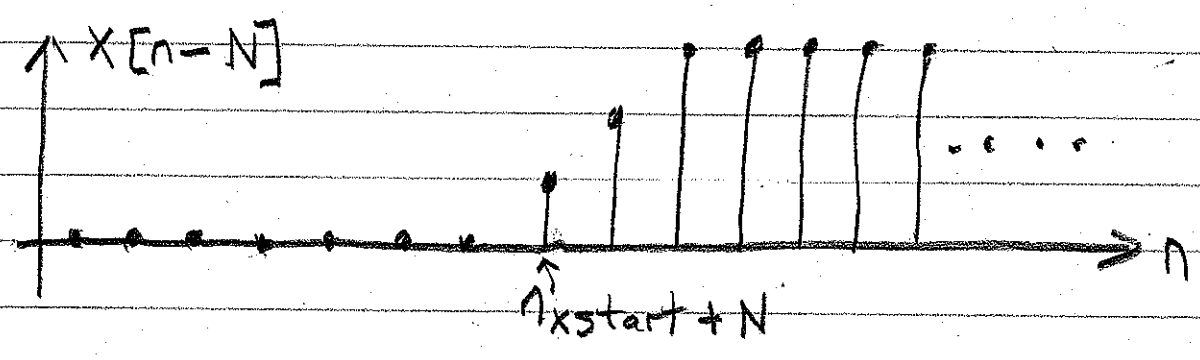
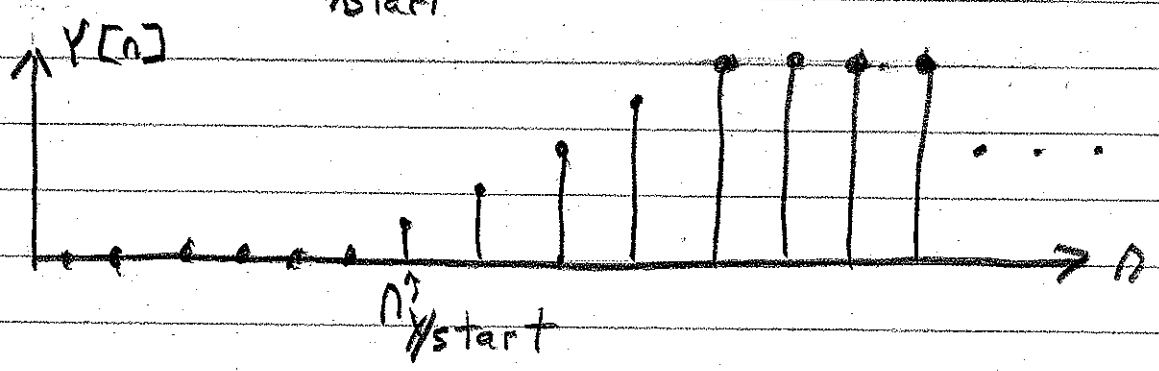
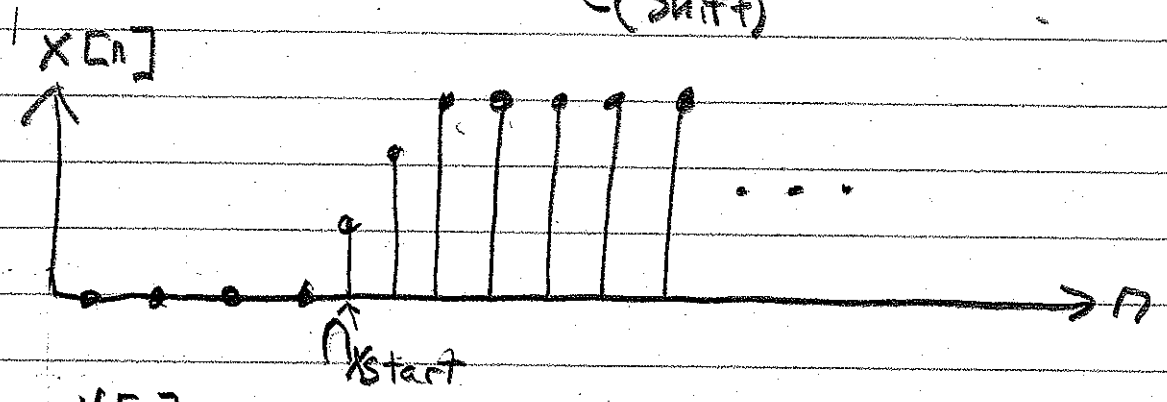
1) Wires are Causal



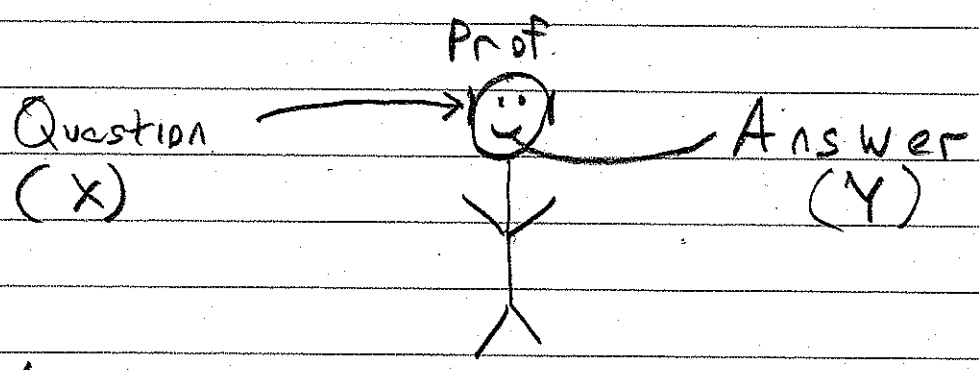
Wires can not predict the future!

A change in X causes a change in Y

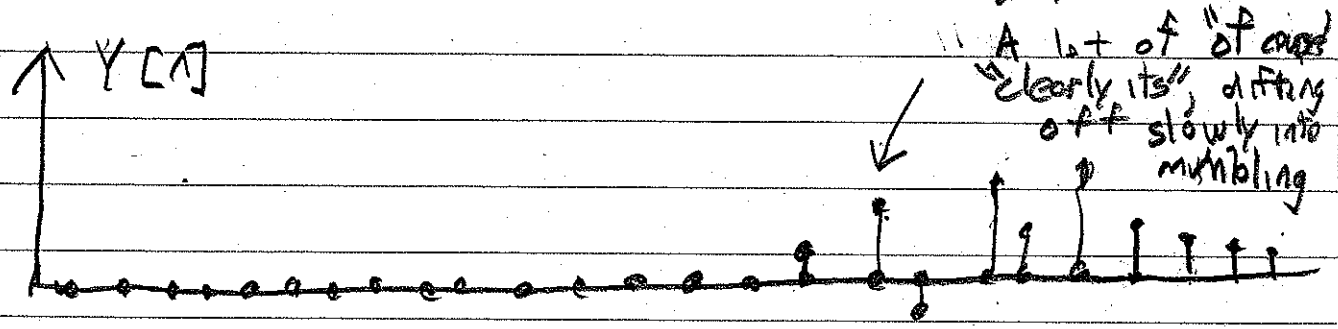
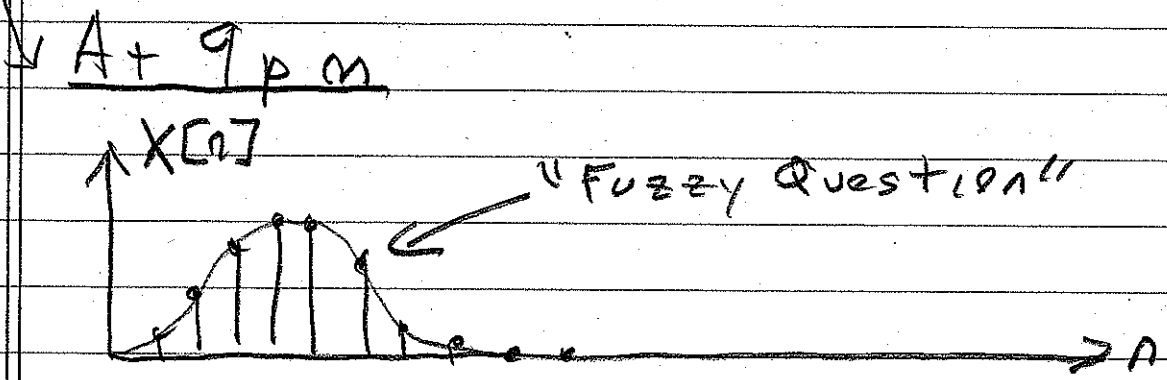
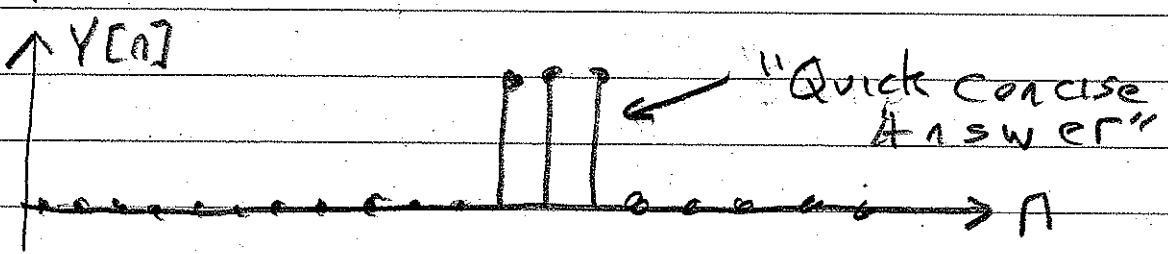
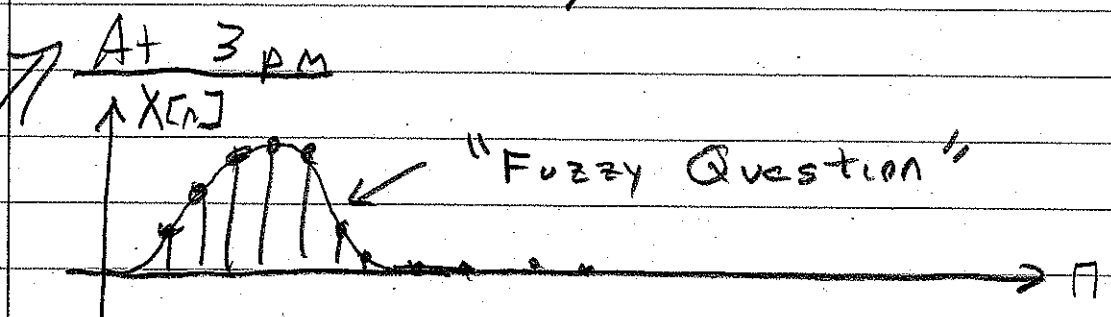
2) Wires are Time-Invariant (Shift)



A Non Time Invariant System

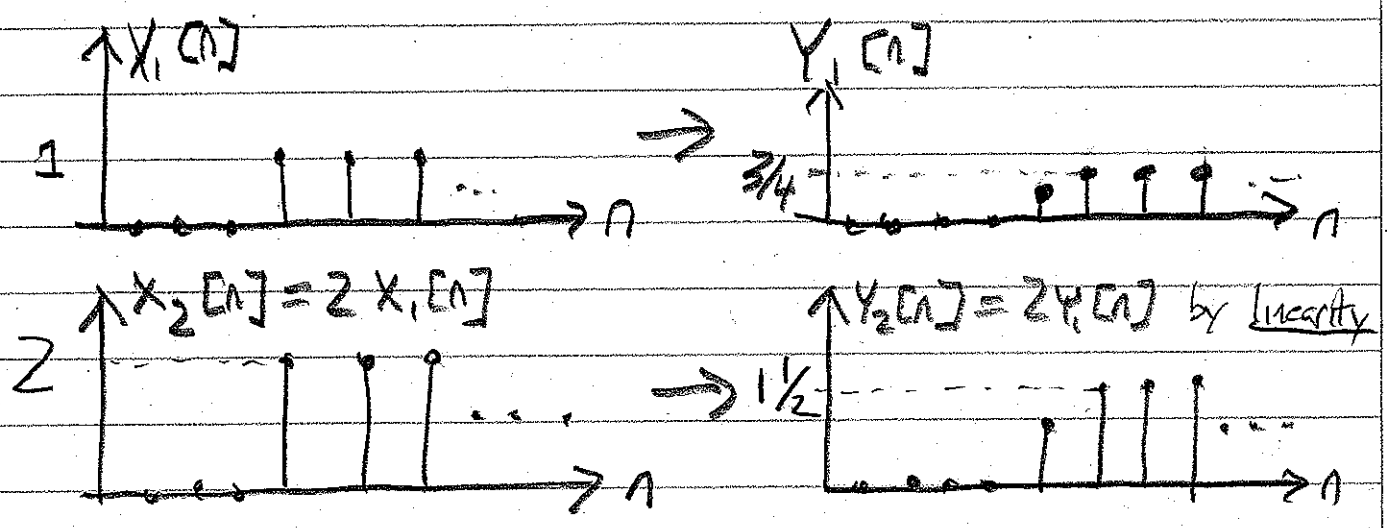


Time Varying System



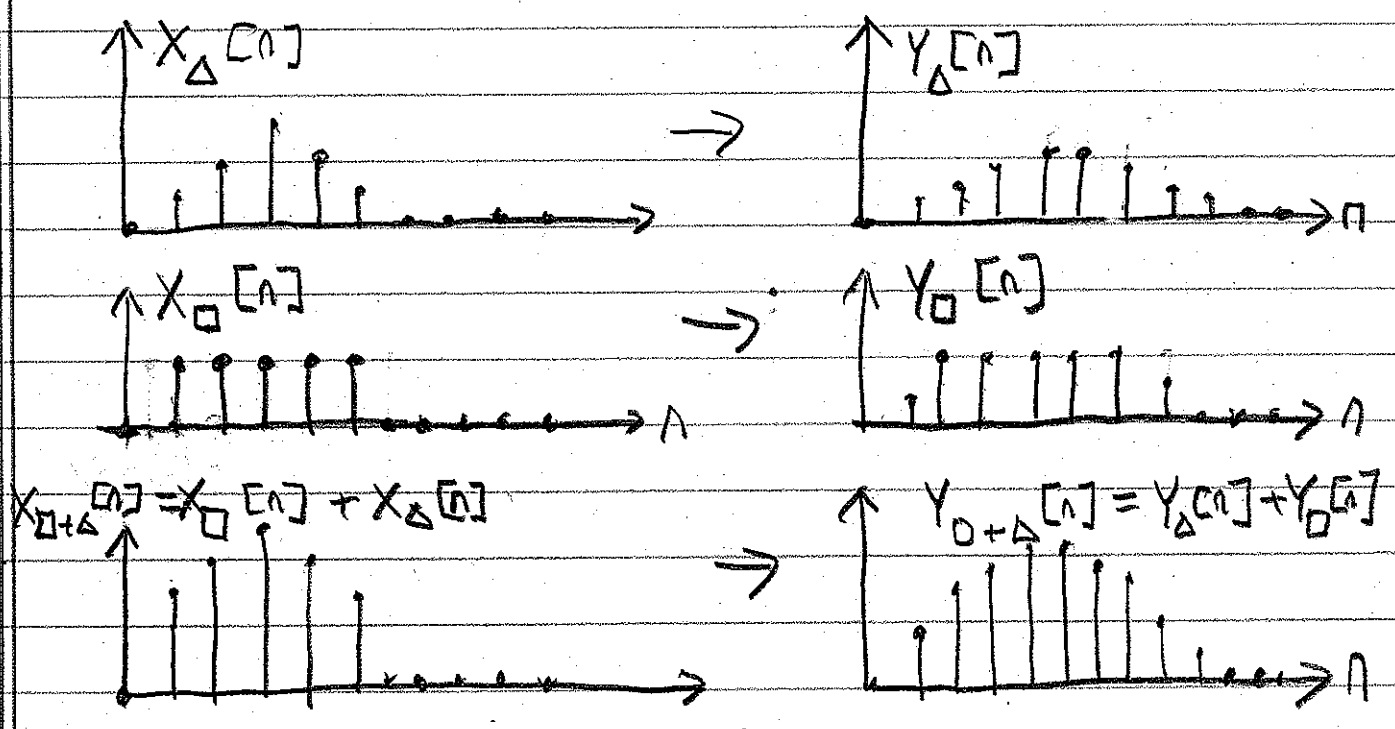
3) Linearity (A Strong Assumption!)

3a) Scaling



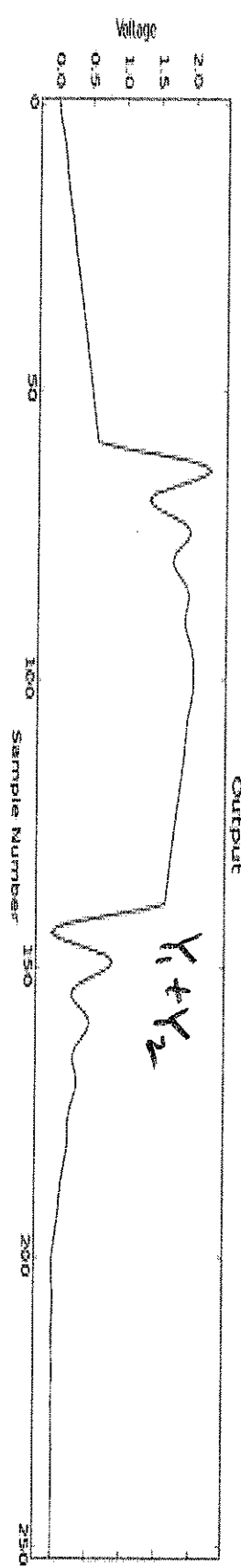
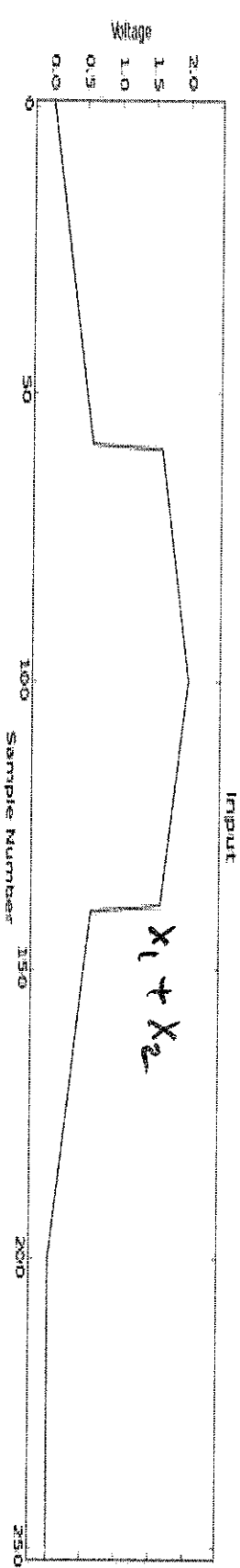
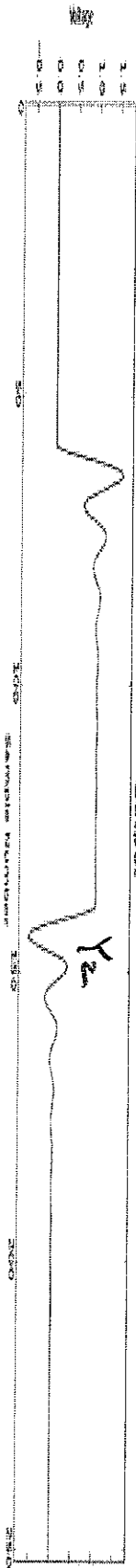
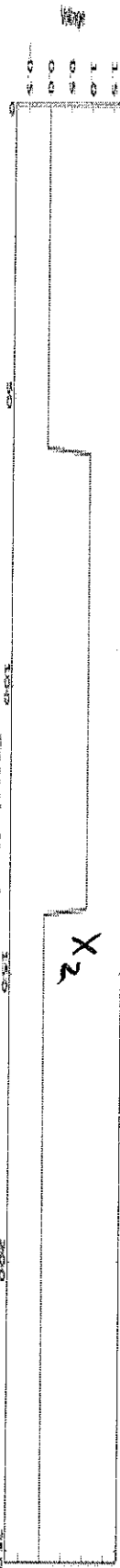
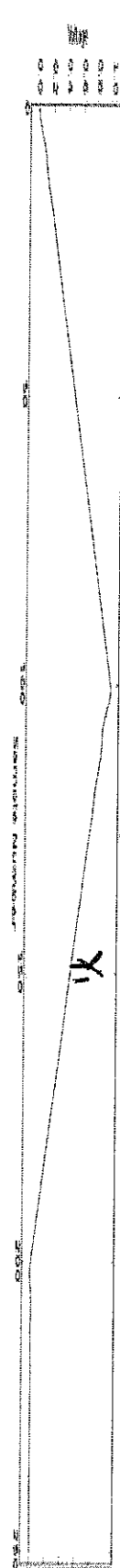
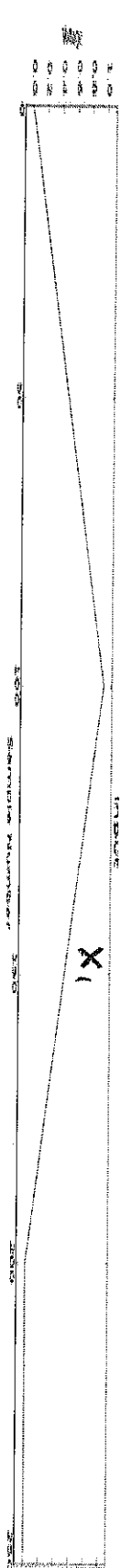
Scale Inputs \rightarrow Scaled Outputs

3b) Sum Inputs \rightarrow Sum Outputs



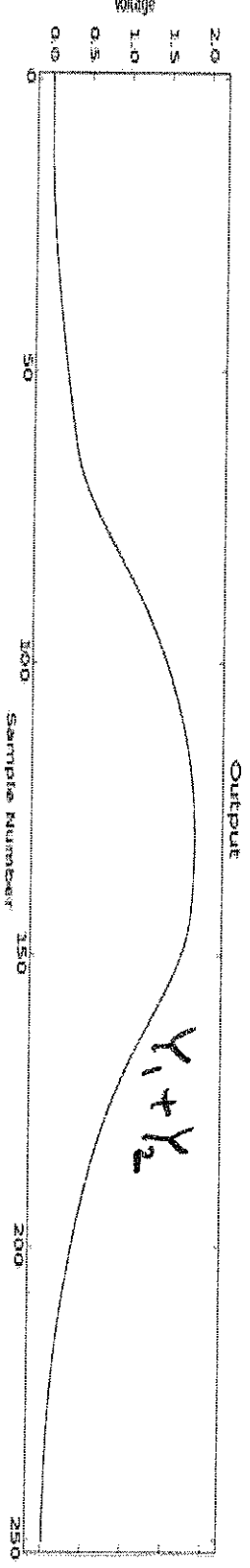
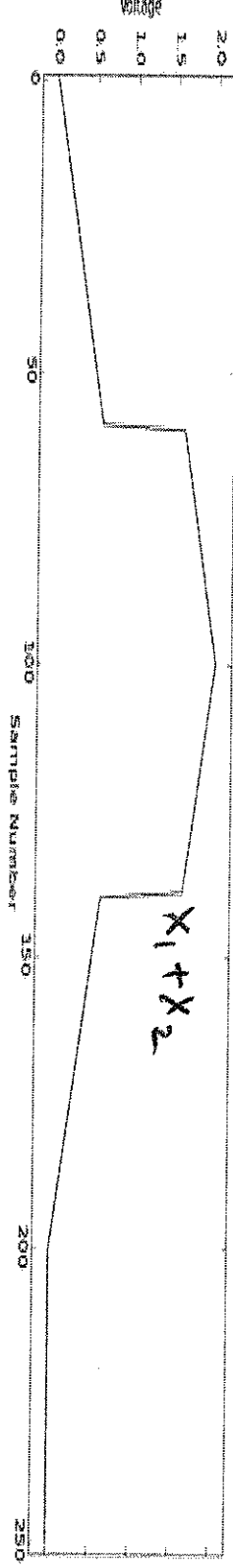
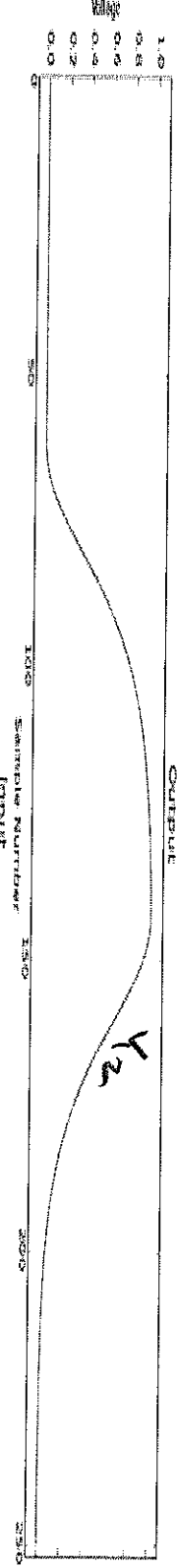
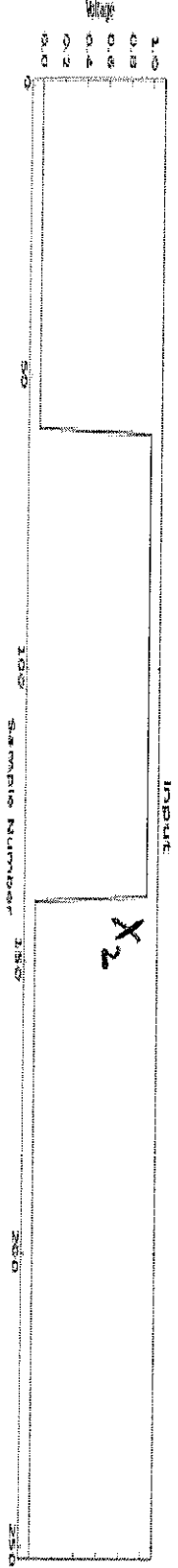
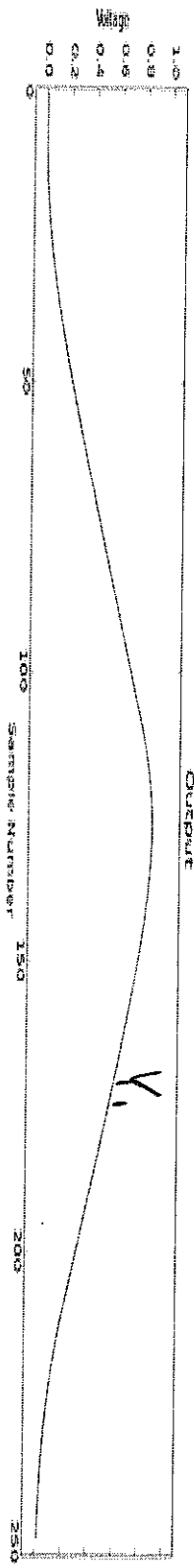
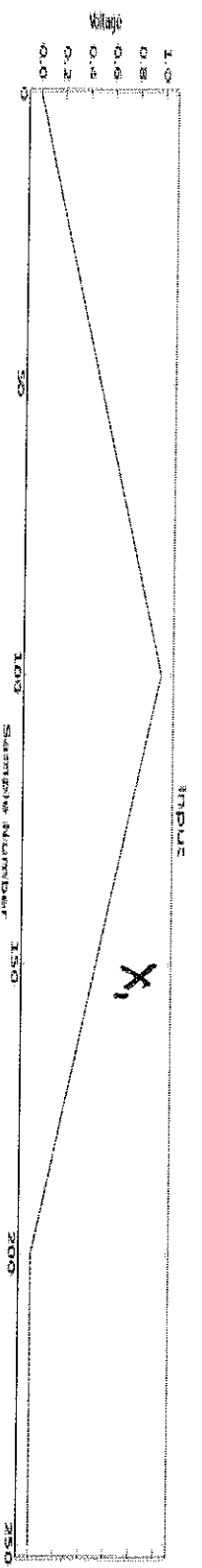
RLZGHSYSTEM

n



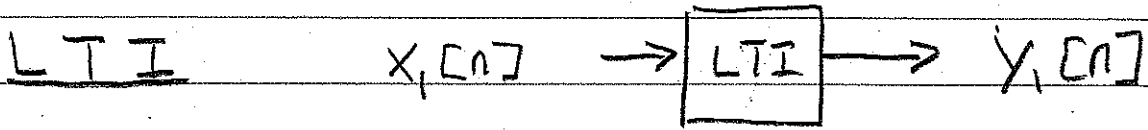
LOW SYSTM

noin

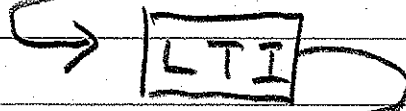


Linear Time Invariant Systems

Examples

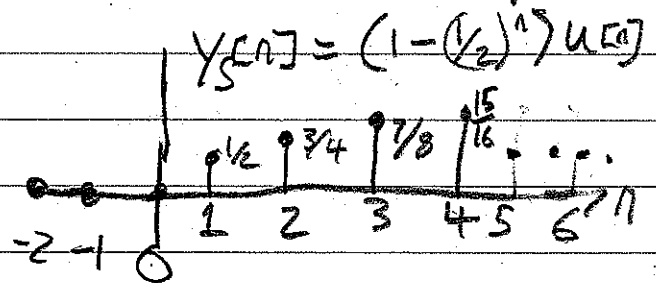
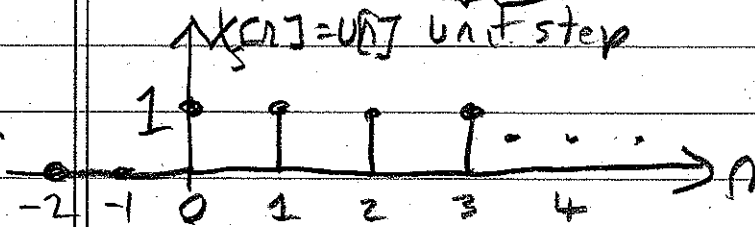
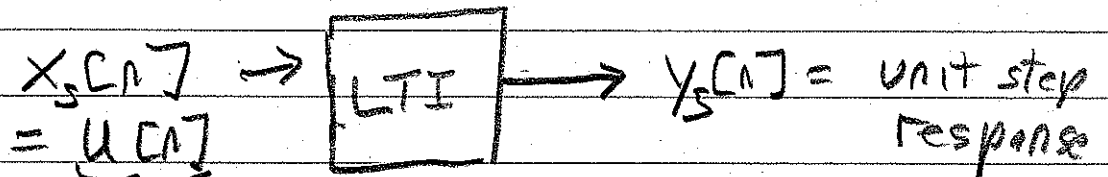


$$\Rightarrow A x_1[n - N_A] + B x_2[n - N_B]$$

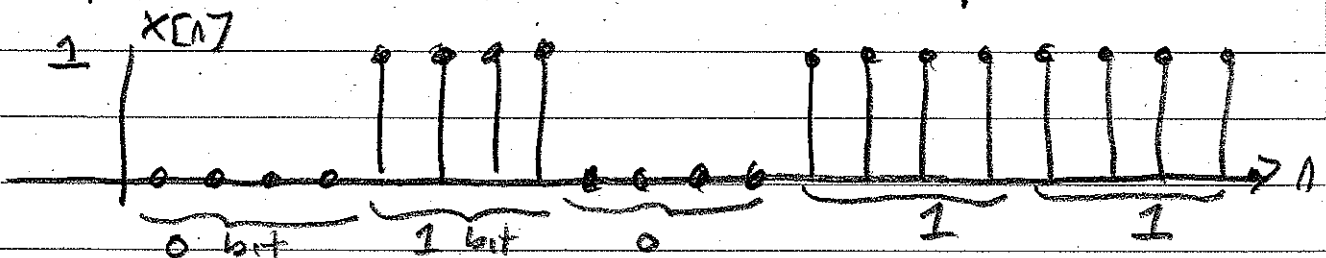


$$\rightarrow A y_1[n - N_A] + B y_2[n - N_B]$$

Example - Unit Step Responses



Suppose $x[n] =$ $y[n] = ?$



Rewriting $X[n]$

$$X[n] = U[n-4] - U[n-9] + U[n-13] - U[n-21]$$

$$\begin{aligned} \Rightarrow Y[n] &= y_s[n-4] - y_s[n-9] \\ &+ y_s[n-13] - y_s[n-21] \\ &= \left(1 - \left(\frac{1}{2}\right)^{n-4}\right) U[n-4] - \left(1 - \left(\frac{1}{2}\right)^{n-9}\right) U[n-9] \\ &+ \left(1 - \left(\frac{1}{2}\right)^{n-13}\right) U[n-13] \\ &- \left(1 - \left(\frac{1}{2}\right)^{n-21}\right) U[n-21] \end{aligned}$$

