**FETs**
- Spec sheets
- Configurations
- Applications

**Acknowledgements:**
Neamen, Donald: Microelectronics Circuit Analysis and Design, 3rd Edition

---

### MOSFET vs JFETS

**MOSFETS**
- Much more finicky difficult process (to make) than JFET’s.
- Good news: Extremely high input impedance. Zero input current.
- Bad news: Easily blown up by ESD on the gate. Add protection circuit and input bias current becomes at best comparable to JFET’s.
- Good news: Essentially infinitely fast. If you change the gate voltage, the device will respond instantaneously! Essentially always in static equilibrium.
- Bad news: It can be really hard to change the gate voltage quickly! (especially power devices)
- Much better power devices than JFET’s. (There were briefly power JFETs as output devices in audio amps. Too many blew up.)
- And you can’t make digital VLSI out of JFET’s.

---

### JFETS - MOSFETS

<table>
<thead>
<tr>
<th></th>
<th>BJT</th>
<th>JFET</th>
<th>MOSFET</th>
</tr>
</thead>
<tbody>
<tr>
<td>Circa</td>
<td>1960</td>
<td>1970</td>
<td>1980</td>
</tr>
<tr>
<td>Gm/I (signal gain)</td>
<td>Best</td>
<td>Better</td>
<td>Good</td>
</tr>
<tr>
<td>Isolation</td>
<td>PN Junction</td>
<td>Metal Oxide</td>
<td></td>
</tr>
<tr>
<td>ESD</td>
<td>Low</td>
<td>Moderate</td>
<td>Very sensitive</td>
</tr>
<tr>
<td>Control</td>
<td>Current</td>
<td>voltage</td>
<td>Voltage</td>
</tr>
<tr>
<td>Power</td>
<td>YES</td>
<td>No</td>
<td>Yes</td>
</tr>
</tbody>
</table>

---

### JFET’s
- Very simple manufacturing process like BJT’s. Much cheaper than (discrete) MOSFET’s. Quieter than MOSFET’s.
- Low input bias current – like back biased diode. As low as 10pA.
- But note this doubles every 6 deg C! At high temps a JFET op amp can have more input current than some bipolar op amps!
- Used in microphones, hearing aids and other high impedance sources (electret microphones have very high output impedance) because of low noise and ruggedness compared to MOSFET’s.
- Fast. Used on many high speed scope probes. Was major advance in bias current and speed over bipolar-input op amps. See data sheets of (JFET input) LF356 series and compare to then extant bipolar.
- Downside is input capacitance can’t be as low as some BJT’s.
- Wide spread in threshold voltage and zero-Vgs current. Sometimes requires sorting and selecting for a given circuit.
Field Effect Transistors (FET)

- FETs are voltage controlled devices with very high input impedance (little current)
- MOSFET: Metal Oxide Semiconductor FET
- JFET: Junction FET

\[
\begin{align*}
\text{G} & \quad \text{D} \\
\text{S} & \quad \text{D} \\
\text{N channel JFET} & \quad \text{P channel JFET}
\end{align*}
\]

MOSFET Symbols

- MOSFET made VSLI (microprocessors and memories) possible.
- Very high input resistance
- Voltage controlled device
- \( V_{gs} < V_t \) off state
- \( V_{gs} \geq V_t \) on state

Simple Model of MOSFET

Excellent graphic showing four states of MOSFET for different \( V_{gs} \) and \( V_{ds} \)

Ohmic contact to body to ensure no body bias, top left: threshold, top right: Ohmic, bottom left: Active mode at onset of pinch-off, bottom right: Active mode well into pinch-off – channel length modulation evident
What’s the difference between the drain and the source?

MOSFET’s can be symmetrical and drain and source interchangeable. Especially inside IC’s.

But discrete devices (with few exceptions) have input protection networks on the gate to protect against ESD. Also, the substrate must connect somewhere.

Once the input protection clamping and the substrate are connected to a terminal, that must be the source.

“ideal” mosfet curves continued

Triode mode, or “linear” mode, or ohmic region.

\[ I_D = \frac{\mu_c C_{ox} W}{L} \left( V_{GS} - V_T \right) V_{DS} - \frac{V_{DS}^2}{2} \]

Saturation or active mode.

\[ I_D = \frac{\mu_c C_{ox} W}{2} \left( V_{GS} - V_T \right)^2 \left( 1 + \lambda (V_{GS} - V_{DS}) \right) \]

As the channel length becomes short, these equations become inaccurate. At the channel ends, source and drain regions causing “fringing” effects and Distort the electric fields from the “ideal” case used to derive above eq’s.

For analog design, long-channel MOSFET’s can offer extremely high output Impedance, making excellent “stiff” current sources. Minimum geometry transistors used in digital VLSI do not have such flat curves.
MOSFETS: Gain & non-linearity

MOSFETs (metal-oxide-semiconductor field-effect transistors) are four-terminal voltage-controlled switches. Current flows between the diffusion terminals if the voltage on the gate terminal is large enough to create a conducting “channel”, otherwise the mosfet is off and the diffusion terminals are not connected.

\[ I_{DS} \propto \frac{W}{L} \]

FETs as switches

The four terminals of a Field Effect Transistor (gate, source, drain and bulk) connect to conductors that generate a complicated set of electric fields in the channel region which depend on the relative voltages of each terminal.

**CONDUCTION:**
If a channel exists, a horizontal field will cause a drift current from the drain to the source.

**INVERSION:**
A sufficiently strong vertical field will attract enough electrons to the surface to create a conducting n-type channel between the source and drain. The gate voltage when the channel first forms is called the threshold voltage -- the mosfet switch goes from "off" to "on".

### N-Channel General Purpose Amplifier

#### Electrical Characteristics

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>OFF CHARACTERISTICS</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Vss</td>
<td>Gate-Source Breakdown Voltage</td>
<td>Vgs = 0 V, Vds = 600 V</td>
<td>600 V</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Gate-Source Current</td>
<td>Vds = 0 V, Vgs = 600 V</td>
<td>70 mA</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Gate-Source OFF Voltage</td>
<td>Vgs = 0 V, Vds = 600 V</td>
<td>70 V</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Output Current</td>
<td>Vds = 60 V, Vgs = 600 V</td>
<td>70 mA</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Output Voltage</td>
<td>Vgs = 0 V, Vds = 60 V</td>
<td>70 V</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### Small Signal Characteristics

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Characteristic</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Forward Transconductance</td>
<td>500 S</td>
<td>500 S</td>
<td>500 S</td>
<td>S</td>
</tr>
<tr>
<td></td>
<td>Input Capacitance</td>
<td>1 pF</td>
<td>1 pF</td>
<td>1 pF</td>
<td>pF</td>
</tr>
<tr>
<td></td>
<td>Output Capacitance</td>
<td>1 nF</td>
<td>1 nF</td>
<td>1 nF</td>
<td>nF</td>
</tr>
<tr>
<td></td>
<td>Common Source Figure</td>
<td>100</td>
<td>100</td>
<td>100</td>
<td></td>
</tr>
</tbody>
</table>
MOSFET Configurations

NMOS Common Source

- More generalized common source with “source degeneration” and equations:

<table>
<thead>
<tr>
<th></th>
<th>Definition</th>
<th>Expression</th>
</tr>
</thead>
<tbody>
<tr>
<td>Current gain</td>
<td>$A_I = \frac{i_{out}}{i_{in}}$</td>
<td>$\infty$</td>
</tr>
<tr>
<td>Voltage gain</td>
<td>$A_V = \frac{v_{out}}{v_{in}}$</td>
<td>$-g_m R_D \frac{1}{1+g_m R_S}$</td>
</tr>
<tr>
<td>Input impedance</td>
<td>$r_{in} = \frac{v_{in}}{i_{in}}$</td>
<td>$\infty$</td>
</tr>
<tr>
<td>Output impedance</td>
<td>$r_{out} = \frac{v_{out}}{i_{out}}$</td>
<td>$R_D$</td>
</tr>
</tbody>
</table>
NMOS Common Drain – Source Follower

- Equations

<table>
<thead>
<tr>
<th>Definition</th>
<th>Expression</th>
<th>Approximate expression</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>Current gain</td>
<td>$A_I = \frac{i_{out}}{i_{in}}$</td>
<td>$\infty$</td>
<td>$\infty$</td>
</tr>
<tr>
<td>Voltage gain</td>
<td>$A_V = \frac{v_{out}}{v_{in}}$</td>
<td>$\frac{g_m R_S}{g_m R_S + 1}$</td>
<td>$1$</td>
</tr>
<tr>
<td>Input resistance</td>
<td>$R_{in} = \frac{v_{in}}{i_{in}}$</td>
<td>$\infty$</td>
<td>$\infty$</td>
</tr>
<tr>
<td>Output resistance</td>
<td>$R_{out} = \frac{v_{out}}{i_{out}}$</td>
<td>$\frac{R_S}{g_m R_S + 1}$</td>
<td>$\frac{1}{g_m}$</td>
</tr>
</tbody>
</table>

MOSFET Configurations

Three basic configurations.

Common source

Common drain

Common gate

NMOS Common Gate

- Equations:

Cascode Configurations

All have the same purpose – to decouple the input terminal (of the bottom device) from capacitive feedback from the output by taking the output from a second device.

Bottom device: Current gain (no appreciable voltage gain)
Top device: Voltage gain (no current gain)
Combines common-emitter/source/cathode with common-base/gate/grid. Result is

BJT

JFET

MOSFET

Vacuum tube triode
Cascode Configuration continued

Bottom device: Current gain (no appreciable voltage gain)
Top device: Voltage gain (no current gain)

Combines:
common-emitter/source/cathode
with
common-base/gate/grid.

Result is like a single common-emitter/source/cathode device with drastically reduced “Miller capacitance” from the output to the input.

JFET Amplifier Configurations

- Common Source Amplifier
- Common Drain Amplifier [Source Follower]
- Common Gate Amplifier

JFET Amplifier Configurations

Common Source JFET (bypassed source resistor)

\[ A_v = -\frac{V_{in}}{V_{out}} = -g_{m}v_{gs}R_L \]
\[ A_{v} = \frac{g_{m}v_{gs}R_L}{1 + g_{m}R_S} \]

* For polarized (electrolytic) input coupling capacitor, the “+” should be oriented towards the most positive DC voltage. For example, if there is -2V on the gate, and -8V associated with Vin, then the capacitor orientation should be reversed as shown.

The input coupling cap for the common gate configuration will most often be a polarized electrolytic, since the impedance at the Source of the JFET is only \(1/g_m\) in parallel with \(R_S\).
Common Drain Amplifier (Source Follower)

\[ A_v = \frac{v_{out}}{v_{in}} = \frac{g_m v_{gs} R_S}{v_{gs} + g_m v_{gs} R_S} = \frac{g_m v_{gs} R_S}{v_{gs} [1 + g_m R_S]} \]

\[ A_i = \frac{g_m R_S}{1 + g_m R_S} \]

Output Resistance – Source Follower

Remove \( R_S \) and replace it with a test AC voltage generator.

Short the input signal \( V_i \) and replace it with its source resistance \( R_i \).

Solve for \( I_{test} \), which is a consequence of applying the test generator \( V_{test} \) and \( V_{in} \), in terms of the hybrid-\( \pi \) parameters.

To correctly calculate the value of a bypass capacitor for \( R_s \), use the parallel combination of \( r_o \) and \( R_S \).

\[ r_o = \frac{V_{test}}{I_{test}} = -\frac{V_{gs}}{g_m} = \frac{1}{g_m} \]

Low Frequency Hybrid \( \pi \) Model

<table>
<thead>
<tr>
<th>Characteristic</th>
<th>Common Source</th>
<th>C Source with ( R_S )</th>
<th>Common Drain {Source Follower}</th>
<th>Common Gate</th>
</tr>
</thead>
<tbody>
<tr>
<td>Voltage Gain ([\text{if } f_{\text{in}} &gt;&gt; R_i])</td>
<td>( A_v = -g_m R_i )</td>
<td>( A_v = -\frac{g_m R_i}{1 + g_m R_i} )</td>
<td>( A_v = -\frac{g_m R_i}{1 + g_m R_i} )</td>
<td>( A_v = \frac{g_m R_i}{1 + g_m R_i + \frac{R_i}{R_S}} )</td>
</tr>
<tr>
<td>Current Gain</td>
<td>( I_2 ) ( I_2 ) Very large</td>
<td>( I_2 ) ( I_2 ) Very large</td>
<td>( I_2 ) ( I_2 ) Very large</td>
<td>( I_2 ) ( g_m R_i + 1 )</td>
</tr>
<tr>
<td>Input Impedance</td>
<td>( R_0 )</td>
<td>( R_0 )</td>
<td>( R_0 )</td>
<td>( R_0 ) ( \frac{1}{g_m} / R_S )</td>
</tr>
<tr>
<td>Output Impedance ([\text{if } f_{\text{in}} &gt;&gt; R_i])</td>
<td>( R_0 ) ( R_0 )</td>
<td>( R_0 ) ( R_0 ) ( \frac{R_0}{g_m R_i + 1} / R_S )</td>
<td>( R_0 ) ( R_0 ) ( \frac{R_0}{g_m R_i + 1} / R_S )</td>
<td></td>
</tr>
<tr>
<td>Phase Reversal?</td>
<td>Yes</td>
<td>Yes</td>
<td>No</td>
<td>No</td>
</tr>
</tbody>
</table>
OK, now what can we do with these things?

This schematic from the now obsolete Intersil 7662 datasheet shows how a “flying capacitor” generates a negative voltage from a positive voltage. Slightly different connections can double a voltage instead of inverting it.

JFET follower

A JFET follower using matched (dual) JFETs. The bottom JFET automatically generates just the right amount of current to bias the top one so Vin is approximately equal to Vout.

JFET variable attenuator

The Dolby B noise reduction circuit used this circuit as a Variable attenuator. Horowitz and Hill go through the equations to show how adding \( \frac{1}{2} \) the drain voltage back to the gate voltage greatly linearizes the JFET resistance.

Synchronous Rectification

Patent 8,493,751 Dr. Schlecht, former MIT Professor of Electrical Engineering

Synchronous rectification refers to replacing diode rectifiers with power MOSFETs, and “synchronizing” their on/off to the primary. MIT Professor Schlecht did not invent the concept, but he came up with a fiendishly clever way to drive the MOSFET’s with effectively reactive components and waste less power in the gate drive. He founded SynQor, now in Boxborough Mass, in 1997. Power converters generating high currents (50A, 100A) at low voltages (3.3V, 1.8V) for digital boards (think Google server farms) must use synchronous rectification – the forward voltage drop of even Shottky rectifiers would kill the efficiency.
Neat Circuit Ideas

3-LED CHASER

This circuit lets you see how a FET turns on and how it works. Remove the connections to the gate of the first FET and the LED will start to illuminate. The gate will start to get a charge on it and the FET will turn on. Place a 1M between gate and 0v and the FET will turn off. This shows the sensitivity of the gate. The charge on the gate must be removed for the FET to turn OFF.

This circuit will show how the FET turns ON slowly as the voltage on the gate increases and turns OFF slowly as the voltage decreases.

More from same web site – note single-ended drive implies this motor has commutator brushes. I had wrongly assumed these drills used brushless motors.

PWM MOTOR SPEED CONTROLLER

Here is a circuit from a 12v drill. The MOSFET will deliver up to 30Amps. The frequency of the oscillator is in the range 550Hz to about 6.5kHz, with an off period of about 2.6us.

Continuing from this website – This is a great summary of MOSFET failure modes – AKA (Also Known As) What NOT to do with a MOSFET.

WHY MOSFETs FAIL

There are quite a few possible causes for device failures, here are a few of the most important reasons:

Over-voltage:

MOSFETs have very little tolerance to over-voltage. Damage to devices may result even if the voltage rating is exceeded for as little as a few nanoseconds. MOSFET devices should be rated conservatively for the anticipated voltage levels and careful attention should be paid to suppressing any voltage spikes or ringing.

Prolonged current overload:

High average current causes considerable thermal dissipation in MOSFET devices even though the on-resistance is relatively low. If the current is very high and heatsinking is poor, the device can be destroyed by excessive temperature rise. MOSFET devices can be paralleled directly to share high load currents.

Transient current overload:

Massive current overload, even for short duration, can cause progressive damage to the device with little noticeable temperature rise prior to failure.
Shoot-through - cross conduction:
If the control signals to two opposing MOSFETs overlap, a situation can occur where both MOSFETs are switched on together. This effectively short-circuits the supply and is known as a shoot-through condition. If this occurs, the supply decoupling capacitor is discharged rapidly through both devices every time a switching transition occurs. This results in very short but incredibly intense current pulses through both switching devices.
The chances of shoot-through occurring are minimized by allowing a dead time between switching transitions, during which neither MOSFET is turned on. This allows time for one device to turn off before the opposite device is turned on.

No free-wheel current path:
When switching current through any inductive load (such as a Tesla Coil) a back EMF is produced when the current is turned off. It is essential to provide a path for this current to free-wheel in the time when the switching device is not conducting the load current.
This current is usually directed through a free-wheel diode connected anti-parallel with the switching device. When a MOSFET is employed as the switching device, the designer gets the free-wheel diode "for free" in the form of the MOSFET's intrinsic body diode. This solves one problem, but creates a whole new one...

Excessive gate drive:
If the MOSFET gate is driven with too high a voltage, then the gate oxide insulation can be punctured rendering the device useless. Gate-source voltages in excess of +/- 15 volts are likely to cause damage to the gate insulation and lead to failure. Care should be taken to ensure that the gate drive signal is free from any narrow voltage spikes that could exceed the maximum allowable gate voltage.

*** WAIT A MINUTE! This author fails to point out that practically all discrete MOSFET's have a voltage clamp on the input. The actual failure mechanism is usually you melt the clamping zener, and the puddle of molten silicon forms a short. The MOSFET may be fine, but the gate is now shorted to the source, which makes it kind of hard to use.

Slow reverse recovery of MOSFET body diode:
A high Q resonant circuit such as a Tesla Coil is capable of storing considerable energy in its inductance and self capacitance. Under certain tuning conditions, this causes the current to "free-wheel" through the internal body diodes of the MOSFET device. This behaviour is not a problem in itself, but a problem arises due to the slow turn-off (or reverse recovery) of the internal body diode.
MOSFET body diodes generally have a long reverse recovery time compared to the performance of the MOSFET itself.
This problem is usually eased by the addition of a high speed (fast recovery) diode. This ensures that the MOSFET body diode is never driven into conduction. The free-wheel current is handled by the fast recovery diode which presents less of a "shoot-through" problem.

Insufficient gate drive - incomplete turn on:
MOSFET devices are only capable of switching large amounts of power because they are designed to dissipate minimal power when they are turned on. It is the responsibility of the designer to ensure that the MOSFET device is turned hard on to minimise dissipation during conduction. If the device is not fully turned on then the device will have a high resistance during conduction and will dissipate considerable power as heat. A gate voltage of between 10 and 15 volts ensures full turn-on with most MOSFET devices.

***NOTE: The reference to gate voltages of "between 10 and 15 volts" applies to older or higher voltage power devices (like 20 to 200V). The newer power parts have long been based on the latest digital process: i.e., they're designed for 5V. Newer power MOSFET's have guaranteed on resistance at lower Vgs voltages consistent with use in 3.3V logic inputs, and have Vds absolute maximum ratings of 6V or 7V, and similar abs max Vgs ratings. Modern logic requires lots of power conversion devices operating at these low voltages.
Hi-freq signal path ("tweeter")

Low freq signal path ("woofer") uses low-frequency op amp. Hi & lo freq combined in output stage that drives 50 ohm scope input.
For further reading and possible inspiration for your projects, read Jim Williams app notes! You gotta love a guy who titles an app note (#25):

Switching Regulators for Poets
A Gentle Guide for the Trepidatious

And on the next slide here's the last page:

(They told me I couldn't leave the last page blank)