Analog Synthesizer Project

6.101 Final Project Report

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Overview

From the birth of popular music, with the invention of the phonograph, to the increased availability of music, due to various music stores and libraries such as iTunes, technology shaped the creation of music. This effect has touched every aspect of the industry, from the business model to the music itself. One particular interest is how technology has changed the style and sound of music. For example, the electric guitar forever changed music by ushering in rock, while computers caused an equally large shift by enabling modern electronic music, such as techno. The analog synthesizer was another influential device that changed rock music as well as helped to create electronic music.

Analog synthesizers were the first purely electrical instruments. Although electric guitars preceded analog synthesizers, analog synthesizers produce purely electronic signals while electric guitars convert mechanical signals (the vibration of wires) into voltages that are then processed to produce sound. Due to this mechanical input, mechanical instruments produce distorted waveforms, which are impossible to replicate in purely analog systems. These uniquely distorted waveforms give the instruments their distinctive sound. Similarly, the unique sound of an analog synthesizer is due to the perfect waveforms generated by these instruments. This perfect signal has a sound that is nothing like a conventional instrument and has helped to create as well as heavily influenced electronic music. Influential bands such as Kraftwerk and Brian Eno used analog synthesizers prominently in their seminal work.

In the eighties, analog synthesizers were largely replaced by digital synthesizers, which in the nineties were replaced by computers. Both digital synthesizers and computers enable the generation of arbitrary waveforms. Despite the advantages of these alternatives, analog synthesizers continue to remain popular among some musicians, because the analog signals provide a precise sound that digital systems cannot match. In addition, the modularity of the synthesizer encourages musicians to create new and unique combinations of sounds in a way that a pre programmed instrument cannot.

In addition to their musical uses, analog synthesizers are of great interest to electrical engineers because they use concepts and building blocks from a diverse set of electrical systems. A single module may incorporate elements from AM and FM radios, timers, and filters in addition to digital circuitry. Common building blocks include multipliers, exponential current sources, and voltage controlled resistors. In addition, in order to drive the generated music through speakers loud enough for a live audience, a lot of work must be done to create a high power amplifier and power supply. Therefore engineers can gain a lot of useful knowledge and experience from building an analog synthesizer.

Our group, Elliott, Lauren and Elaine, divided the analog synthesizer project into three components: the power supply, signal processing, and power amplifier stage, with Elliot focusing on the signal processing, Lauren designing and building the power supply, and
Elaine working on the power amplifier. These three systems were designed separately and then integrated together near the end of the project timeline.

Design Overview

This document describes the proposed design of our analog synthesizer project. The project is partitioned into three sections: the analog synthesizer module, and the power supply and the power amplifier.

Figure 1: The Overall Block Diagram for the whole system. Key presses on a keyboard are passed to the signal processing unit that creates a tone. The tone is then driven through a speaker by the amplifier. The power supply provides power to both systems. Elliott built the Signal Processing unit, Elaine built the amplifier, and Lauren built the power supply.

1. Analog Synthesizer Module (Elliott)

An analog synthesizer consists of several modules that can be wired together in different ways to create different sounds. A particular wiring setup is called a “patch”. Modules connect to each other using two different types of signals. One type is called a waveform signal, which is a waveform being generated, modified, or played through a speaker. The other type of signal is a control signal, which determines how a module works. A control signal may be a 5 volt pulse to trigger an event in another module or a varying waveform to control the amplitude of an output signal at a given time. Waveform signals have a voltage range of plus and minus 5 volts while control signals range from zero to 5 volts. Because any module can be plugged into any other module, signals are carried between modules via quarter inch mono cables through standard output and input buffers. The output resistance of the output buffer is set to 1k to prevent damage should the output
be grounded. The input resistance of the input buffer is set to 100k to reduce attenuation.

Because the synthesizer is modular, a fixed block diagram of the system does not accurately describe how the system works. However, a fairly standard patch is shown in Figure 1 to provide the reader with a reference to help understand the function of each module and how they may be used together.

![Block Diagram of a Typical Patch on an Analog Synthesizer](image)

**Figure 2. Block Diagram of a Typical Patch on an Analog Synthesizer:** The blocks represent modules while the lines represent signals. The black lines are waveform signals while the colored lines represent different control signals. Note that analog synthesizers are inherently modular and thus this block diagram only represents one such configuration. In this setup, the controller reads the keyboard presses and produces the corresponding control signals. The one volt per octave signal is fed into both the VCO and the VCF so that filter will track the tone generated. The output of the VCF is then modified by the output of the envelope generator to produce an output signal that is fed to the amplifier.

The standard analog synthesizer is made up of five basic modules, the controller, the voltage controlled oscillator, the voltage controlled filter, the voltage controlled amplifier, and the envelope generator. Additional modules were added as stretch goals. These modules are the sample and hold, the noise source, the portmanteau, and the low frequency oscillator.

The controller is the user interface of the synthesizer. It converts key presses on a keyboard into three control voltages that define the signal to be generated. One signal is a voltage proportional to the key that was pressed. This voltage is set so that an increase in one octave will increase the control voltage by one volt, which will result in a doubling in frequency at the output of a VCO. This one volt per octave signal is an exception to the typical voltage limits of a control signal and may range from -5 volts to 5 volts to provide an output bandwidth from around 30 Hz to 20 kHz. The other two output signals are a 5 volt trigger and a 5 volt gate. The trigger is simply a pulse that indicates exactly when a note has been pressed. A gate is a signal that is high whenever a note is held down and low when all notes are released. These two signals can be used by an envelope generator.
to control the amplitude of the output waveform over time based on the inputs on the keyboard.

A voltage controlled oscillator produces several waveforms dependent on the input signals and its knob settings. Output signals include sine, triangle, sawtooth, square, and PWM waveforms. The frequency of oscillation can either be controlled by a potentiometer or by a 1 volt per octave signal from a controller. VCO’s sometimes have an optional input that can perform frequency modulation of the input signal and the generated signal.

A voltage controlled filter is a bank of filters controlled by input voltages and potentiometer settings. While there are many types of VCFs with different output types, the proposed system will have low pass, band pass, band stop, high pass, and notch filter outputs. The basic VCF filters an input signal at a frequency set by control knobs and input voltages. Typically the one volt per octave input voltage output of the controller is inputted to both the VCO and the VCF. In this setup, the filter will track the frequency of the outputted waveform and will thus produce the same effect at different frequencies. This is typically used to remove some selection of harmonics to alter the timbre of the output waveform. Advanced VFC designs provide options to adjust properties of the filter such as its Q.

The voltage controlled amplifier is a two quadrant multiplier that allows a control input to modify the amplitude of an input signal. Clearly the VCA takes in one control input and one signal input. VCA’s are typically used in combination with envelope generators to give notes a realistic time response. Instead of turning notes on and off immediately, which introduces high frequency components that create a clicking sound, notes are turned on and off more gradually like a mechanical instrument. VCA can also be used to add other effects such as AM modulation. A two quadrant multiplier is used so that a slightly negative control voltage will ensure the signal is turned off. This makes it easier to control the amplitude of the output signal. Four quadrant multipliers, referred to as ring modulators, are also used in analog synthesizers albeit less frequently. Ring modulators are used to create audio effects such as tremolo.

Finally, the envelope generator is a module that takes in a gate and trigger signal and generates a time dependent output signal to be used by a VCA to give the output signal a more realistic sound. A typical envelope generator creates an ADSR signal. ADSR stands for the four sections of the envelope, attack, decay, sustain, and release. The attack phase is an exponential rise to some peak voltage when the generator receives a trigger. Once the peak voltage is reached, the exponentially drops to a final value that is held until the gate signal ends. The exponential drop is the delay stage while the held final value is the sustain stage. Once the use lifts their finger, the sustain voltage exponentially drops down to zero volts. This last stage is called the release stage. Each of the voltage levels and timing values of the ADSR envelope can be modified. This allows an envelope generator to simulate a large number of possible envelopes.
These five main modules form a minimum of what is needed on a synthesizer in order to produce interesting musical tones using a keyboard. Other modules are typically found in an analog synthesizer though not as prominently as the five described above. These modules were stretch goals that greatly enhanced the range of output sounds that can be produced. These additional modules include a sample-and-hold, a noise generator, a low frequency oscillator, and a portmanteau. There are enough additional modules that one can spend a lifetime working with analog synthesizers (as many hobbyists do). However, time only allowed the creation of these extra modules.

The extra modules perform the following tasks. The low frequency oscillator is a more limited oscillator whose frequency is controlled manually. However, the low frequency oscillator is designed to produce frequencies from around a kilohertz down to millihertz. This low frequency oscillation can be used as a control signals to create interesting effects. For example, the LFO can be used to sweep the frequency of the VCO or VCF to create slowly changing tones or timbers.

The random noise source produces a collection of fixed noise outputs. The implementation in this design is able to create white noise, pink noise, and low frequency noise. The white noise has constant power spectral density at all frequencies and sounds like the static from a tv set or radio not tuned to the proper channel. The power spectral density for pink noise decreases linearly with frequency. This noise sounds different than that of white noise. Finally the low frequency noise only contains noise at low frequencies. These noise sources can be used as audio inputs that can be processed by the VCO and other modules or as control voltages to control modules effecting other signals.

The portmanteau limits the slew rate of an input voltage to a rate specified by a potentiometer. While both linear and exponential portmanteaus are possible, this design utilized an exponential portmanteau because humans perceive both amplitude and frequency logarithmically, therefore an exponential change will be perceived as linear. This module can be used on the controller to make the synth glide from one note to the next.

The sample and hold is very self descriptive. The module samples an input voltage and produces an equal output voltage for a fixed period of time. The sample rate can be controlled by either an external clock on an internal clock whose rate is controlled by a potentiometer. This module can be used to sample a random source to produce random tones or on a ramp to create a staircase waveform.

Below is a detailed description of the specific implementation of all of the modules included in the signal processing system.
a. Voltage Controlled Oscillator (VCO)
Figure 3: Voltage Controlled Oscillator Schematic. This schematic is courtesy of Electronotes by Bernie Hutchens. Some adjustments were made to replace outdated parts or resolve implementation issues that arose.
Figure 3 is the circuit implementation for the Voltage Controlled Oscillator. The VCO can be broken up into two subcircuits. The first is a sawtooth wave generator that creates a dc-biased low magnitude sawtooth wave whose frequency is proportional to the input control voltages. The second subcircuit, the wave shaper, takes in this sawtooth wave and processes it into five different output waveforms, sawtooth, triangle, square, sine, and PWM. We begin by discussing the implementation of the sawtooth wave generator.

![Figure 4: Block Diagram of Sawtooth Wave Generator subcircuit. This subcircuit is one half of the VCO module. This subcircuit produces a sawtooth waveform whose frequency is exponentially proportional to the input control voltage. It also has the ability to sync frequencies with another VCO in addition to performing FM modulation.](image)

Figure 4 is a high level block diagram that describes the implementation of the sawtooth wave generator in more abstract terms than the circuit diagram. Input voltages from external sources and panel potentiometers are summed together with an op amp summer to form a single voltage proportional to the desired output frequency of the sawtooth waveform. This voltage is then used to drive an voltage to exponential current converter that is biased by some current.

The exponential current converter can be created by connecting the emitters of two matched npn transistors together, driving one of the bases with a small voltage, and attaching the base of the other to ground. The driven npn is then biased with some current to set its gm. The resulting configuration is an voltage to exponential current converter. This is illustrated by the following math for the two transistors.

\[ Ic1 = a \cdot Is \cdot \exp((V_{in} - V_e)/26mV) \]

\[ Ic2 = a \cdot Is \cdot \exp(-V_e)/26mV \]

\[ Ic1 = a \cdot Is \cdot \exp(-V_e/26mV) \cdot \exp(V_{in}/26mV) \]

Note that since the transistors are matched, the coefficients are equal. Therefore:

\[ Ic1 = Ic2 \cdot \exp(V_{in}/26mV) \]
Note that IC1 is driven by the bias current and IC2 is the output current. Therefore:
\[ I_{out} = I_{bias} \times \exp(-V_{in}/26mV) \]

Clearly a linear increase in voltage will produce an exponential decrease in current. Because the input summer is an inverting summer, an increase in input voltage to the summer will create an exponentially larger current output of the current converter. The output current of this converter is proportional to the frequency of the output signal. Clearly range of the output frequency needs to match the range of human hearing (~20 Hz to 20 kHz) and the input voltage can only range from -Vcc to +Vcc. This difference in range is the reason that an exponential current converter is used instead of a linear converter.

The bias current of the converter is controlled by a voltage to current converter driven by a fixed voltage and an optional fm input voltage. If this input voltage is increased, the bias current of the exponential current converter is also increased. This in turn causes the voltage to current gain of the exponential converter to be increased. Thus the output current will be higher for a given input because the given input voltage is effectively multiplied by the fm input voltage. Therefore if an ac voltage is applied to the fm input, the output current of the exponential converter will vary with the frequency of the ac signal. Because this current is proportional to the frequency of the output waveform, the frequency of the output waveform will vary with the fm input frequency. Therefore the frequency set by the input control voltages is linearly modulated by the frequency of the fm input, creating linear fm modulation.

The output current of the exponential current converter is then used to drive a capacitor. Because \[ I = \frac{dV}{dt} \], driving a capacitor with a fixed current will cause the voltage to increase at a fixed rate. This capacitor voltage is then buffered and sensed by a comparator. If the capacitor voltage is higher than some threshold, the comparator drives a FET to short the capacitor. The capacitor will then begin to charge up again at the same rate. This process will repeat, with the capacitor being shorted whenever it reaches a threshold. Because the capacitor is shorted at a fixed voltage, the frequency at which the capacitor is shorted is proportionate to the input current. This capacitor voltage is thus a sawtooth wave with some dc-offset whose magnitude is set by the threshold voltage and frequency is set by the input current. Therefore the sawtooth generator subcircuit creates a sawtooth waveform whose frequency is proportionate to the input voltage.

This subcircuit does have one extra functionality. By placing a differentiator (small coupling capacitor) between the sync in input and the center of the resistor divider that defines the threshold, a large change in sync in can greatly alter the threshold. If a large negative change in voltage was driven across the cap, the threshold would drop to zero forcing the comparator to be triggered and the capacitor to be shorted prematurely. Therefore, driving the sync in voltage with a large sawtooth wave will force the capacitor to short whenever the sync in voltage dropped. Connecting two VCO’s so that both have their sync in connected to the other will thus cause the two sawtooth generators to synchronize as the shorting of one capacitor will short the other as well. Thus two VCOs can be synchronized together.
Figure 5: Block Diagram of Wave Shaper subcircuit. This subcircuit is one half of the VCO module. This subcircuit shapes a dc offsetted input sawtooth waveform into a zero centered sawtooth waveform in addition to a Square, Triangle, Sine, and PWM waveforms. This subcircuit also produces a Sync Out signal to be used in syncing VCOs.

Figure 5 is a high level block diagram that describes the implementation of the wave shaper subcircuit. The dc-offset sawtooth waveform is amplified and centered around zero an inverting amplifier with dc adjust. This block creates an inverted sawtooth waveform centered around zero. This waveform is then inverted again to create a sawtooth waveform centered around zero. This waveform is then outputted directly as a sync out signal, and attenuated to ± 5v to produce the sawtooth wave output.

The sawtooth wave is then compared with the origin to create a square wave. Because the sawtooth is symmetric with respect to the origin, it spends half of its period negative and half of the period positive. Therefore, the output of the comparator will indeed be a square wave. Similarly, the inverted sawtooth wave is compared with an adjustable threshold to produce a pwm waveform. This threshold can be adjusted manually to manually set the duty cycle of the pulse, or with an input waveform to create pulse width modulation. The threshold is generated by summing the manual control and the pwm input together. This threshold is compared with the inverted sawtooth wave so that the output is high whenever the threshold is larger than the sawtooth.

The max of the sawtooth and inverted sawtooth waveforms is then generated by connecting one end of two diodes together and the other end to the sawtooth waveforms. Each diode will conduct whenever the waveform they are connected to is larger than the other. This creates a triangle waveform that ranges from zero to the peak values of the sawtooth waveforms. There is a little issue in the comparison in that their is a glitch whenever the two waveforms suddenly shift. This glitch is reduced by using a compensating capacitor to reduce the change in voltage that results form the glitch. This triangle waveform is then amplified and shifted by another inverting amplifier with DC adjust. The output of this waveform is a triangle wave centered at zero.

Finally the triangle waveform is used to drive a FET in its nonlinear regime. Because the current of a FET is
quadratically related to the input voltage at large voltages, the current output to a large voltage ramp input is a curve. Therefore by driving a FET with a large triangle waveform, the output current becomes a curved triangle. This curved triangle is an excellent approximation of a sine curve, especially with trimmer potentiometers to control the magnitude of the input triangle and thus the curvature of the output current. This current is pushed through a resistor to create an sine voltage which is then amplified to create a sine output.
b. Voltage Controlled Filter (VCF)

Figure 6: Voltage Controlled Filter Schematic. This schematic is courtesy of Electronotes by Bernie Hutchens. Some adjustments were made to replace outdated parts or resolve implementation issues that arose.
Figure 7: Block Diagram of Voltage Controlled Filter Module. This module uses the voltage-to-exponential converter used in the VCO to control the resistors in a state-variable filter. By changing the input voltage, the breakpoint frequency of the filter changes exponentially. This module provides a notch (not shown), high, low, and band pass filter output in addition to Q control.

Figure 6 is the circuit implementation for the Voltage Controlled Filter. Figure 7 is a high level block diagram that describes the implementation of the VCF. The basis of this specific VCF is the State-Variable Filter. The State-Variable filter consists of two integrators and two feedback loops. The output of the second integrator is added to the attenuated output of the first integrator and fed into the first integrator. The behavior of this filter is well understood yet lengthy to analyze. Instead of reprinting the entire mathematical analysis, a simple description of the results will suffice. Those interested in the mathematical analysis should view [2] or do a quick internet search. The state variable filter is simultaneously a first order high-pass, low-pass, and band pass filter, depending on where the output is taken from the feedback loop. The low and high pass filter responses can also be summed together to produce a notch filter. The Q of the filter can be adjusted by controlling how much of the band pass response is fed back into the input.

The circuit implementation of the State Variable Filter is simple, it is just two integrating op amps, a voltage summer, and an attenuating potentiometer in the feedback path. In order to create a VCF, however, the breakpoint frequency of the filter must be exponentially adjusted by a voltage input. The breakpoint frequency can easily be adjusted by altering the resistance of the integrators simultaneously. By varying the resistance, the RC time constant of the integrators change and the break frequency of the filter changes. Current controlled resistors in addition to the voltage-to-exponential current converter described in section 1a, are used to exponentially control the integrator resistors, and thus the breakpoint frequency with a control voltage. All that remains is to create a current controlled resistor.

A transconductance amplifier can be used to create a current controlled resistor.
amplifier has the following input output voltage equation.

\[ I_{out} = g_m(V_p - V_m) \text{ where } g_m = C \times I_{bias} \] for some constant C

Therefore if the minus terminal is fixed at ground and \(V_p\) is used as an input:

\[ I_{out} = C \times I_{bias} \times V_{in} \]

Yet \( R = \frac{V}{I} \), therefore:

\[ R = \frac{1}{C \times I_{bias}} \]

Clearly as the bias current increases, the effective resistance of the transconductance amplifier decreases. This in turn shifts the breakpoint frequency of the filter higher. Thus by biasing the transconductance amplifiers with the output current from the voltage to current converter, the breakpoint frequency of the filter can be exponentially controlled with a linear control voltage.

c. Voltage Controlled Amplifier (VCA)

Figure 8: Block Diagram of Voltage Controlled Amplifier Module. This module implements a simple two quadrant multiplier to modulate the magnitude of a signal input with the magnitude of a control input. Its two quadrant nature allows a negative control voltage to produce a 0 volt output signal, ensuring that no signal passes through.

Figure 9 is the circuit implementation for the Voltage Controlled Amplifier. Figure 8 is a high level block diagram that describes the implementation of the VCA module. The VCA should multiply an input voltage of positive or negative sign with a positive control voltage. This way a slightly negative control voltage will ensure zero output from the VCA. This slightly negative voltage is much easier to obtain than an exact zero. Therefore the VCA is a simple 2 quadrant multiplier. One way of achieving a two quadrant multiplier is biasing two matched BJTs in a differential tied emitter configuration with a current proportional to the control voltage. In this scheme, the transconductance is proportional to the control voltage and thus the output current is proportional to the product of the control voltage and input signal at the base. Therefore, this scheme requires a current to voltage converter at the output and a voltage to current converter at the input. To ensure linear multiplication, the input and output voltages must be small and thus an attenuator is needed at the signal input and an amplifier is needed at the signal output.
A voltage to current converter with the proper coefficients can be created by placing a current multiplying current mirror in feedback with a summing op amp. The input voltages are summed together as currents and pushed through the collector of the first transistor in the current mirror. The mirror tries to reflect this current to the opposite bjt's collector current to force the base emitter voltages to be equal. However because the second bjt has a smaller emitter resistor, more current is pushed through the second transistor. The op amp sinks both of the emitter currents. Therefore the differential multiplying pair is driven by a current proportional to the control voltages.
d. Envelope Generator (EG)

Figure 10: Envelope Generator Schematic. Note that while this schematic is original, it is based on a design courtesy of Electronotes by Bernie Hutchens.

Figure 10 is the circuit implementation for the Envelope Generator. The EG can be broken up into two subcircuits. The first, the control subcircuit, is a state machine that controls the generator switches that generate the ADSR waveform. The second subcircuit, the generator, is a switched circuit that will generate an ADSR waveform. The desired output waveform is an ADSR waveform. An ADSR waveform begins to increase to some maximum value when the trigger goes high (the Attack phase), then decay (the Decay phase) to some sustain voltage that it stays at (the Sustain phase) until the gate is released. At this point, the waveform decays to zero (the Release phase). Figure 11 depicts an ADSR waveform.

The control subcircuit takes in two signals, the Gate and Trigger control signals. This signals are buffered with comparators to ensure a fast response to either input. The attack phase should begin whenever the trigger goes high, and remain on until either the gate falls or the output waveform reaches its peak of 5V. At this point, the attack phase should end and the decay/sustain phase should begin. The decay/sustain phase should remain on unless another trigger occurs (in which case the attack starts again) or the gate falls. Whenever the gate is low, the controller should be in the release phase.
Figure 11: The ADSR waveform. When the key is pressed, the waveform magnitude ramps up during the attack phase. Once the waveform reaches a peak it decays down to a sustain level. When the key is released the waveform decays back to zero during the release phase. The envelope generator module implements this waveform and allows the attack, decay, and release time constants in addition to the sustain level to be controlled. Note that the EG produces an exponential attack, decay, and release, not linear as is shown in the figure.

Figure 12: Block Diagram of Control subcircuit. This subcircuit makes up half the Envelope Generator. This circuit controls the switches in the generator subcircuit by performing necessary digital logic operations (implemented with bjets and ttl logic). This module ensures that the phases transition correctly and at the right
Figure 12 is a high level block diagram that describes the implementation of the control subcircuit. The logical expressions in this description are implemented using BJT inverters or a TTL nor package. The flip flop is created by placing two nor gates in feedback with each other. The flip flop is set whenever the trigger occurs and reset whenever the gate is low or the peak is reached. Therefore the attack signal will go high if the trigger is pressed and will remain high as long as the peak is not reached and the gate is high. The decay/sustain signal should be high whenever the gate is high and the attack is low. This is created by anding the not attack output of the flip flow and the gate signal. Finally, the output waveform is compared with a 5V reference to determine whether or not the peak has been reached. Clearly this controller implements the proper signalling to control the ADSR waveform.

Figure 13: Block Diagram of Generator subcircuit. This subcircuit makes up the other half of the Envelope Generator. A capacitor is pulled to different voltage levels through different time constant setting resistors depending on which switch is currently active. The time constants and sustain voltage are controlled via potentiometers.

Figure 13 is a high level block diagram that describes the implementation of the generator subcircuit. The subcircuit consists of three voltage sources connected to a capacitor by three switches with a variable resistor in the middle. When the switch is down, the capacitor voltage is pulled to the associated voltage through a variable resistor that sets the time constant of the voltage change. This capacitor voltage is the ADSR envelope that is buffered and outputted. The three voltage sources and resistors determine the behaviour of the three major phases of the ADSR waveform. The switches of these legs are controlled by the controller. The attack leg pulls the capacitor voltage up to 6V, forcing the capacitor voltage to go above 5V and trigger a change in state. The decay/sustain leg pulls the capacitor voltage to a voltage set
by the sustain potentiometer. Finally, the release leg pulls the capacitor voltage to ground. Thus as the switches are turned on and off, the capacitor voltage increases to 5 volts, drops to the sustain voltage, and then drops to zero again.

e. Controller (C)

Figure 14: Controller Schematic. This schematic is courtesy of Electronotes by Bernie Hutchens. Some adjustments were made to replace outdated parts or resolve implementation issues that arose.

Figure 14 is the circuit implementation for the Controller. The controller is interfaced with a keyboard via a series of switches. Each key on the keyboard has its own switch that is closed whenever the key is pressed. A 100 ohm resistor is placed between one end of each sequential switch, creating a massive resistor chain. The resistor chain is then driven by a fixed current and thus the voltage at each of the switches is equal to $100^*i^*N$ when $i$ is the current and $N$ is the number of the switch (with the lowest key being 0). $i$ is set so that one the voltage at a given key is one volt more than the voltage at the key an octave below it. This creates a 1 volt per octave scaling of the key voltages. Note that this current can
be adjusted to change the tuning of the voltages.

The other end of all of these switches are tied together with a massive resistor to -15 and buffered. The output of this buffer is called the keyboard state voltage. When no key is pressed, the keyboard state voltage is negative. Pressing one of the switches causes the keyboard state to become the voltage of the pressed key. The massive resistor forces the current through resistor chain, unaffected by the output voltage. If multiple keys are pressed, the keyboard state voltage becomes the voltage of the lower state.

The rest of the controller circuit processes the keyboard control voltage to output the desired control voltages, namely that the proper key voltage is outputted when a key is held, that the gate is high when a note is held, and that the trigger goes high whenever a note is pressed.

Figure 15: Block Diagram of Controller module. The switches of a keyboard are used to short a current driven resistor chain to create voltage indicating which key is currently pressed. This voltage is then processed to produce the trigger and gate control voltages in addition to the 1 VPO control voltage requested by the current key press.

Figure 15 is a high level block diagram that describes the implementation of the controller. The Keyboard state voltage is first compared with the origin. If the state voltage is positive than at least one key is being held down and the gate goes high. In addition the state voltage is differentiated and amplified to create a large voltage spike whenever the state voltage changes. This spike will occur whenever a new note is pressed or a note is released. However, this spike is not well defined in terms of length in time. Therefore a 555 timer is used to create a millisecond pulse every time the spike occurs. This pulse is a transition detection pulse. Note that the transition detection pulse is not the same the trigger because the trigger only occurs when a note is pressed and transitions occur when a note is released. Because of the time delay associated with the transition detection pulse generator, this pulse can safely be and-ed with the gate signal to determine whether the transition is a trigger. If the transition is a trigger, another pulse generator is used to create a millisecond trigger pulse. This trigger pulse is outputted as the trigger signal.
The trigger pulse is also used to sample the keyboard state voltage. This sampled voltage is buffered and outputted as the 1 VPO control voltage. The keyboard state control voltage is sampled so that the 1 VPO voltage will not change if the key is released. This way, the tone of a note will not change as the envelope of the waveform enters its release phase (if an envelope generator is used). The sampling circuit is simple to understand. A capacitor is connected to the keyboard control voltage via a FET. The trigger pulse is used to turn the FET on and pull the capacitor up to the keyboard state voltage. When the trigger falls, the FET closes and the capacitor retains the state voltage. The capacitor size is chosen so that it is small enough to quickly be pulled to the sampled voltage yet large enough to retain the sample voltage for an extended time period in the presence of leakage currents.

f. Low Frequency Oscillator (LFO)

**Figure 16: Low Frequency Oscillator Schematic.** This schematic is courtesy of Electronotes by Bernie Hutchens. Some adjustments were made to replace outdated parts or resolve implementation issues that arose.

**Figure 17: Block Diagram of Low Frequency Oscillator.** A simple Integrator Schmitt trigger oscillator whose frequency is controlled by attenuating the schmitt trigger output voltage using a potentiometer. This module is able to generate triangle and square waveforms on the order of several seconds.

Figure 16 is the circuit implementation for the Low Frequency Oscillator. Figure 17 is a high level block diagram that describes the implementation of the LFO. The LFO is a basic triangle square oscillator. The output of a schmitt trigger is attenuated and fed into an inverting integrator. The output of this attenuator is then fed into the schmitt trigger. Suppose the output of the schmitt trigger is positive. The inverting integrator will thus output a negative slope. At some point, this slope will cross below the negative threshold of the schmitt trigger, forcing the output of the schmitt trigger to the negative supply. The integrator will then output a positive ramp and thus the input to the schmitt trigger will start...
increasing. Eventually this voltage will become larger than the positive threshold of the trigger and the cycle will begin again.

This loop is clearly an oscillator with a triangle wave output at the integrator output and a square wave output at the schmitt trigger output. The magnitude of the triangle wave is set by the schmitt trigger thresholds while the frequency is set by the slope of the integrator output. This slope is controlled by the magnitude of the output of the schmitt trigger. Therefore by placing a controllable attenuator to adjust the magnitude of the input into the integrator, the slope of the output of the integrator can be adjusted. This allows the frequency of the oscillator to be adjusted. Fortunately this method of frequency control allows for very low oscillation frequencies as the only limitation is the op-amp parasitics.

g. Noise Source (NS)

![Noise Source Schematic](image)

Figure 18: Noise Source Schematic. This schematic is courtesy of Electronotes by Bernie Hutchens. Some adjustments were made to replace outdated parts or resolve implementation issues that arose.
Figure 19: Block Diagram of Noise Source. A back biased base emitter junction of a BJT produces a small amplitude white noise signal. This white noise signal is amplified to be a 5 volt signal and then filtered to produce both pink and low frequency noise.

Figure 18 is the circuit implementation for the noise source. Figure 19 is a high level block diagram that describes the implementation of the noise source. A BJT transistor is reversed biased by connecting its base to ground and placing the emitter at a higher voltage, the collector is not connected to anything. This configuration creates an almost gaussian noise signal of extremely low magnitude. This gaussian noise source is greatly amplified (through two amplifiers to maintain bandwidth) to create a 5V white noise source. This white noise is then passed through a shaping filter create a pink noise source. Because pink noise already has attenuated high frequencies, the pink noise is then passed through a low pass filter to create noise only at low frequencies.

h. Portmanteau (P)

Figure 20: Portmanteau Schematic. This schematic is courtesy of Electronotes by Bernie Hutchens. Some adjustments were made to replace outdated parts or resolve implementation issues that arose.

Figure 20 is the circuit implementation for the portmanteau module. The portmanteau is achieved by driving an RC circuit with the input voltage. This RC circuit causes the capacitor voltage to exponentially approach the input voltage. By making the resistor adjustable, the time constant of the exponential can be controlled. The voltage across the capacitor is then integrated over a short time period to limit the maximum slope of the response. Therefore, the rate of change between voltages can be adjusted by adjusting the resistor.
i. Sample and Hold (S+H)

Figure 21: Sample and Hold Schematic. This schematic is courtesy of Electronotes by Bernie Hutchens. Some adjustments were made to replace outdated parts or resolve implementation issues that arose.

Figure 21 is the circuit implementation for the Voltage Controlled Oscillator. Figure 22 is a high level block diagram that describes the implementation of the sample and hold module. The sampling circuit is very similar to that of the controller. A capacitor is connected to the input voltage via a FET switch that is turned on by a clock pulse. When the FET is on the capacitor charges up and when the FET is off, the capacitor retains its voltage. The input voltage and capacitor voltage are both buffered to drive the capacitor quickly and to help the capacitor retain its voltage over long periods of time.

The triggering of the FET is handled by a switchable monostable 555 timer circuit. In one configuration, the 555 timer acts as a pulse generator whenever pin 2 is triggered by a buffered external clock. This external clock is buffered by a comparator to ensure a snappy response. In the other configuration, pin 2 is triggered by an RC circuit. In this circuit, C discharges through an adjustable R until pin 2 is triggered. At this point pin 3 goes high, forcing a sample and charging C back up through the diode. This resets the timer circuit. The rate of this internal clock is controlled by an adjustable resistor, allowing the user to set an arbitrary sample rate.
2. Power Amplifier System (Elaine)

The signal from the analog synthesizer was amplified using a Class-G power amplifier with +/- 25V and +/-15V supply rails at the output. The input signal into this amplifier was expected to be at maximum +/-5V peak to peak, so the gain of this amplifier was designed to be about 4 (rail to rail output cannot be reached because of diode drops in all three stages of the amplifier). As the human ear can hear from about 20Hz to 20kHz, the bandwidth of the amplifier was designed to uniformly amplify sound in this range, although problems were seen with distortion at maximum input signal and frequencies above 17.4 kHz. A class G amplifier was chosen for the power amplifier stage because it is more efficient than a class B amplifier but still maintains linearity (unlike a class D amplifier). Linear systems generally give less distortion at the output than non-linear ones, so with the class G amplifier we can strive for both efficiency and sound quality. The general design of a power amplifier can be divided into five smaller stages: The input stage, the voltage amplifying stage, the output block, the output network, and the negative feedback loop that extends from the output back to the input stage (see figure 23). In this document, the feedback network will be described as part of the output stage. The output network must be designed with the characteristics of the speaker system in mind. This block was not implemented in the final network as attention needed to be focused on maintaining the other stages of the system.
The Power Amplifier Design. This design consists of five modules: the input stage, the voltage amplifying stage, the class G output stage, the output network, and the negative feedback stage.

a. The Input Stage

The input stage of the amplifier was a differential amplifier with current set using a pnp bjt above the Complementary Feedback pair differential amplifier, and with an npn current mirror below (see figure 2). The bjt allows the user to control the amount of current being supplied into the input stage, therefore from here the slew rate of the overall amplifier can be tweaked. The 10k resistor sinks current through the 1N914 diodes, these diodes set the voltage above the 10k resistor at 13.6V. This sets the voltage across the resistor to be between 0.6V and 0.7V, measurements need to be taken to check this exact value when building the circuit. The complementary feedback pairs (Q34,Q35 and Q36,Q37) in the differential input circuitry provides local negative feedback that has been measured in other designs to halve third harmonic distortion for a -30 dBu input voltage (Audio Power Amplifier Design Handbook). Note using that the complementary feedback pair adds another set of resistors to the circuit: a higher resistor value here improves the linearity, but it also adds more noise. The recommended value for this resistor is therefore 2.2kohms. The two 22 ohm resistors (Figure 24) also improve the input-stage linearity and decrease high frequency oscillation by providing local negative feedback, these values are approximated by \( r_e = 25/I_c \) ohms; \( I_c \) here is in terms of mA (Audio Amplifier Design Handbook).

The differential amplifier has two inputs, one being for the raw input signal from the signal processing unit, the other being for the negative feedback of the scaled down output signal. A differential amplifier makes a good input stage because it allows for global negative feedback to set the gain of the amplifier. The output current can be determined by the following relationship: \( I_{out} = I_e \cdot \tanh(-V_{in}/2V_t) \), \( I_e \) being the total current of the circuit and \( V_t \) being the thermal voltage of about 26 mV. Maximizing \( I_e \) thereby increases transconductance (we double \( I_e \) by using a current mirror instead resistors at the collectors of the differential amplifier); it also gives us the opportunity to increase the slew rate, which is determined by \( I_e/C_{dom} \) (\( C_{dom} \) is the dominant capacitor, see VAS stage). The slew rate must be taken into account for producing clean high frequency signals; the required slew rate for this amplifier is \( 2\pi \cdot \text{frequency} \cdot \text{peak voltage} \).

The sizing of C2 is described in the Audio Amplifier Design Handbook as important to maintain the low frequency response and to prevent capacitor distortion from causing a rise in third harmonic distortion at low frequencies. In my design I used a 10uF capacitor with protective shunt diodes (1N4148) in both directions. After building the circuit, however, it was not clear if this capacitor was truly effective in decreasing distortion. The small networks located in the top and bottom supply rails are meant to provide ripple protection, which were potentially critical as our group was building our own power supply. Ripple protection was incorporated these into the proposed pcb layout, but was not used in the breadboard layout which still worked well since the power supply had minimal ripple voltage.
Figure 24: final input stage design. Note that R54 can be adjusted to set the required current, which equals roughly R54/0.6V. My final value for this resistor was 340 ohms, and should have actually been a lower value (see the design process section).

b. The VAS stage

The VAS stage consists of a 2 kilo-ohm resistor current source that feeds into a string of eight diodes, followed by a 2N2219A common emitter transistor that is supported by a 34 ohm emitter degeneration resistor below (figure 25). The input is fed into the base of the transistor, while the output is taken from different points across the diode string. The resistor sustains a voltage drop of about 34V when attached to the input stage, and therefore supplies a 17 mA current. The VAS stage is critical for providing the full voltage swing, as well as for being the site of pole compensation. The 850 pF capacitor connecting the base (and the input) of the 2N2219A transistor to the emitter of the same transistor is in place to keep the phase shift from falling below 180 degrees before the gain of the overall amplifier falls below unity: this would cause high frequency oscillation. The diodes in this circuit compensate for the diode drops in the following output stage, and therefore prevent crossover distortion. Outputs are taken from across the four center diode drops, for instance, to account for the four diode drops between the high and low input transistors in the class-B portion of the class-G amplifier (see next
c. The Class G Stage

Its two supply rails characterize the Class G stage, which as previously stated were +/- 25V and +/- 15V. The Class G stage is composed of two Class-C outer power devices, and an inner Class-B power device (see figure 26). Class C power devices are characterized by their switching on and off during operation.; these are only powered by the 25 and -25 volt rails. The uppermost and lowermost Power BJTs that are each a part of a Class-C sub-module are turned on according to the VBE multiplier biasing (or diode drop biasing) from the previous VAS stage. When the voltage on the other side of the top input, for instance, is higher than 15V added with 2 diode drops (or about 16.2V), the top class C portion of the amplifier turns on. The biasing essentially “pushes” the input signal up (or down), so a larger portion of the signal can be powered by the two more extreme rails. If the bias voltage is set too low, the outer class-C circuits will turn on too late, resulting in the amplifier not being able to source enough current. Meanwhile, if the bias voltages are set too high, then the amplifier exhibits excessive heat dissipation. The 15 V rail only supplies current when the voltage on the other end of the limiting diode drops below roughly 14.4V, upon which the diode turns on. The output stage provides the current to drive the load, but has only unity gain. The 100 ohm emitter degeneration resistors in both the class B and class C portions of the circuit provide local negative feedback, which reduce output distortion. Emitter degeneration resistors valued at 0.5 ohms were placed in the class-B portion of the output stage to keep the transistors from overheating. A resistor was sized to give the appropriate voltage gain, and was fed the output signal back to the negative feedback port of the differential amplifier. The gain can be determined by (feedback resistor)/1 +1 for this circuit. For the class G output stage, I used FJA4210OTU (pnp) and FJA4310OTU (nnp) transistors in the power stage, as well as 1N4001 diodes at
the 15V source and 1N4741 diodes feeding into the output stage from the VAS stage (see figure 27).

Figure 26: The Class G Output Stage: note that the component values are described more clearly in the text.

**d. The Proposed Output Network**

The output network generally needs the most tweaking due to the presence of inductors. It is comprised of a shunt Zobel network and series output inductor/damping resistor parallel combination. The Zobel network provides stability into inductive loads, while the latter circuit gives stability into capacitive loads. It is important to note that the output inductor should be air-cored to eliminate the possibility of distortion due to magnetic materials. The coil wire should be thick, as thin wire will add more parasitic resistance and, reducing the voltage drop across the 8 ohm speaker load (Audio Power Amplifier Design Handbook). A very small resistor can be placed in parallel to the output inductor to reduce overshoot and ringing. Again, this portion of the circuit was not implemented due to time constraints, but would have reduced some distortion and remains a proposed improvement to the design.

**e. Integrated Schematic and Component List**
See figure 6 (below) and previous sub-circuits for more details.

Input Stage: 2N3906/2N3904 bjts, 0.5W, 0.34 kilo-ohm resistor sourcing from the 25V rail, all other resistors are 0.25W (2 x 22 ohms, 2 x 2.2 kilo-ohms, and 2 x 100 ohms), 2 x 1N914 diodes, and a 10k resistor to sink current in the biasing circuitry for the current source.

Voltage Amplifying Stage: 1N914 diodes for biasing, 2N2219A common emitter bjt, resistors at 0.5W (34 ohms, 2 kilo-ohms), 850 pF capacitor.

Class G Output Stage: 2N3055/D45H11 power transistors, 2N2219A/2N2095A bjts for all other transistors, MUR460 diodes, MURS320 diodes, 0.5 ohm, 1W resistors, 4 x 100ohm 0.5W resistors.

Feedback: 0.25W resistor, sized with consideration of the input signal.

Figure 27: The Power Amplifier full schematic
3. Power Supply (Lauren)

Lauren is designing and building the power supply, which will be a fixed-voltage, linear power supply. This design will provide +/-25V and +/-15V to the power amplifier and +/-15V to the signal processing of the analog synthesizer. The idea was to have the power supply supply a peak of 3.2A at 25V to the power amplifier (25V/8 Ohm = 3.2 A) and ~2A at 15V, as well as 2A at 15V to the signal processing. However, in implementation, we realized our system drew less current, so the power supply ended up supplying 2A at 15V as well as 3A at 25V. To accomplish this, the power supply requires six transformers, two rated at 24VAC at 4A and four rated at 18VAC@2A. Working at such high currents required high current rated components as well as heat sinking.

The power supply design is comprised of five major modules: the transformer, the rectifier, the filter, and the regulator. These modules will be modified and designed to output both +/-25V and +/-15V as shown below in Figure 3 and Figure 4.

![Figure 28: Fixed-Voltage, Linear Power Supply for +/-15V](image)

As shown in Figure 3, the first module includes two Transformers, which are responsible for stepping down the AC line from 110VAC to 18VAC. With 18VAC, there is approximately 25V to work with to generate an output of 15V. By putting two transformers in parallel, 4A of current is able to be obtained. The AC signal is then rectified by a diode circuit, which is then filtered into an unregulated DC signal by a large capacitor. The signal is then regulated to reduce output ripple, and produce a constant +/-15V output.

![Figure 29: Power Supply for +/-25V](image)
As shown in Figure 4, the +/-25V is similar to the +/-15V design, however the +25V and the -25V require 24VAC@4A transformers. Because we were able to purchase 4A transformers, putting two transformers in parallel is not necessary. The entire voltage will be rectified, filtered, and regulated to output the final output voltage. Overall, the transformer converts down the AC line voltage to a smaller peak voltage, which is approximately 34V, which gives 9V to work with. The rectifier uses diodes to produce a rectified sine wave, which has a large DC component. The filter then smooths out the rectified signal wave, creating an unregulated DC voltage with ripple. The final regulating circuitry eliminates ripple, producing a DC output. In addition to meeting the power requirements of the signal processing, the power supply requires much heat sinking, lower gauge wires, and higher rated components to accommodate for the large currents and voltages it must supply.

Figure 31: Power Supply Circuitry Design. The above schematic details the power supply circuitry. The +VAC and -VAC inputs are from the 18VAC and 24VAC transformers, and the output is +/-15V and +/-25V respectively.

The above figure depicts the power supply implementation. The following section details the submodules in this design.

a. Transformers

Figure 31: The Transformers. This is a picture of the six transformers used in the power supply. On the left are two 24VAC@4A transformers. On the right are four 18VAC@2A transformers. The furthest two on the right are connected in parallel to create a 18VAC@4A supply, as are the leftmost 18VAC transformers.

The first stage of the power supply design is the transformers, as shown above. The two 24VAC
transformers on the left are connected to one power cord, while the four 18VAC transformers on the right are connected to another. This stage takes the output of the wall socket of 110VAC and steps it down to 18VAC and 24VAC. These transformers are connected so that they supply 4A to both 15V rails and both 15V rails.

b. Diode Rectifier

![Diode Rectifier](image)

**Figure 32: The Diode Bridge Rectifier.** Above is the diode bridge that is used to rectify the 18VAC as well as the 24VAC into 25VDC and 35VDC, respectively.

The diode rectifier rectifies the AC output of the transformer, resulting in a rectified sine wave. The resulting voltage from the rectifier is approximately \( \sqrt{2} \) times the AC voltage. Therefore, the unregulated DC value for the 15V circuitry is \( 18\text{VAC} \times \sqrt{2} \) which is approximately 25V while the 25V circuitry is approximately 35V. The component used for this part is the MC84 diode rectifier.

c. Filtering Capacitor

![Capacitor](image)

**Figure 33: The Filtering Capacitor.** The capacitor used for the power supply is a 24,000uF capacitor. This capacitor meets the requirements for voltage ripple reduction and is able to supply the DC current required for this application.

The rectified waveform is then sent to a filtering capacitor that smooths the rectified sine wave, resulting in unregulated DC. This capacitor is large to supply DC current, however because there is voltage regulation circuitry, the value of the filtering capacitor is not crucial.
d. Voltage Regulator

Figure 34: The Power Supply Circuitry. This picture depicts two of the four voltage rails that were soldered onto perforated boards. Starting from the bottom, one can see the heatsink of the diode rectifier which then is connected to the voltage regulator circuitry.

The voltage regulation circuitry has two main characteristics: negative feedback and current limiting. The output voltage is set by the negative feedback, which has a voltage reference based on a reversed zener diode. For the 25V circuitry, the zener diode is 15V while the 15V circuitry is 5.1V. This reference is compared to the output of a sense resistor divider. The output of the 25V is divided by the resistor divider that is implemented with R2=10k and R3=15K, i.e. 15K/(10K+15K)*25V = 15V. The op-amp compares these values, and forces them to be equal by driving the darlington pair (i.e. Q1 and Q2, i.e. the TIP120) with more or less current. For the 15V circuitry, R2=20 and R3=10k, i.e. 10K/(10K+20K)*15V = 5V. The op-amp compares these values, and forces them to be equal by driving the darlington pair with more or less current.

Additionally, the voltage regulator is implemented with current limiting. This is implemented using an npn transistor, 2N2219, and 1 Ohm 2W resistors. The Resistors placed in the location of R4 sets the current limit because I_out = V_be/R_4. When the current is high enough to turn on the transistor, i.e. it hits the current limit, the transistor begins to conduct, and draws current away from the darlington pair. As a result, the output voltage and current will drop; therefore providing current limiting. For the 15V circuitry, R4=1 Ohm// 1 Ohm = .5 Ohms which results in 2A current limiting, and for the 25V circuitry, R4=1 Ohm// 1 Ohm // 1 Ohm = .333 Ohms which results in 3A current limiting.

Components List
4 18VAC Transformers  
2 24VAC Transformers  
2 Power Cords  
2 Barrier Strips  
4 MB84 400V 8A Diode Bridge Rectifier + Heat Sinks  
4 24,000uF Capacitors rated at 50V  
4 .1uF capacitors  
8 1uF capacitors  
4 22uF capacitors  
4 100uF capacitors  
4 5.1V Zener Diode  
4 15V Zener Diode  
4 1Kohm Resistors  
4 10K resistors  
4 10K resistors  
4 20K resistors  
4 100 Ohm resistors  
10 1Ohm 2W resistors  
4 T1P 120 Darlington Transistors + Heat Sinks  
4 2N2219 npn Transistors + Heat Sinks  
4 Perforated Boards  
4 LT1632 Op-amps + IC Sockets  
18 Gauge Wire  
22 Gauge Wire  
26 Gauge Wire

Design Process and Experiences

Signal Processing System Design Process and Experience (Elliott)

I decided I wanted to do this project last summer when talking to a coworker at my summer job about analog synthesizers. Not only did they seem like a lot of fun to play with, they seemed to contain a lot of really interesting systems that I wanted to learn more about as an electrical engineer. My coworker recommended that I pick up some of Electronotes by Bernie Hutchens. Electronotes is a semi-regular newsletter about the engineering behind music that has been running in one form or another since the 70’s. A large portion of the notes are dedicated to the design and construction of analog
synthesizers. Interested, I purchased a copy of The Musical Engineer’s Handbook and the Builder’s Guide and Preferred Circuit Collection. These two books form an introduction to analog synthesizers and the application of electrical engineering to music. I read all of both books over spring break so that I would understand everything that I needed to do prior to starting on my project. After comparing the presented topologies of each module, I selected one of each while on vacation. That way when I returned to MIT I would be ready to jump right in. I had one goal when returning to MIT, try to build the synthesizer on a breadboard as fast as possible to work out all of the bugs so I could create a permanent PCB version that I could keep.

Work on the synthesizer went very well. While the schematics supplied by the books were extremely helpful, a fair amount of tweaking was needed. Because the schematics were from the 70’s, a fair amount of the components were no longer available. This ultimately changed the design of certain blocks slightly and required a great deal of rework. After three very busy weeks of work I completed all of the modules except for the controller and was thus ready to build my PCB. I didn’t include the controller on the PCB because it needed to interface with a toy keyboard that I did not own yet.

The creation of the keyboard interface was challenging. Most cheap keyboards today use a microcontroller to scan an array of switches to see which switch is down. Figure 35 is a picture of such an array. Unfortunately I needed a series of independent switches. Fortunately, every switch was connected to the array on one side and a diode on the other. By unsoldering all of the diodes and soldering a wire in its place, I was able to get an independent wire for each switch. I then soldered all of the array wires together to form the keyboard state voltage node. This method turned out to work very well except for the warping of keys due to the hot glue used to keep wires in place. A future design will have a mover carefully constructed keyboard.
Figure 35: Keyboard Switches. The gold pads along the top of the PCB are switches that conduct whenever a conducting plate (not shown) attached to the key touches the PCB. As can be seen by the traces, the pads are interconnected in a complicated grid, yet all are attached to a diode (orange tubes at the front of the image). These diodes can be de soldered and replaced with wire to get an independent wire for every switch.

My project was heavily based on work of other people. Typically I would not recommend this because less design is required. However, I would highly recommend using pre existing schematics if one is going to tackle an exhorbitantly complicated project like mine. A project of this scale would simply not be possible for one person to do in one month. A great deal of work was needed just to implement a pre existing schematic. Having to design everything from scratch would have been impossible.

A small note on schematics. I did not include the rework in the schematics included in this paper because they were very much implementation specific. I figured that the original schematics would be more helpful to those using this paper as a source to build their own version. The one exception is the envelope generator. The EG needed to be redesigned from scratch, so I have included my redesign. That being said, I highly recommend picking up some Electronotes, especially the Musical Engineer’s Handbook. It is a wonderful book that shows how EE concepts can be applied some really interesting applications. It is a joy to own and to read.

Working on the breadboard was incredibly fun and rewarding. Every time I finished a module I had a new toy to play with and make interesting sounds. I learnt a great deal
about layout management in addition to how to properly use a large variety of chips. In addition, I have learnt how to build a wide range of circuit modules that will be invaluable in future design.

Figure 36: Analog Synthesizer PCB schematic. This PCB has four layers and contains all of the modules described in this paper in addition to a mixer. The size of the PCB is 2.5” by 3.8”. The yellow squares are capacitors or resistors, the red circles are wire holes and the rest is ICs. Notice how incredibly complicated this schematic is and thus how hard long it took to layout and to ensure it was error free. This is why surface mount is a bad idea, no matter how powerful the size reduction is.

The PCB design was an incredibly difficult task. What I thought would take 10 hours or so took me at least 24. The reasoning for this is that I had so much stuff to implement that I decided to do surface mount. By choosing tiny resistors and ICs, I was able to fit my entire project on a mini board (shown in figures 37 and 38). However this density required creating an incredibly dense chip that took hours to verify. The PCB schematic for the project is shown in figure 36.
Once the chip was designed and manufactured, I had to spend hours tweezering tiny components onto the chip. A stencil was created by saving the expressPCB file as a cad file and using the laser cutter on a sheet of projector plastic. This stencil was used to smear solder paste on the pads. This process is extremely valuable and will save a large amount of time, however, one must be very careful removing the stencil or paste will be smeared over the chip in the wrong places. I also recommend spending a good amount of time when ordering parts to ensure you understand what reflow profile you should use. In my case, we figured it out at the last minute and did it fairly ad-hoc. This may or may not have destroyed some of my components through overheating. Once the PCB was done, testing showed that some modules were working while others were not. Because I did not have a lot of time left until the project was due, I decided to put the PCB on hold and present the breadboarded circuit.
I do not recommend using surface mount parts in a lab project (or any non-industry project) unless the desired goal is a physically small chip (not a dense chip). There are many reasons for this. The design and assembly time for such a chip is significantly larger than a through hole project, so much larger that you run the risk of not completing the chip. I spent a week doing PCB layout alone and a week doing assembly alone and still did not finish. The main reason everything took so long was complexity. There were simply too many components in too small of a space. Another problem is that the chance of making a mistake goes up dramatically in a more complex system, especially if you do not have a lot of extra time to verify things. In a chip that dense, one error could ruin everything. Through Hole projects are limited in their complexity by their size and thus are not as large of a problem. They are also much easier to manufacture. If one is to do a PCB board I cannot stress the importance of breadboarding everything on the PCB before the PCB is manufactured. Otherwise if the design requires any adjustment at all, the PCB will be ruined. This is too likely to happen, and too costly of a mistake. Therefore if the goal is to produce a PCB, extra time is needed and thus the student should get working on the project as soon as possible (building the week after spring break).
This was a wonderful project that was a complete joy to work on. I very much plan on getting my PCB to work sometime in the fall and to keep adding to the system in the future as a hobby. I really liked working with Elaine and Lauren and I hope I get the chance to do so again in the future.

Power Amplifier System Design Process and Experience (Elaine)
I learned the most about amplifier design from the Audio Power Amplifier Design Handbook by Douglas Self, and I based my original design work on suggestions from this book. I also found useful resources online, but these either gave suggestions that were also in the book or were more complex enhancements that I did not get a chance to try to implement. In my design I focused on maintaining linearity through local negative feedback systems. In particular, for the VAS stage, I spent time looking into the benefits and drawbacks of different topologies, considering gain and linearity. I spent time understanding each individual stage and enhancements I could make to improve them, although I did not put enough effort into understanding what to expect when stages were linked together, and how bias points would change. More effort could have also been put into understanding the frequency analysis and phase plots associated with the amplifiers.

I first simulated my circuit using LTSpice using 2N3904/2N3906 transistors in the input stage and voltage amplifying stage, 2N2219A/2N2905A transistors in the Vbe multiplier stage and pre-power class G stage, and 2N3055/D45H11 power transistors in the final power stage. MUR460 diodes (max current = 4A, Vbrkdn = 600V) were used to supply current from the 15V and -15V supply rails, while MURS320 diodes (max current=3A, Vbrkdn=200V) were used to supply the signal to the upper and lower ports of the class G output stage from the Vbe multipliers. The overall circuit was simulated with +/- 25V and +/- 15V supply rails. The simulation showed high amplitude, high frequency oscillations, which could be reduced by increasing the Cdom value, increasing current in both the input and VAS stages, and adding capacitors across biasing diodes and other locations where ac signal did not need to be transmitted through. I changed my design frequently based on the results of my simulations. My simulations were useful in matching biasing points while building my circuit, particularly for the input and voltage amplifying stages, however, they were not as useful in understanding the ac characteristics of my amplifier. When built, high frequency oscillations were not nearly as much of an issue, likely because parasitic capacitances in the circuit would have further enlarged the dominant pole. I did however, have heating issues and frequent short circuits, problems that I would not have been able to predict from the LTSpice simulations.

In my original design for the input stage, I used a 62 ohm resistor as the current setting resistor above the pnp bjt. According to the literature, this should set my slew rate at 11.385*10^6 A/F. As my required slew rate was 2.89*10^6 A/F, this would have given me a high enough slew rate to operate normally. I also originally planned to use a matched pair in the current mirror of the input stage, however, when faced with some biasing issues while building the input stage and integrating the input stage with the voltage amplifying stage, I switched to using two 2N3904 transistors, with gains of 196 and 200, to manually make a
matched pair current mirror and more closely match the design of my simulation. To reduce some high frequency oscillation, I altered my input stage and used a 1kohm resistor (0.5W) in parallel with a 560 ohm (0.5W) resistor as the current settings resistors, giving me an input current of 1.67 mA. This set my slew rate at $I_e/C_{\text{dom}} = 1.67 \text{mA} / 850 \text{pF} = 1.966 \times 10^6 \text{A/F}$, which while building I did not realize was too low. I therefore had slewing problems in the class G version of my amplifier after 17.4 kHz and noticed a distortion peak on the rising side of the output. Interestingly, the AB version of this amplifier did not exhibit this same distortion peak, suggesting that the peak was likely caused by the 15V rail 1N4001 diode in the output stage. More work could have be done to balance between increasing the slew rate and keeping out high frequency oscillation, I had problems with shorting out my circuit and therefore ran out of time to focus on this issue when I had to keep fixing my output stage. I also made significant changes to my design while building the voltage amplifying stage (VAS). The original design for the Voltage Amplifying stage was as shown in figure 3, utilizing a beta-enhancing 2N2219A emitter-follower that would increase negative feedback and therefore improve linearity, similar to the complementary feedback pairs in the input stage. The 850pF capacitor feeding between the bias voltage circuitry and the base of the emitter follower bjt determines the dominant pole of the circuit so that the total loop gain falls below unity before enough phase shift accumulates to cause high frequency oscillation, i.e. a phase shift of 180 degrees before the gain of the amplifier falls below unity. The top portion of the circuit supplies current, a high enough current must be supplied as to not make the VAS stage the limiting factor in effecting the slew rate. The original biasing circuitry consists of VBE multipliers and is meant to remove crossover distortion caused by diode drops in the output stage. The biasing circuitry also determines the voltage at which the upper rail of the output class G stage will be turned on; with VBE multipliers this turn-on point could be tweaked to compromise between distortion and efficiency. I needed higher impedance above my npn common emitter transistor, so I pulled out my bjt current source and just used a 2kohm (2 1kilo-ohm 0.5W resistors in parallel). This resistor must sustain a voltage drop from 25V down to approximately -9V, so this resistor must be either large enough or rated at a high enough power (I managed to melt out a resistor and two diodes while testing). In theory the emitter follower transistor feeding into the common emitter transistor (see figure 39) should have worked, however I had heating problems with the emitter follower transistor and therefore further simplified the design. Part of this may have been due to inconsistencies in the biasing conditions between the simulation and the actual circuit, or perhaps high frequency instability after all. If given more time, I would have tried to implement at least this portion of my original design, and perhaps alter the values of the emitter degeneration resistors. With the 62 ohm resistor in the input stage, the open loop gain of this amplifier (excluding the class G stage) was in the range of 3000. This value was significantly reduced when the input stage current setting resistor value was increased.
Figure 39: Proposed Voltage Amplifying Stage with emitter follower and Vbe multipliers. This stage used 2N2095A (top) and 2N2219A (bottom) transistors. Note that the supply rails are +25V and -25V, and the input from the input stage is fed into the 850pF capacitor/emitter follower base. See Figure 6 for final VAS stage.

The original plan was to put the input stage and the VAS stage on a PCB board. The PCB layout was not actually used in the final product as the voltage amplifying stage was changed significantly. The traces in the PCB were also disconnected in some places, particularly in the input stage. More careful PCB design would involve linking the PCB file to a schematic file. I designed the PCB without building the circuit first because the PCB took time to ship, so I designed the PCB assuming my simulations were accurate, and they were not. If I were to redo this project, I would spend less time tweaking the simulation that showed high frequency oscillations that did not exist in the actual circuit. I would then build the breadboarded version, tweak that, and only order the PCB when I know that the physical design works. The simulations would be used mostly for checking quiescent voltage values when building and debugging. I included my PCB layout in figure 40 for reference. For this circuit 0.010 inch traces were used, which can support a current of 0.3 Amps.
The output stage remained largely unchanged from beginning to end, note that it is key to use large enough emitter degeneration resistors in the output power rail (I used 0.5 ohm resistors). Initially I used 0.1 ohm resistors here and found that my transistors would heat up quickly. When I built the output stage, I used stand-alone heat sinks, with the transistors attached using a nut, screw, and thermal paste. In hindsight, it would have been better to electrically isolate each transistor and attach these to a common heat sink. With this method, I could have also attached the proposed Vbe multipliers in the input stage to the common heat sink, thereby thermally coupling the Vbe multipliers with the power stage. This method would have given better control of the circuit from better tracking between the Vbe multipliers and the power stage, as well as in general dissipate heat more efficiently. For my project, I used a fan to cool the transistors, a method which also proved to be effective. If I did not use the fan, I observed that the current readings from my test current supplies would steadily climb.

In building the class G output stage, I used FJA4210OTU (pnp) and FJA4310OTU (npn) transistors in the power stage, as well as 1N4001 diodes at the 15V source and 1N4741 diodes feeding into the output stage from the VAS stage (see figure 27). To improve this stage, protection circuitry could have been added to prevent some of the frequent short circuits that I experienced while debugging my amplifier. One of the most challenging portions of this project was repeatedly fixing the output stage (and occasionally the inner stages) because a transistor melted.
I based my design off of a design in Power Electronics Handbook (Third Edition) by Muhammad H. Rashid and suggestions from Professor Gim Hom; however a voltage regulator based on a Darlington pair and negative feedback is a classic topology. Although the design was a good basis, I ended up slightly altering my original design by inserting additional capacitors as described below. Overall though, my original design was sufficient in meeting my design goals.

I constructed the first stage of the power supply (the transformer block) by power drilling all six transformers onto a block of wood. After the transformers were secure, I scraped the shellac protective coating off of one of the holes on each of the transformers and screwed a lug nut with 20 gauge wire soldered onto it into the hole. I then took each of these wires (the purple wires above) that were connected to the transformer casing and heat shrunk it to the earth ground lead of my power cords. This connection provides a protective connection to earth ground incase any shorts arise. Next, I connected the primary leads of the 18VAC transformers to the ground and high leads of my power cord. Because the 18VAC transformers I obtained were center tapped and able to support both 230VAC and 115VAC, I connected the power and ground of the power cord to one of the outer leads and the center lead. I had to do this so that the transformer would step down my input voltage of 110VAC to the desired 18VAC; if I had connected the other leads, I would have obtained too low of an output because the turn ratio is different between the outer leads than an outer and center lead. Then, I clipped the unused lead for safety reasons and heat shrunk the connections together. I took the same steps for the 24VAC, however I also had to solder 20 gauge wire leads to both the primary and secondary side, because my 24VAC came with lug connections, not leads. After the transformers were successfully and safely connected to my power cords on the primary side, I connected the secondary side to a barrier strip so that I could connect the stepped down AC voltage to my regulation circuitry. Additionally in this stage is when I connected my 18VAC transformers in parallel. By taking the outer leads of the secondary side (the 18VAC was center tapped, however I needed the stepped down voltage), I matched the outer leads of one 18VAC to another 18VAC and then soldered them together. By connecting them in parallel, I was able to obtain effectively 2 18VAC supplies at 4A, one for the +15V rail and one for the -15V rail. Additionally, one 24VAC rail was available for the +25V rail and one 24VAC was available for the -25V rail.

After I successfully had my 18VAC and 24VAC supplies, I connected it to and tested my voltage regulation circuitry on a breadboard. I was able to see that my voltage regulation was successfully outputting the desired voltages of 25V and 15V, however I could not test my circuitry under a load until I transferred my circuitry to perforated board, because the bread board could not supply the high currents I needed. After heat sinking each of my transistors using thermal grease and screws, nuts, and washers to connect each the heatsinks, I soldered two 15V circuits to one perforated board and two 25V circuits to the other perforated board. I then tested the output of my voltage regulation circuitry again, and saw that I did in fact have
the correct output voltages of 15V and 25V when my circuitry was not connected to a load resistor. Then I tested under a 8 Ohm 100W high power ceramic chasis variable resistor, and found that my circuitry was outputting the desired voltages at 3A, however with a significant amount of ripple (1-2V). At first, I tried to fix the problem by inserting a variety of capacitors in various parts of my circuits. I inserted .1uf, 1uf, and 100uF across the resistor and zener voltage divider at the output of my filtering capacitor and I also inserted a 1uF and 22uF capacitor across my output resistor divider. These additions significantly improved the AC ripple I was observing, resulting in around 200mV of ripple, however I decided to investigate further. I probed the output of my op-amp and discovered that it was oscillating because my phase margin was too small. To fix this issue, I inserted a 1uF capacitor across the output and minus terminals of my op amp. This capacitor effectively introduced a lead zero, increasing my phase margin, and stabilizing the output of my op amp. When I again tested my circuit, all output ripple was eliminated.

Next, after my partners knew what maximum current they would be drawing, I added in my circuit limiting circuit. For the 15V supply, this ended up being two 1 Ohm resistors in parallel which resulted in 2A current limiting. For the 25V supply, this ended up being three 1 Ohm resistors in parallel which resulted in 3A current limiting. I also tested this with my load resistors and verified that the voltage did in fact drop when the circuit was asked to provide current above the limits.

Next, I took my two 15V rails and my two 25V rails and connected them so that I could have plus and minus rails. Because my output rails are relative floating voltages, I was able to combine them to obtain positive, ground, and negative rails. To do this, I connected the negative lead of one rail to the positive lead of the other rail to create a relative ground. By doing so, I created a positive rail (from the first unconnected positive lead) and floating “ground” or neutral rail (from the connected first negative lead and second positive lead) and a negative rail (from the unconnected second negative lead). I made these connections with the 4 leads from my two 15V rails as well as with the 4 leads from my two 25V rails, then took the remaining 3 leads from the 15V rail (+15, neutral, and -15) and the remaining three leads from the 25V rail (+25, neutral, and -25) and connected the two neutrals. As a result, I had 5 final leads; +25V, +15V, neutral (or ground), -15V, and -25V. I connected these leads to a barrier strip, where Elaine and Elliott were able to connect to their +/-25V, +/-15V, and ground wires. From these ports, I was able to successfully power my partners’ projects.

For integration, I first supplied only the +/-15V to Elliott, who was able to successfully power his signal processing system. Then I supplied the +/-15V and the +/-25V rails to Elaine; however our integration results in an issue. Elaine and my circuitry fried each other’s, due to a possibly short in the power supply. My current limiting circuitry is not short protection circuitry, so all of my transistors (the TIP 120s and the 2N2219 npns) fried, and I was forced to de-solder them and replace them with new transistors. This required also heat sinking the new transistors, so the process took a significant amount of time. Once I replaced my transistors though, and Elaine fixed her output stage, we re-integrated the projects, and I was able to successfully power my partners’ projects.

I designed my entire system based on what my partners needed, which was a high voltage as well as a high current power supply. This was not an easy task, and several
tradeoffs were made along the way. I purchased the highest voltage and current rated transformers that were reasonably priced, and I worked with a simple but elegant topology that could meet my partner’s specifications. Through completing this project, I was able to obtain valuable experience in working with power supply systems. Additionally, I was able to exercise several practical construction skills. I used power tools to construct the base of my supply, I soldered and heat shrinked connections to my transformers, I heat sanked all of my components, and I soldered and de-soldered and resoldered my circuitry. Overall, the four power rails that I constructed were a practical but challenging project, and I am very satisfied with my system.

**Testing**

**Signal Processing System Testing (Elliott)**

Testing was done using both an oscilloscope to verify signal shape and functionality in addition to though a speaker to verify audio quality. The oscilloscope allows for clear verification of both wave shape of the oscillator waveforms and the time varying response of the envelope generator. Testing via ear was able to verify filter performance in addition to sine wave purity. The human ear is very good at determining spectral content and thus it was simpler to listen for distortion and proper filtering than to try to understand the waveforms on the screen.

**Power Amplifier System Testing (Elaine)**

The input stage was tested by matching node voltage values with LTSpice simulation results. A 20mV signal was then sent through the input of the differential amplifier (the other input of the differential amplifier was grounded), with the expected result that the output would rail since the gain of this stage was around 3000. This gain had been estimated by adjusting a voltage divider at the front of the differential input until the output no longer railed. The gain was equal to the magnitude of this output divided by the the magnitude of the scaled down input. The VAS stage was first tested alone, once again by comparing quiescent voltages with simulation values. The VAS stage was then connected to the input stage, quiescent voltages were once again probed, and both stages were tweaked until the output also railed here. The DC offset of the input needed to also be adjusted, or a functioning amplifier might not display the rail to rail output in the oscilloscope output. Once the stage synthesis was complete, however, I noticed that the DC offset could be set to near zero.

A class AB output stage was then tested with the pre-output stages and negative feedback. Testing was done with both the eight ohm speakers and a silent eight ohm resistor when sound was not necessary. The amplifier was tested over the range of 20 Hz to 20 kHz, and input voltages up to 10 V peak to peak, with an amplifier gain of 4. Once this testing was complete, the class G stage was connected to the input and VAS stages. This new setup was tested across the same range of frequencies and amplitudes. Both the class AB and class G
amplifiers were tested using lab power supplies that gave current readings and the ability to set a current limit. Initially the lab kit power supply was used, but this ended in a diode melting within the labkit.

Transistors in the output stage had to be continuously tested as they would often burn out. A faulty circuit could be identified when the readings on the power supplies were imbalanced and the output wave form through the oscilloscope was significantly distorted. The transistors that were the most likely to fail were the transistors that fed directly into the power transistors, but not the power transistors themselves, as these were rated to withstand up to ten amps of current. When a transistor blew out, testing involved checking the operation of all transistors and diodes in the power stage and voltage amplifying stage. Possibilities of loose wire connections were probed by checking for open circuits using the voltmeter, while sinusoidal output distortion was checked using the oscilloscope.

Power Supply Testing (Lauren)

Testing occurred in several stages, as I built each section of my design. I first tested after connecting and heat shrinking the various connections of my transformers to the power cord for the wall socket. I checked that the output of my transformers were indeed stepped down from 110VAC to 18VAC and 24VAC. After verifying that, I tested my voltage regulation circuitry on a breadboard, to verify it produced the correct DC voltage. Next, after I had soldered my circuit to a perforated board, I tested that my circuitry was able to produce the desired output voltage under a load. The load I used for testing was a 8 Ohm 100W variable chasis resistor. By connecting the load resistor to each of my power rails, I was able to verify that my circuit supplied 3A at both +/-15V and +/-25V. After adding several capacitors to reduce output ripple and stabilize my op-amp, I tested again with the load resistor and verified that my power supply was successfully operating. The final testing we completed was when we integrated our systems together. I monitored my output voltages on both a multimeter and oscilloscope as both my partners’ hooked up their systems to my power supply. By monitoring that the output of my supply was a flat DC output at the correct voltage, I was able to verify that my power supply was correctly operating.

Results

Signal Processing System Results (Elliott)

All of the modules were successfully constructed on the breadboard and some of the modules were successfully constructed on the PCB. Every module proved useful and interesting. The system proved to be fun to play with and produced quality sounds of an incredibly large variety. I was able to generate a new tone every single time I sat down to experiment with the synthesizer. I plan on continuing to build the PCB to create a more permanent and stable synthesizer.
Figure 41: Completed Breadboard Project and Keyboard. Notice that the breadboard is a tangle of wires that is hard to use or keep from breaking. This was a major motivating factor to put the circuit on a PCB and into a nice case.

Power Amplifier System Results (Elaine)

Integration with the analog synthesizer was successful; I increased my gain to 11, as the analog synthesizer output signal was smaller than expected. The analog synthesizer output included sine waves, square waves, and sawtooth waveforms. The final amplifier showed little distortion at maximum output (42 V peak to peak) up to 17.4 kHz, which was well above the frequencies supplied by the analog synthesizer. Integration with the power supply was more difficult, although integration with the +25/-25 volt rails was successful. The design for the +/-15V rails worked previously for the analog synthesizer, it is likely that something was short circuited due to human error.

Power Supply Results (Lauren)

Figure 42: The Power Supply. This is a picture of the power supply, including the six transformers used, the four filtering capacitors, and the two perforated boards with the four voltage regulation circuits.
The power system was based on what the power amplifier and signal processing needed, which was a high voltage as well as a high current power supply. This was not an easy task, and several tradeoffs were made along the way. The power supply was able to supply both +/-25V and +/-15V at 3A with relatively zero output ripple. Supplying +/-15V to the analog synthesizer was successful. However, when we integrated the +/-15V and the +/-25V power supply with the amplifier, a short occurred and fried the +/-15V rails. I was able to replace and fix the +/-15V rails, by replacing the TIP120 transistors and the 2N2219 npn transistors. Overall, the four power rails that I constructed were successful in meeting the design specifications, and powering the project. Moreover, the power supply system was a practical but challenging project, and I am very satisfied with my system.

**Conclusion**

In conclusion, our project involved challenges in individual design and integration. The Analog Synthesizer proved to be an exciting project that covered a wide range of EE concepts. It also proved to be an exciting and interesting product to experiment with and play music with. The Power Amplifier worked to amplify signals from the analog synthesizer at high volume, but when tested showed some distortion at high frequencies. The Power Supply was able to supply both +/-25V and +/-15V at 3A and 2A respectively with relatively zero output ripple. Overall, our integration was a success; we were able to output sound from the analog synthesizer and draw current from the power supply to do so.

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