Nick Arango
6.101 Final Project Proposal Draft
Portable Electroencephalogram (EEG)

Introduction

Measurement of microvolt scale signals on the skull correlated with brain activity can provide useful data for doctors diagnosing sleep or brain disorders. The cost of electroencephalograms (EEGs) used to measure these small signals have decreased dramatically and consumer products promising in home sleep monitoring and even simple mind control toys have come to market. These products amplify the small EEG signals sensed while minimizing external interference, digitize these signals, and perform simple digital filtering to extract signals correlated with different thought patterns, sleep cycles or blinking.

The signal processing needed to analyze sleep or concentration is relatively simple. The EEG signal is split into several frequency ranges each correlated with different brain activity. The relative magnitudes of the frequency ranges indicate the type of brain activity. Due to the low frequency of the signals involved these signals can be computed by low power microcontrollers or analog electronics.

There are two standard ways of electrically connecting EEG circuitry to a user's head that each provide different strengths. Passive wet electrodes use a conductive gel to provide an electrical connection to a user. These electrodes can't contact skin through hair and are either non-reusable or require cleaning after each use. They do provide an advantage of low output impedance reducing noise in the system. Dry active electrodes can make contact through hair and don't require cleaning. However, their output resistance is rather high and need additional circuitry to reduce noise. In consumer applications dry active electrodes are their obvious choice due to the lower maintenance at the cost of increased circuit complexity.

Project Goals

This project aims to create a portable electroencephalogram (EEG) that can be used without preparation time to analyze concentration, blinking and sleep cycles. To achieve this goal we build active dry electrodes, filtered differential amplification, analog optical isolation, high selectivity bandpass filters, and thresholding. Figure 1 shows a block diagram of the system and the divide between the front end signal amplification and the back end signal processing.

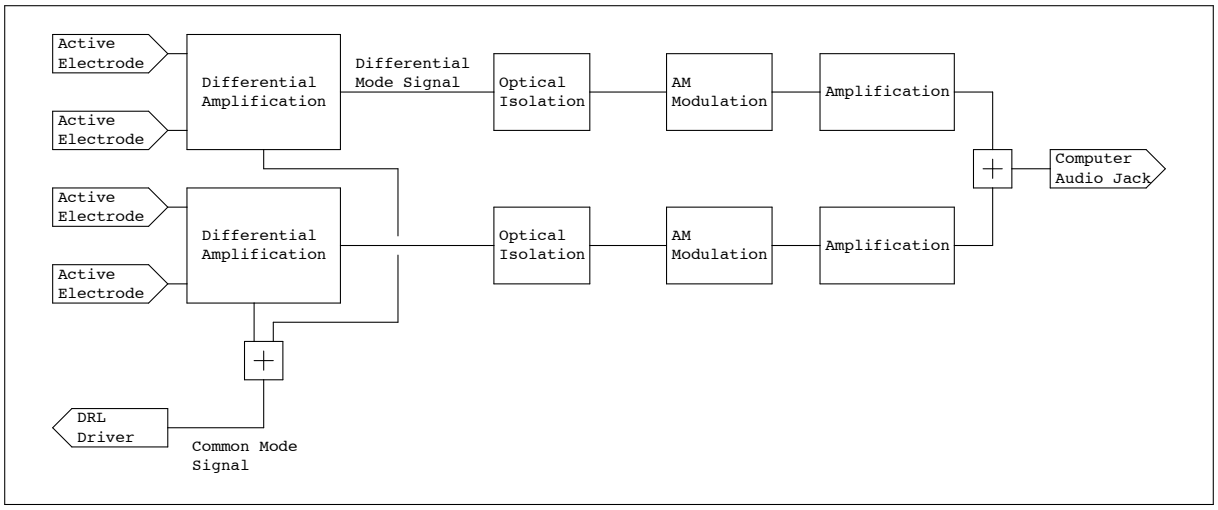

Figure 1: High level block diagram of the portable low noise EEG. Active electrodes connect to the scalp of the user and the output attaches the the laptop of the user

Front End Design

The analog front end takes small differential mode signals from dry electrodes attached to the scalp and amplifies the microvolt level signals at the frequencies 1 and 40 Hz that are correlated with brain activity. Because the sensed signals are so small, immunity from outside noise sources and reduction of noise from electrical components is critical. The major sources of noise are ripple on the power supply, RF interference on high impedance signals and component drift.

To avoid noise sources in the circuit itself, components precision low drift components must be selected. External noise will also couple into the system through the power supply so care must be taken in powering the front end. Sixty hertz mains interference will be minimized by powering the front end from 9 volt battery regulated to 5 volts. This constraint will drive the selection of low voltage single supply opamps and instrumentation amplifiers. Electromagnetic interference will be avoided by shielding and minimizing the length of wires carrying small high impedance signals. This impacts the design of the active dry electrodes. A block diagram of the front end is shown in figure 2.

The high output impedance of the dry electrodes necessitates buffering physically close to the electrodes to prevent electromagnetic interference. These low noise electrode buffers will provide 20dB of gain and shielding of short cable between them and the electrode. They will be implemented with a single supply low input current amplifier such as a JFET or CMOS input stage amplifier.

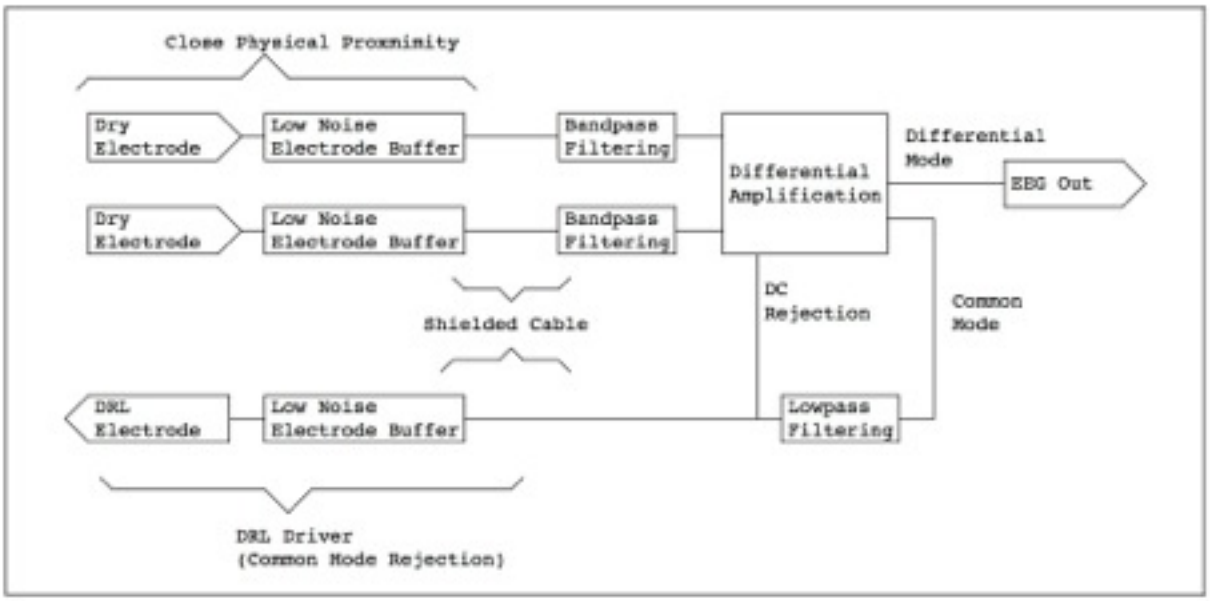

Figure 2: Block diagram of the analog front end of the EEG system. the dry electrodes and low buffers are the most critical components for low noise operation. The DRL electrode also reduces noise by boosting the common mode rejection ratio.

Because the EEG signal is inherently differential, once buffered, the electrode signals will be subtracted in a differential amplification stage with a gain of 80dB. The common mode signals will provide an additional noise source and while this is mitigated by the common mode rejection ratio of the amplifiers, further action can be taken. To reduce this source of noise, the body is driven to a potential to cancel out the common mode voltage of the electrodes. The common mode signal will be low passed before driving the body as the most prevalent common mode noise is 60Hz mains interference.

Designing this circuit will pose challenging due to the low noise requirements. Testing it will also pose a set of challenges. Bench function generators don’t provide the microvolt level signals needed to test the electrode buffers and differential amplifier. However, simple resistor attenuators can provide the necessary signals at reasonable common modes. The each of the amplifiers will be tested individually prior to integration in the front end by measuring the frequency response given microvolt inputs.

Isolation

Isolation between the analog front end and signal processing back end is necessary to prevent ground noise from swamping the EEG signal. The two halves will be isolated using an analog optoisolator with one internal LED and two matched internal photodiodes. One photodiode sits on either side of the isolation barrier. The photodiode

on the driver's side of the barrier is used in a transimpedance feedback loop. Because the two diodes are matched and receive the same light inside of the optoisolator package, the input voltage output diode current relationship is linear. Because EEG signals are very low frequency, there is little concern for bandwidth in this design.

This analog isolation circuit requires a specialty optoisolator but otherwise uses common off the shelf components.

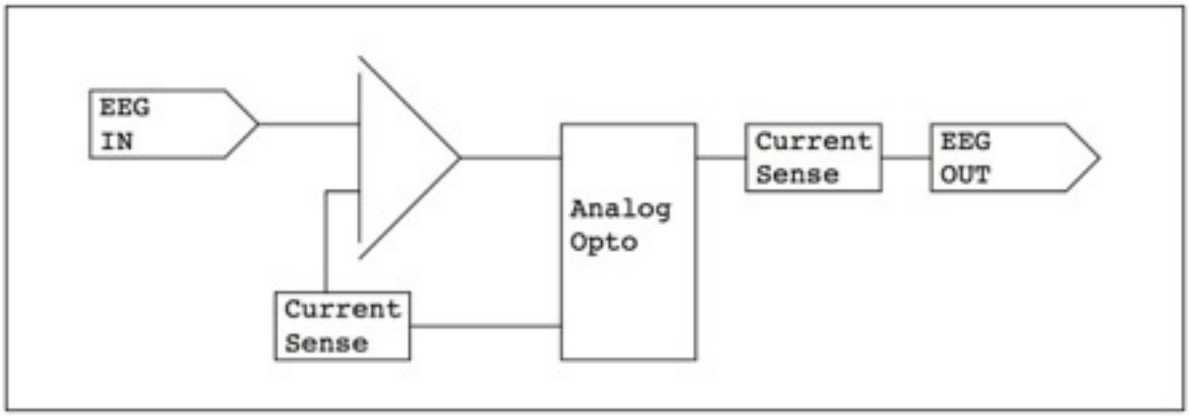

Figure 3: Diagram of the analog optoisolator. Feedback from matched photodiodes is used to ensure linearity while maintaining isolation

Conclusion and Schedule

Our design for is both modular and feasible with reasonably inexpensive components. Open source EEG schematics exist and will be used as a reference point for component selection. Each component can be tested individually (albeit with with the construction of additional circuitry.

By april 17th schematics will be designed and components will be purchased. This will allow for the construction of the active electrodes and differential amplifier over the next two weeks. These will be complete by April 27th and integrated together. The optical isolation circuit wont present significant difficulty because of the low bandwidth. This will be constructed the week of the 27th as all of the systems are integrated.