Hardware Neural Net Entertainment System (HNES)

Project Abstract

This project entails the creation of a neural network implemented as an FPGA-powered nested FSM hardware structure. The initial goal of the project will be to implement the output of one neural network layer using hardware matrix multiplication architecture. For complex networks this is a difficult computational task in itself with a significant amount of ongoing research. However, interesting usage applications can be solved on smaller network topologies. Once this initial step is complete, further goals will expand this architecture to implement neural network topologies with greater depth and width. A functional topology will be created to play retro video games such as those designed for the Nintendo Entertainment System (1985). This will be achieved by interfacing the FPGA with an x86 video-game system emulator on a host CPU. The emulator will output the game-state feature vector to the FPGA, which will then use the neural network FSM structure to drive controller outputs. As part of the project, layer weights will be trained using a custom-programmed FPGA-accurate neural net simulator on a computer. Possible challenges for this project include determining appropriate network depth, width, and topology to adhere to FPGA computation, memory, and bandwidth constraints. Stretch goals include training the network to play more than one game, and exploring different network topologies enabled by runtime-selectable bitmasks.

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