6.111 Neural Network Project Checklist

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1. **The Commitment**

   The minimum goal we will reach is a correct single layer computation. In this model weights and inputs are transferred from the PC, outputs computed on FPGA, and then outputs transferred back to PC for display. This goal will involve all components of the project; however, having only a single layer can greatly simplify the layer controller. If the next goal is not reached, the visual demonstration for this stage would be created by using the FPGA as a matrix-multiply coprocessor. This matrix multiplication can be visualized itself, or it can be used to accelerate graphics applications or other matrix-heavy workloads.

2. **The Core Goal**

   Our main goal is to extend the baseline implementation to the continuous computation of multiple feed-forward layers on the FPGA. The weights of the layers and inputs are still given by the PC and outputs sent back to it, but the FPGA is responsible for all intermediate computation. Given this functionality we could use the FPGA to execute arbitrary integer feed-forward networks that fit within the precision constraints set by the 25x18 multipliers on the DSP slices. If this is the final goal that we reach, the FPGA could be utilized to execute a test network. The inputs and correct outputs are determined on the PC, and for each set of inputs, the FPGA outputs will be compared to expected values. Even if the test network is not designed to perform meaningful computation, it will still correctly demonstrate the full functionality and capability of the project.

3. **The Stretch Goal**

   Our stretch goal is to utilize the above network structure to perform useful inference. This allows for interesting examples to be shown visually. Specifically, we will train a feed-forward network on the computer to play a chosen NES game, such as Super Mario Bros. This network will be then downloaded to the FPGA via sets of weight parameters. The specifics of the game execution and training of this network are unrelated to the main goal of the project itself (which is FPGA hardware inference), but doing so will grant us a compelling presentation of the functionality of our project.