

# FPGA Digital Synthesizer

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# System Overview

overview

interface

tone  
generation

recording/  
playback

control  
module

extensions

checklist

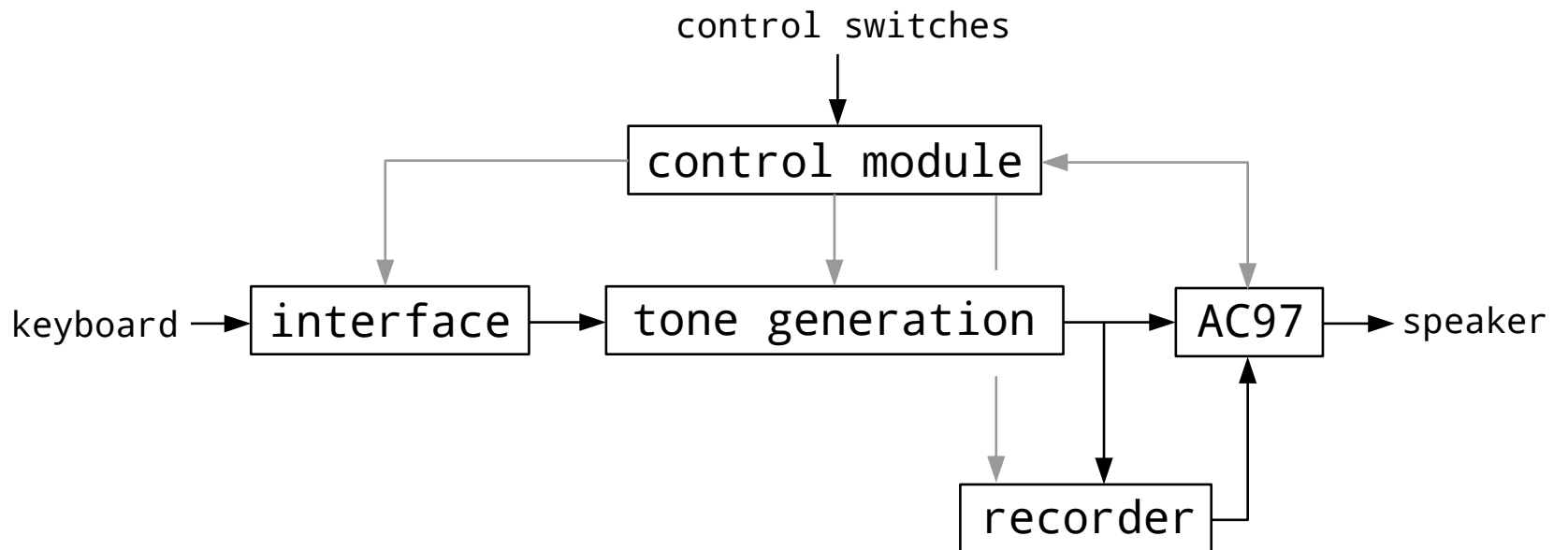
schedule

## System Input

- + notes from keyboard
- + octave select
- + volume
- + ASDR/effect parameters
- + record/playback settings (mode)

## System Output

- + audio from AC97
- + LEDs for setting visualization



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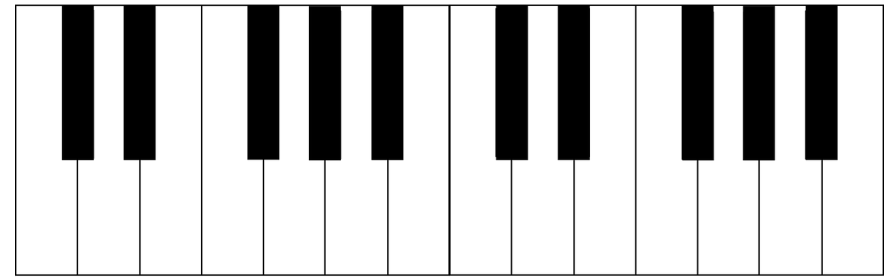
checklist

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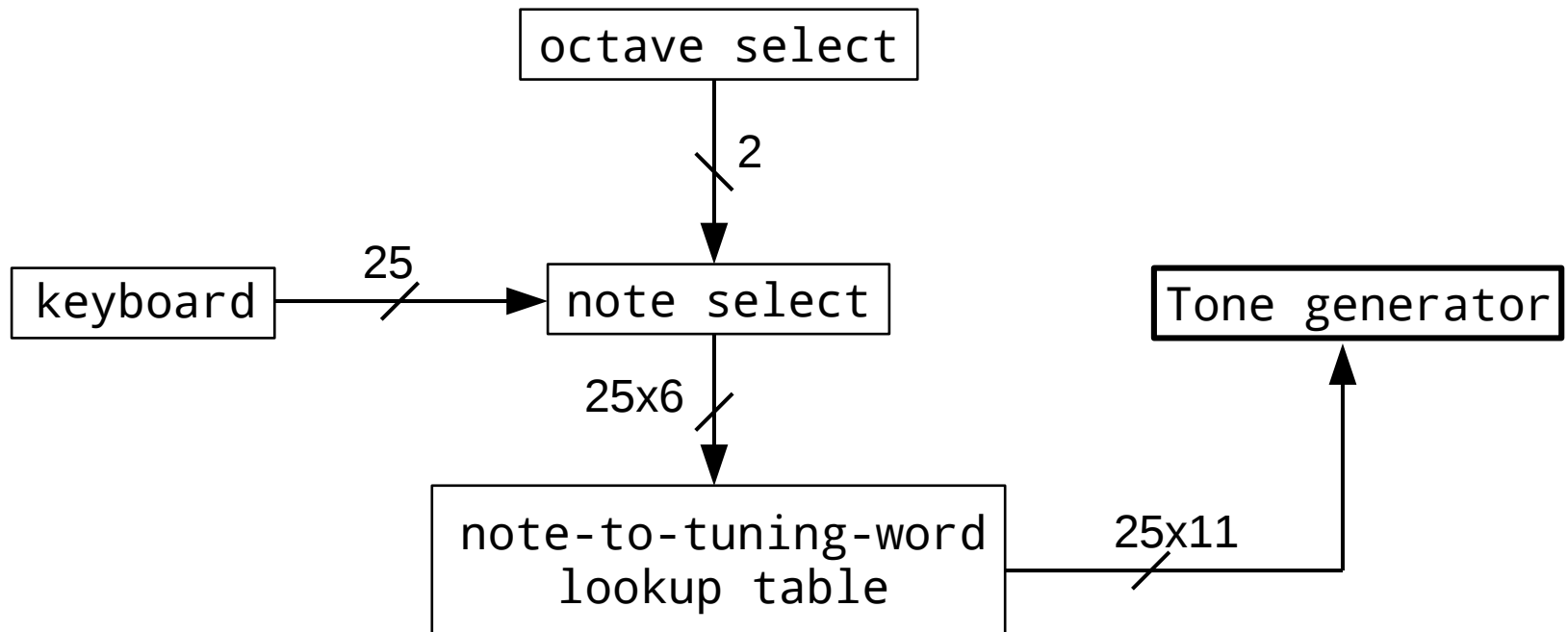
# Input Interface

## System Input

- + Two octaves worth of "keys"
- + Octave select
- + Buttons vs. MIDI



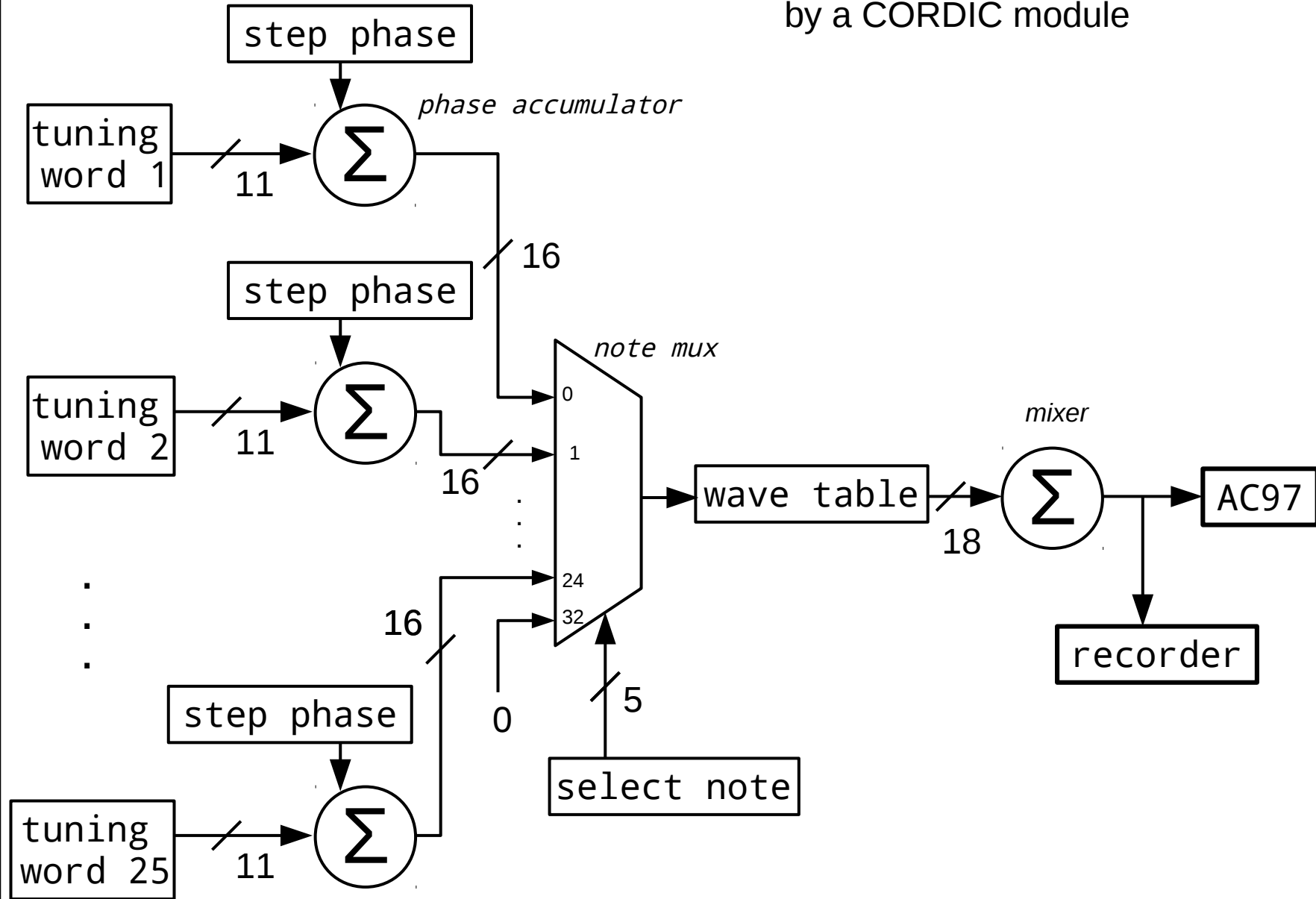
\* 56 possible notes (5 octaves)



# Tone Generation

\*wave table may be replaced by a CORDIC module

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- tone generation
- recording/playback
- control module
- extensions
- checklist
- schedule



# Recording and Playback

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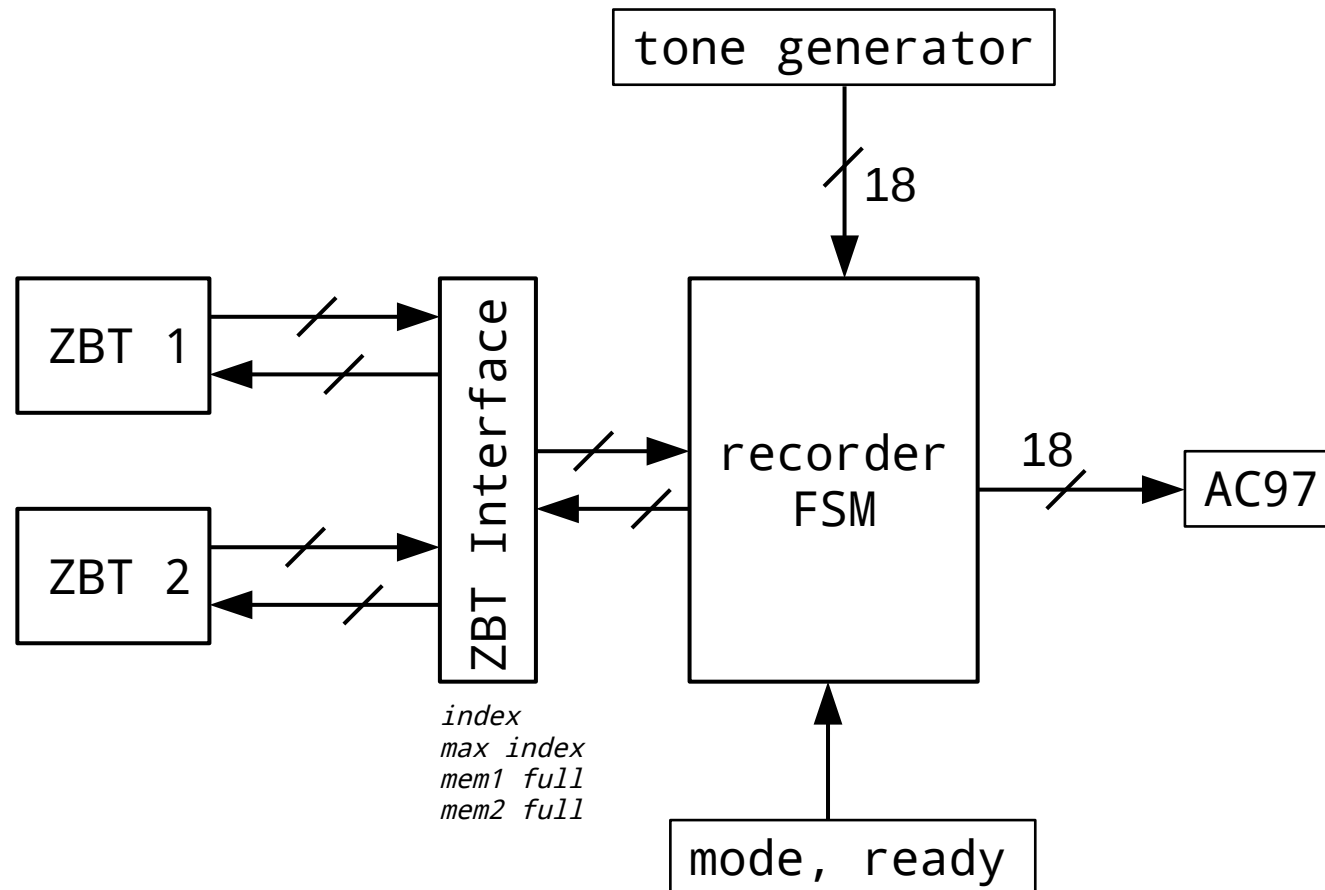
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## System Input

- + uses both ZBT memories
- + able to record approx. 1.5 minutes of audio (18b samples @ 12kHz)



# Control Module

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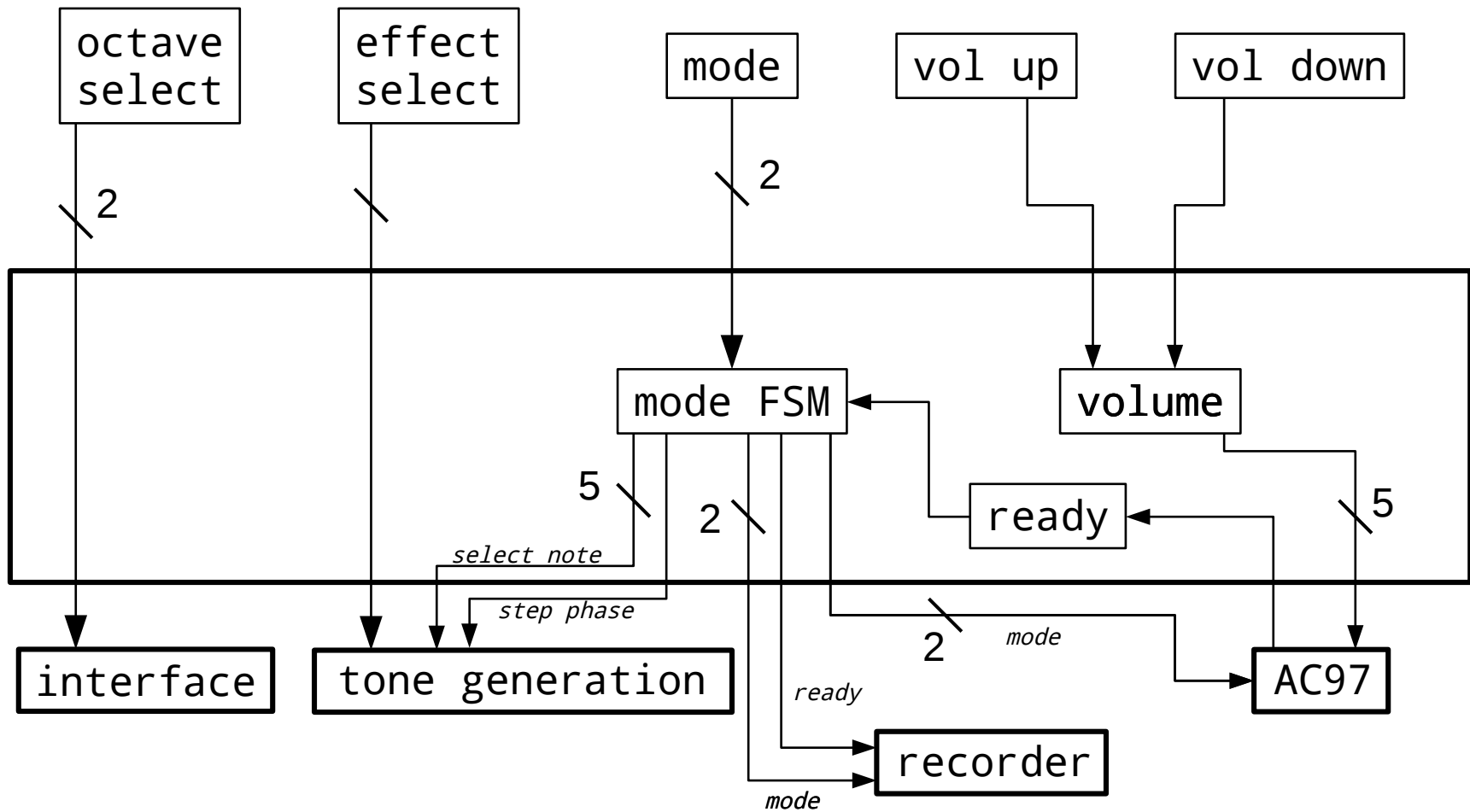
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# Beyond the Basics

## MIDI Keyboard

- + more ergonomic input
- + protocol interfacing
- + serializes input

## ADSR Enveloping

- + makes instrument sound more “real”
- + adjustable

## Audio Effects

- + overtones
- + reverb
- + echo

## Fancier Record/Playback

- + recording multiple samples/tracks
- + looping/record over playback
- + extra memory

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# Checklist

## Commitment

- + functional synthesizer with no “special features” (effects, enveloping)
- + button input
- + basic recording functionality

## Goal

- + MIDI input
- + multi-track recording & looping
- + enveloping and at least one static effect

## Stretch

- + multiple effects
- + adjustable effects
- + extra memory





# Project Schedule

## As of right now...

- + research
- + basic design finalized
- + wave table tone generator implemented

## Nov 12 – Nov 18 (this week!)

- + test tone generator
- + implement mixing
- + implement/test CORDIC module

## Nov 19 – Nov 25

- + finish memory recording/playback
- + integrate memory, interface, and tone generator

## Nov 26 – Dec 02

- + MIDI keyboard integration
- + ASDR enveloping
- + work on stretch goals

## Dec 03 – Dec 09

- + work on stretch goals
- + final integration and testing

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# Questions?

