Outline

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Project Goals

The principal goal of this project is to successfully design, implement, and test a low-power, low frequency (125 kHz) RFID tag reader for the passive RFID tags in MIT ID cards. The tag reader system, which will be based on the 6.111 Xilinx FPGA labkit, will be accomplished in the following manner:

- Build a transmitter antenna that will produce and send a 125 kHz AM sine wave interrogation signal to an MIT ID card.

- Build a receiver antenna that receives a 62.5 kHz AM sine wave reply signal, amplifies it, converts it to a digital format, and processes it to extract a stream of bits.

- Build a decoder that transforms the data to get identification data (MIT ID number).

- Build a video module that outputs the identification data to a display.
Subsystem Block Diagram: Transmitter

- Signal generator creates a constant 125 kHz sine wave
- Antenna transmits signal to transponder in card
• Amplitude modulated 62.5 kHz signal is received by a tuner, then amplified
• A/D converter module outputs a stream of 8-bit voltage values
• Raises adc_rdy when it has a new converted value
Subsystem Block Diagram: Bitstream Generator

- Peak detector compares latest 3 values of adc_out to determine peaks
- Downsampler selects every Nth peak
- Thresholding module converts voltage values to 0 or 1 by comparing to a threshold
- Decoder compares latest 2 values of th_out and computes XOR to find transitions
Subsystem Block Diagram: Descrambler

- Bitstream from decoder (repeating pattern of values) is input to frame detector.
- Frame detector finds beginning of sequence and outputs a frame—the next 224 bits—in parallel.
- Descrambler extracts and transforms the 32 bits relevant to the user ID.
Division of Labor

Katonio:
• Build 125 kHz AM transmitter
• Design 62.5 kHz receiver
• Code Thresholding module
• Code ID Descrambler module
• Code Video Display Module

Akua:
• Build 62.5 kHz AM receiver
• Code A/D converter
• Code Peak Detection & Downsampler modules
• Code Decoder module
• Code Frame Detector module
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06 November: Project proposal conference
11 November: Block diagram conference
15 November: Project presentation
18 November: Checklist conference

Construction of AM transmitter, AM receiver and A/D module complete

24 November: Completion of Bitstream Generator module
## Project Timeline: December 2005

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**02 December:** Completion of Descrambler and Display modules

**09 December:** System testing/debugging

Feature additions (time permitting)

**14 December:** Final Report due